Rp0352 Pixel Processor and Control Chip

INTRODUCTION

The Rp0352 Pixel Processor and Control (PP&C) chip (Figure 1) is one of two components that comprise the Rockwell USB Camera System. The PP&C takes 10-bit RGB digital image data from the Ri0352 Digital CIF format Imager (DCI) and performs signal processing and rate buffering. This data provides a fully compliant USB interface so image data can be transmitted over a USB cable to the USB-equipped host PC. Together with software drivers provided by Rockwell, designers will only need to interface with Microsoft Windows Device Models (WDM) to provide a finished product. WDM is available for desktop imaging and video conferencing applications.

As shown in Figure 2, the Rp0352 is designed to couple with the companion Digital CMOS Imager Array, the Ri0352: A CIF (Common Intermediate Format) image size of 352x288 pixels. With compression, the USB data rates are high enough for a PC display rate of 30 frames per second. A rate buffer inside the PP&C matches various exposure settings to the available USB bandwidth.

Interface to external RAM is available on the Rp0352 which provides an expanded exposure time/frame rate operating envelope. The Rp0352 passes configuration information to the companion Ri0352 imager chip via a 2-wire serial interface as well as providing the clock to the DCI. The PP&C Chip pin out is listed in Table 1.

FEATURES

- Companion chip to the Ri0352 Digital CIF Imager (DCI), a CIF format CMOS imaging device.
- USB interface
  - Bus powered device
- YCrCb digital data stream
  - Compatible with H.324 and H.323
- Supports CIF (352x288), CIF Square Pixel (320x240) & QCIF (176x144) resolutions
- Variable frame rates up to and including 30 fps at full CIF resolution using built in hardware compression
- Software driver reconstructs 24-bit RGB from high speed serial data stream received from device
- Configuration of Ri0352 via 2-wire serial interface
- Frame buffering at 16Kbits internal memory with the option of an additional 256Kbits or 1Mbits of external SRAM
- Drives the Ri0352 with exposure times from 100µs to multiple seconds for capture of quick action or low light performance.
- Multi-term color correction function for excellent color fidelity
- Programmable detail enhancing filter for sharp images.
- Bilinear video scaler provides smooth image resizing
- Fully programmable gamma correction to match the linear response of the Ri0352 to the non-linear response of various CRT based display devices.
- Built-in hardware acceleration for host assisted Automatic Gain Control (AGC) and Automatic White Balance (AWB).
- Power: 150 mA at 3.3 V (nominal)

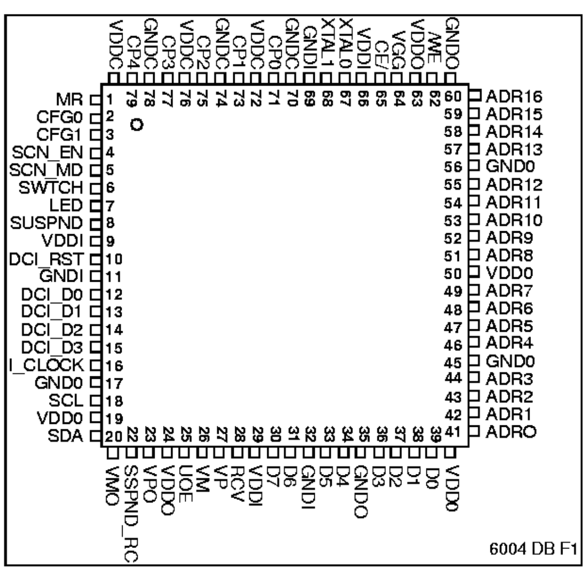


Figure 1. Rp0352 Pixel Processor and Control (PP&C) Chip

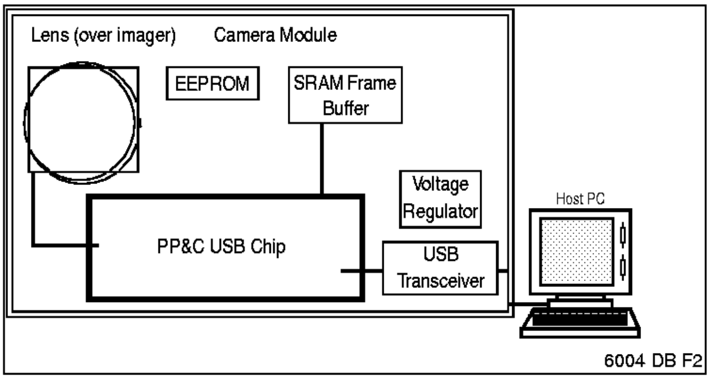


Figure 2. USB PC Camera System Block Diagram

TECHNICAL DESCRIPTION

The Rp0352 PP&C provides the following functions as illustrated in Figure 3.

- Control and interface to the Ri0352 DCI and optional EEPROM.
- Digital signal processing for the DCI: RGB interpolation, gamma correction, color correction, gain adjust, color space conversion from RGB to YcrCb, and video scaling.
- Provide output in CIF (352X288), CIF square pixel (320X240), or QCIF (176X144) resolutions.
- Frame buffer control: Controls an optional external frame buffer, which stores processed data waiting to be sent over the USB interface.
- USB interface: Sends processed video data and image statistics to, and receives command and control information from, the host computer.
- USB Camera Power Management.

RI0352 CONTROL AND INTERFACE

The video data stream along with embedded synchronization information is conveyed out of the DCI to the PP&C through a multiplexed 4-bit digital bus. The 4-bit bus transmits the 12-bit words 3 nibbles sequentially. The control of the DCI is passed from the host application software to the PP&C via the USB and then from the PP&C to the DCI via a two-wire serial interface.

PIXEL PROCESSOR (PIP)

The pixel processor (PiP) transforms raw imager RGB pixels to YCrCb video suitable for transmission to the host computer. This is a pipelined processor capable of processing a full frame in as little 1/30 of a second. The PiP can be bypassed, letting raw imager data through, by changing a control register. A block diagram of the pixel processing is shown in Figure 4. The paragraphs that follow detail each block in the PiP block diagram.

Data Receive and Synchronize

This block interfaces the image processing section of the PP&C with the DCI. It must synchronize with the correct nibble and then decode DCI control codes for determining current position within the image.

Fixed Pattern Noise Reduction

The image quality is improved by suppressing fixed pattern artifacts in the image. This block equalizes the black-level of the image on a column by column basis. A digital fixed pattern noise reduction capability is activated in lieu of the DCI's own analog fixed pattern noise reduction circuit with the benefit of lower overall temporal noise.

Defective Pixel Correction

A maximum of 16 defective pixels may be masked. The defective pixel value is replaced by the average of its two nearest neighbors on the left and right that are of the same color. The bad pixel coordinates are stored in an external serial EEPROM that is accessed by the PP&C through the serial control interface.

Interpolation to Rectangular Grid

Three color components associated with a pixel are obtained from the three surrounding RGB values. Therefore, adjacent pixels on the same line share a common color component. Since the Ri0352A pixels are not on a rectangular grid, this block performs interpolation to put it on a rectangular grid.

Color Correction & Gain Adjust

Color correction is applied to all pixels of the color image to ensure accurate color reproduction. The gains of the corrected RGB values can be adjusted and are host programmable.

Gamma Correction

The gamma correction circuit is used to compensate for display gamma. CRT's have a nonlinear relationship between the displayed brightness and the applied input voltage. Therefore, in order to maintain an accurate image, the input is pre-distorted.

Color Space Converter

The Digital Color Space Converter converts a 24-bit digital input in the RGB format to a 24-bit digital output in a YCrCb format.

Color Balance Histogramming

Image statistics are computed over the entire frame for use by the host computer in white balance control. The host computer reads this histogram data and adjusts the color correction matrix accordingly.

Brightness Histogramming

The screen is divided into two regions: Center and Periphery, each with its own running sum of luminance values for that frame. The screen is segmented so that scene characteristics, such as bright overhead lights can be de-emphasized while the image at the screen center is optimized for contrast.

The host computer reads the brightness histogram data at the end of the frame, and adjusts the color correction matrix, imager gain, and integration time to achieve good image contrast.

Digital Video Scaling

The Digital Video Scaler supports the following output formats:

- CIF 352x288 (CCIR601 aspect ratio)
- QCIF 176x144 (CCIR601 aspect ratio)
- CIF 320x240 (square pixel)

The desired output resolution is obtained by scaling the input 352x288 4:2:2 video horizontally and vertically.

Horizontal Scaling

- 352 to 176 (QCIF): Decimate-by-2
- 352 to 320 (CIF Square Pixel): Fractional scale by (10/11)

Fractional Scaling

The fractional scaler alters the sampling rate by a factor of (10/11). That is, the fractional scaler outputs 10 pixels for every 11 input pixels. The decimating filters perform horizontal filtering on the luminance Y and the chrominance CrCb.

Vertical Scaling

- 288 to 240 (CIF Square Pixel): Fractional scale by (5/6)
- 288 to 144 (QCIF): Averaging scale by (1/2)

To minimize the number of line stores (and complexity), vertical scaling algorithms are used. For vertical scaling by the factor (5/6), the pixel value between two vertically adjacent pixels A and B on adjacent lines is obtained by bilinear interpolation.

Edge Enhancement Filter

The subjective image quality can be enhanced by the application of an edge enhancement filter. A horizontal only FIR is employed. There are three settings–High, low, and off.

Compression

The PP&C can activate a compression capability to get approximately a 4 to 1 compression of the data stream. This allows for 30 frame per second full CIF resolution mode if most of the USB bandwidth is granted and the compression artifacts can be tolerated.

Frame Buffer Control

The PP&C can be configured for modes that bring data from the DCI at a higher instantaneous data rate than the available USB bandwidth. An optional frame buffer can be deployed to temporarily hold the processed imager data for the period that it takes to transmit the image to the host computer.

There are three buffer options available:

- 1Mbit buffer using 128KX8 bit asynchronous SRAM
- 256Kbit buffer using 32KX8 bit asynchronous SRAM
- No external buffer

USB Interface

The function of the USB interface is to accept YCrCb data from the PiP and send it through the USB bus to the host. It is also responsible for sending image statistics used for white balance and brightness control. It also accepts command and control information from the host computer and relays it to the PiP and DCI.

PC INTERFACE (USB)

The Rockwell USB camera system has a built-in fully compliant Universal Serial Bus (USB) interface for transfer of image and control data per USB specifications. Rockwell provides USB and WDM drivers allowing systems integrators to easily connect to common desktop imaging and video conferencing applications.

USB Camera Enumeration

The information that is transmitted to the host at power-up includes:

- Device descriptors
- Config descriptors
- Interface descriptors
- Endpoint descriptors
- String descriptors

The USB core detects the “Get Descriptor Command“ and signals the event on to the application bus. The application responds by sending descriptors. Other commands include:

- Write to Serial Control Interface Controller
- Read from the Serial Control Interface Controller
- Write to PP&C register bank
- Read from PP&C register bank

Configuration Information in Serial EEPROM

The USB configuration information is stored in a Serial EEPROM. If not enumerated based on one configuration the second one will be used.

The changes from one configuration to the next are in bandwidth allocations and not in the number of endpoints associated with the device. Other data stored In the serial EEPROM includes Bad Pixel Coordinates, 4 bytes of “Descriptor Size” and “Descriptor Address” for the USB configurations (4 bytes per configuration), and 3 types of USB configuration data.

If the device is not enumerated using the default configuration, the next configuration is tried and so on. The configuration data stored in the serial EEPROM is accessed through the Serial Control Interface as a response to the “Get Config” command from the USB host.

EXTERNAL BUFFER MEMORY

The PP&C interface allows the PP&C to optionally use low cost external asynchronous SRAM to buffer image data beyond what is provided on the PP&C. The internal frame buffering is set at 16Kbits and is sufficient for low cost camera configurations. The optional external frame buffer size can be set to 256Kbits or 1Mbits when interfaced to the SRAM. Higher performance camera systems will want to make use of the expanded exposure time/frame rate operating envelope the larger memory provides.

POWER MANAGEMENT

The combined chip solution is designed to meet the USB requirements of a bus-powered device. The camera will not need an external A/C adapter. It also supports the required USB ultra low power suspend mode. Since the A/D and sensor subsections of the Ri0352 imager chip need a full 5V for operation, the PP&C device was constructed with a built in charge pump driver to allow this supply voltage to be generated from the low USB supply voltage of 4.4V. Figure 5 shows the recommended power supply scheme. The frame buffering SRAM is operated directly off the 4.4 to 5.25V supply provided by the USB bus. A voltage regulator is used to provide a stable 3.3V supply to the PP&C. 3.3V operation allows the PP&C to run at high speeds with low power.

Power Requirements

The PP&C has three operating modes and associated power dissipation limits. When master reset is applied, the power consumption is limited to the amount allowed in the Initial state. In the Initial state, the PP&C will keep the DCI and the external SRAM buffer in their low power states. The pixel processing circuitry does not need to run, because no pixel data is coming from the DCI. However, the PP&C will be able to communicate with the host via the USB, and will be able to communicate with the DCI through the DCI serial control interface.

In the Active state, both the DCI and PP&C are fully functional and generating real time digital video signals.

In the Suspend state, both the DCI and PP&C are in the lowest power consumption mode possible, with all clocks stopped and all DC bias circuits disabled.

Mode	Maximum PP&C Current
Active	150mA
Initial	100mA
Suspend	150µA

Charge Pump Driver

The PP&C has the capability of providing power for the DCI A/D Vdd and Imager Vdd. The PP&C provides a high current output capability for an external discrete charge pump to develop a high enough voltage to power a 5V LDO linear regulator to provide the 5V necessary for the analog sections of the DCI. The charge pump driver output must generate a high current square wave output. The phase of the charge pump switching corresponds to the pixel time boundaries in the DCI to prevent generating switching noise during pixel quantization.

Overall Power Up Sequence

- Master Reset is applied
- No clocks to DCI
- Charge pump off
- Bus Enumeration process begins and completes
- Enable DCI (power and clock)
- Program DCI registers
- Program PP&C registers and LUTs
- Send Start to the camera (by setting a bit in a register).

Table 1. PP&C Chip Pin Out

Pin #	Pin Name	# of Pins	I/O	Function
USB Transceiver Interface				
25	UOE#	1	OUT	Output enable. Active low, enable the transceiver to transmit data on the bus. When not active the transceiver is in receive mode.
23,21	VPO,VMO	2	OUT	Outputs to differential driver.
28	RCV	1	IN	Receive data.
27,26	VP,VM	2	IN	Gated version of D- and D+. Outputs are logic “0” and logic “1”. Used to detect single ended zero (SE0#), error conditions, and interconnect speed.
8	SUSPND	1	OUT	Indicates when the USB core is in suspend mode, used to power down transceiver chip.
DCI Interface				
16	I_CLOCK	1	OUT	Master clock for DCI imager operation
12	DCI_D0	1	IN	Multiplexed RGB imager data bus, LSB
13	DCI_D1	1	IN	Multiplexed RGB imager data bus
14	DCI_D2	1	IN	Multiplexed RGB imager data bus
15	DCI_D3	1	IN	Multiplexed RGB imager data bus, MSB
10	DCI_RST	1	OUT	Reset pin to initialize DCI.
18	SCL	1	OUT	Clock for SCI bus (no pull up necessary, never tri-states)
20	SDA	1	I/O	Bi-directional serial data for SCI bus (internal pull-up)
SRAM Interface				
2:3	CFG[0:1]	2	IN	PP&C configuration, connect to logic high or logic low, do not leave floating: 0=No External Memory 1=256Kbit 2=1Mbit
39:36,34,33,31,30	D[0:7]	8	I/O	Data bus *
41:44,46:49,51:55, 57:60	ADR[0:16]	17	OUT	Address bus of optional external frame buffer SRAM *
62	/WE	1	OUT	Read write/ line *
65	CE#	1	OUT	Chip enable, used for power conservation, needs to be able to drive within 0.2V of VDD (3.3V or 5V) for SRAM standby low power mode. Connect to 100K pull-up resistor to SRAM VCC pin. This pin must tri-state when PP&C enters suspend low power mode to prevent damage to chip.
Note: * In USB suspend mode, the SRAM must enter its low power standby mode, this requires that all its inputs must drive within .2V of either SRAM supply.				

Table 1. PP&C Chip Pin Out (Cont'd)

Pin #	Pin Name	# of Pins	I/O	Function
Miscellaneous				
71,73,75,77,79	CP[0:N]	5	OUT	High current charge pump driver outputs, wired in parallel to achieve needed drive capability.
1	MR-	1	IN	Master reset. Active low. With hysteresis for allowing simple RC network for reset generation.
68	XTALI	1	IN	Crystal oscillator input.
67	XTALO	1	OUT	Crystal oscillator output.
6	SWTCH	1	IN	General purpose switch input for snap shot or other use, internal pull-up.
7	LED	1	OUT	LED driver capable of driving 20mA continuous.
22	SSPND_RC	1	IN	Power-on sequence suspend. Connect to RC circuit.
Power Supply Connections				
9,29, 66	VDDI	3	PWR	Digital 3.3V power for logic core.
19, 24, 40,50, 63	VDDO	5	PWR	Digital 3.3V power for regular digital output drivers.
72,76, 80	VDDC	3	PWR	3.3V power for charge pump drivers.
11,32, 69	GNDI	3	PWR	Ground for logic core.
17, 35,45, 56,61	GNDO	5	PWR	Ground for regular digital output drivers.
70,74, 78	GNDC	3	PWR	Ground for charge pump drivers.
64	VGG	1	PWR	ESD protection diodes, connected to highest voltage in system.
Scan Chain				
4	SCN_EN	1	IN	Configure F/F's for scan mode, internal pull-down.
5	SCN_MD	1	IN	Scan mode pin select, internal pull-down.
Total pins				
		80	Total Pins	

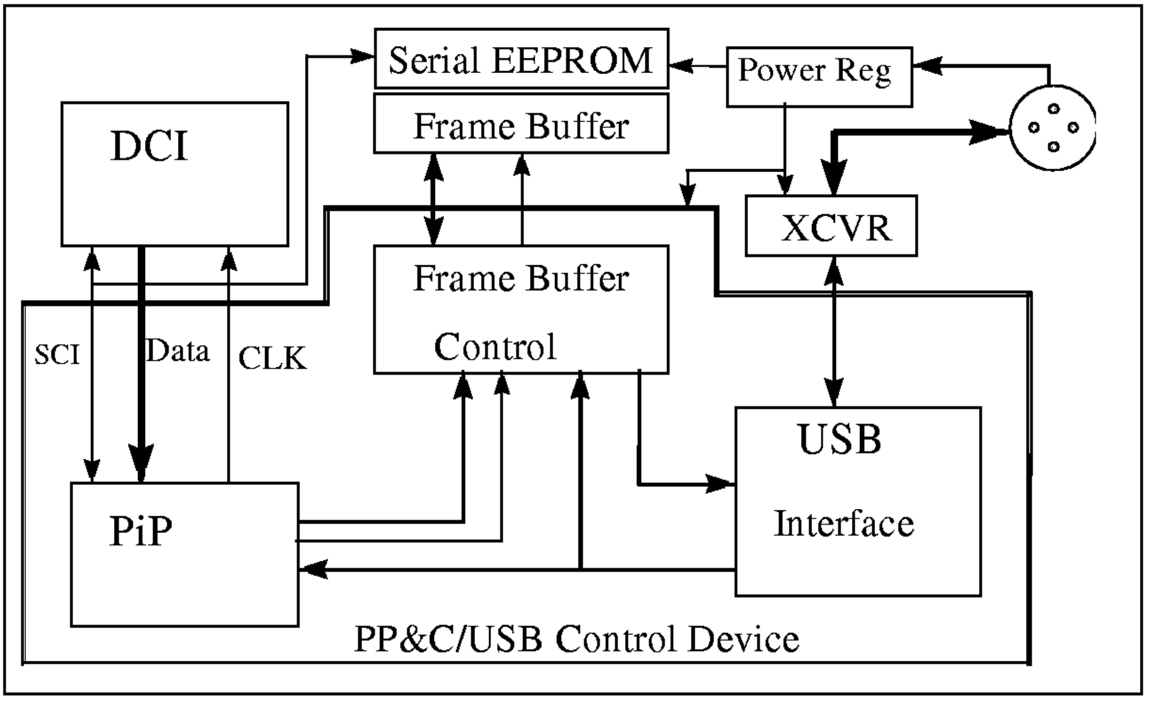


Figure 3. Camera Architecture

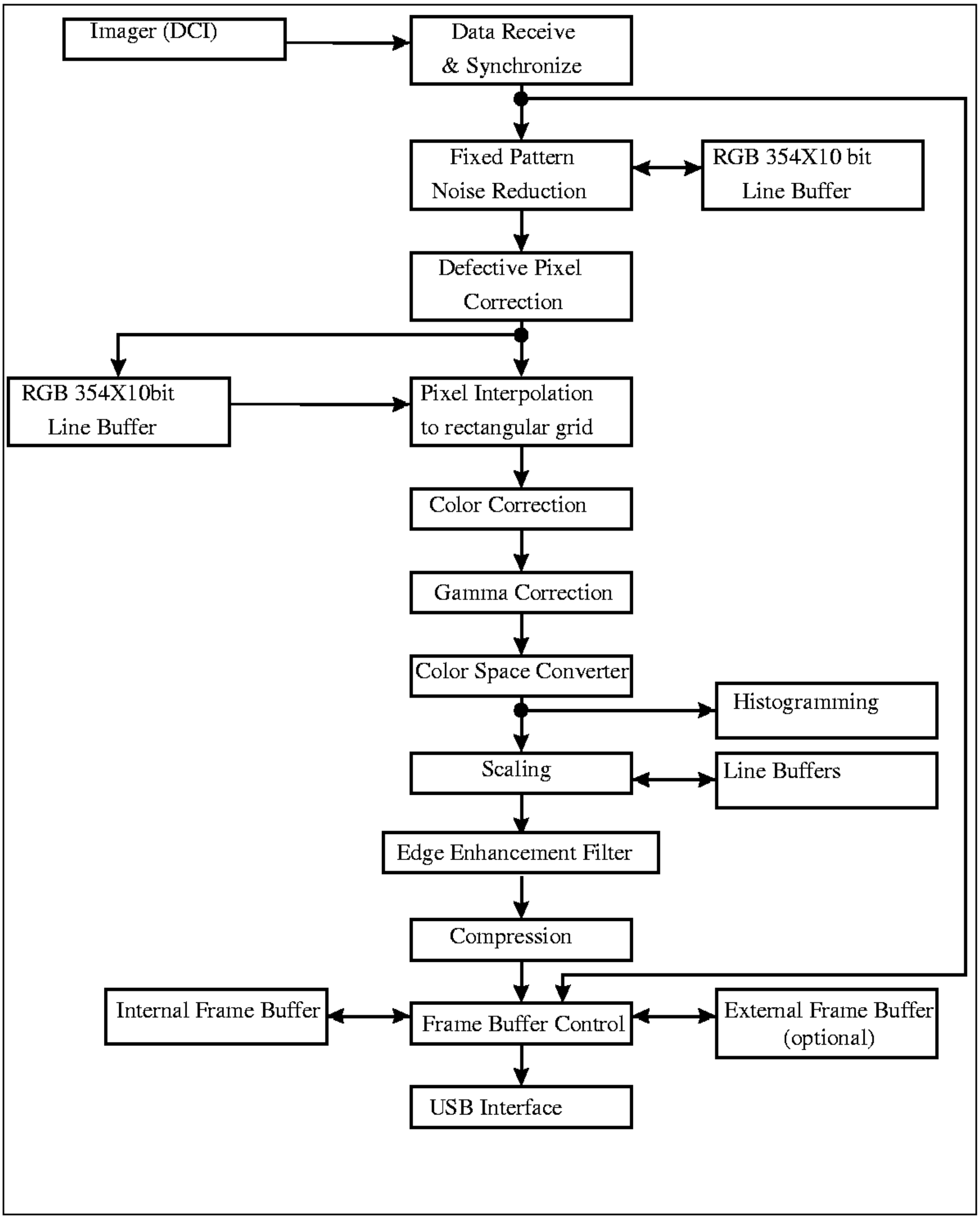


Figure 4. PiP Block and Flow Diagram

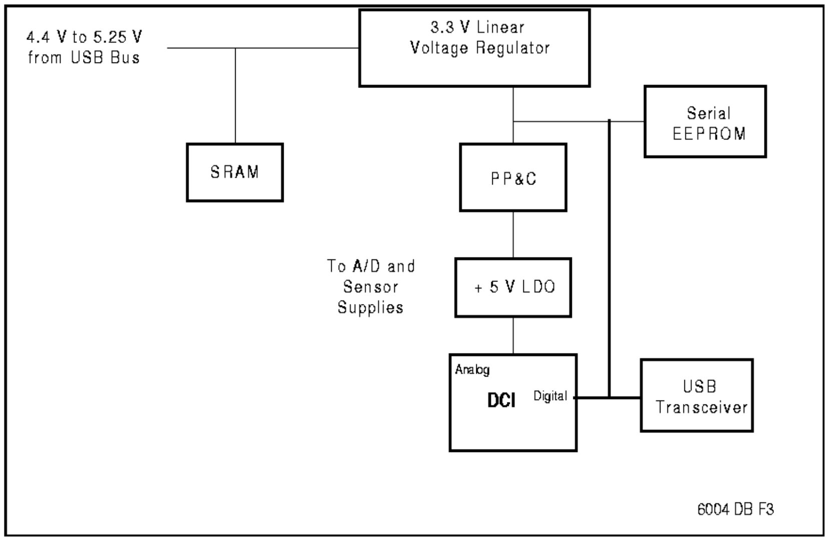


Figure 5. Power Supply Grid for USB Camera System

CLOCKING

The system clock is 48MHz. The clock is generated by use of a conventional crystal oscillator utilizing a 48MHz 3rd overtone crystal and inverting amplifier integral to the PP&C. The oscillator is designed to operate with low cost crystals. The oscillator circuit allows for overdriving from an external oscillator/driver circuit for testing purposes.

TEST ACCESS

The PP&C supports scan chain test access. Internal memories are tested with a BIST circuit.

SYSTEM RECOVERY

If the host determines that the camera state is lost, the PP&C and DCI can be commanded to reset via the USB bus.

REGISTER DEFINITIONS

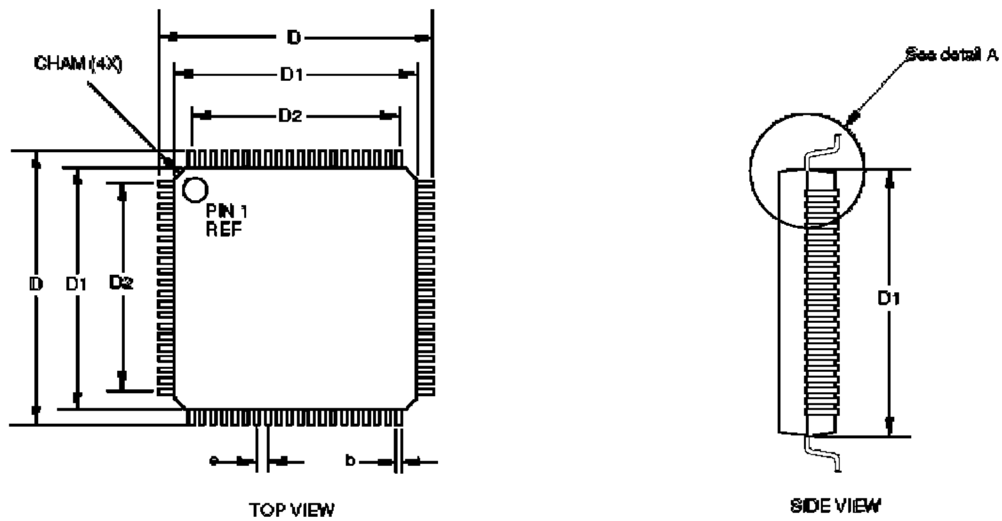
PP&C registers that are double buffered and allow read back return the operational register contents but not the shadow register. Double buffered registers will transfer the shadow registers to the operational register upon frame sync. Table 2 lists each register with its associated description.

DEVICE PACKAGE

The 80-pin PQFP device package is shown in Figure 6.

Table 2. Register Definitions

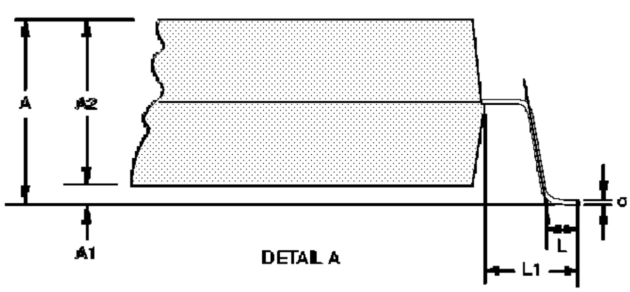
Register	Description
Color Correction Matrix Coefficients	Used for color balance and brightness control.
White Balance Histogramming Parameters	Sets criteria for acceptance as a "white" pixel for inclusion into white histograms. There are 3 of these register pairs, one each for video component (Y, Cr, and Cb).
Brightness Histogramming Parameters	Divides the screen into 9 rectangular regions. There are four registers: X1,X2,Y1,Y2. The statistics collection precedes the scaling process so valid X values are 0-351 and Y values are 0-287.
Defective Pixel Map Registers	These are register triplets used to store the sorted list (left to right, top to bottom) of defective pixels to be compensated by the PiP. This RAM area is large enough to hold coordinates for 16 defective pixels.
Gamma Correction LUT	256 word RAM is used for the gamma correction function.
Gamma Correction Block RAM BIST Configuration Register	Contains configuration bits for the gamma correction block's RAM BIST.
Scaler Configuration Register	Holds configuration of scaler block.
Scaler RAM BIST Status Register 1	Holds the status (read only) of the BIST for RAM in the scaler block.
Clock Generator PiP Reset Register	Holds the PiP reset control address.
Clock Generator Configuration Register	Holds clock generator block configuration information.
Data Receive & Synchronize (DRS) Configuration Register	Holds DRS configuration information.
Data Receive & Synchronize (DRS) Debug Register	Holds the short frame count used to speed simulation. It is used in conjunction with the DPC short frame debug register. In normal operation, this register will not be used. This register is write only.
Defective Pixel Correction (DPC) Debug Register	Holds the short frame count used to speed simulation. It is used in conjunction with DRS short frame debug register. In normal operation this register will not be used. This register is write only.
Fixed Pattern Noise Reduction Circuit Configuration Register	Holds configuration information for the fixed pattern noise reduction block.
Rectangular Interpolation and Decimation Circuit Configuration Register	Contains configuration bits for the RID block's RAM BIST.
Frame Buffer Configuration Register 1	Read only register that allows the host to read the state of 2 external pins.
Frame Buffer Configuration Register 2	Holds configuration telling the FBC which RAM mode it should operate from. In general, FBC configuration register 1 would be read by the host and then written to by this register.
Frame Buffer Configuration Register 3	Holds configuration information to indicate which data stream the FBC should read and relay it to the USB.
Frame Buffer Configuration Register 4	Holds address boundary between the luma (lower) and chroma (upper) partitions in the internal RAM.
Frame Buffer Configuration Register 5	Holds address boundary between the luma (lower) and chroma (upper) partitions in the optional external RAM.
Frame Buffer RAM BIST Control Register	Contains controls for the FBC block's RAM BIST.
Frame Buffer RAM BIST Status Register	Contains the status bits for the FBC block's RAM BIST.
Edge Enhancement Filter Configuration Register	Holds PiP configuration information.
Compression Configuration Register 1	Holds configuration information for the compression block.
Compression Configuration Register 2	Holds configuration information for the compression block.
Serial Controller Configuration Register	Holds serial controller block configuration information.
Brightness Statistics	Holds the results accumulated for two regions. The statistics collection precedes the scaling step. These registers are double buffered with shadow registers being updated from the operational registers upon frame synchronization. This register is read only.
Color Balance Statistics	Hold the results of 4 quadrant binning in the CrCb plane of "white" pixels



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	2.4 MAX		0.0946 MAX	
A1	0.05	0.35	0.0020	0.0138
A2	2.0 REF		0.0787 REF	
D	16.95	17.45	0.6673	0.6870
D1	14.0 REF		0.5512 REF	
D2	12.35 REF		0.4862 REF	
L	0.73	1.03	0.0287	0.0406
L1	1.6 REF		0.0630 REF	
e	0.65 BSC		0.0256 BSC	
b	0.25	0.45	0.0098	0.0177
c	0.13	0.19	0.0051	0.0075
Coplanarity	0.1 MAX		0.004 MAX	

Ref: 80-PIN PQFP (GP00-D227)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.



PD-PQFP-80 (040695)

Figure 6. 80-Pin PQFP Device Package

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