IBM Packet Routing Switch
Serial Interface Converter

Datasheet

Preliminary

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IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction,
NY 12533-6351

The IBM home page can be found at
http://www.ibm.com

The IBM Microelectronics Division home page
can be found at http://www.chips.ibm.com

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Contents

List of Figures

List of Tables

1. General Information

1.1 Features

- Companion to IBM Packet Routing Switch PRS28.4G and IBM Packet Routing Switch PRS64G
- Support for internal (8-port) and external (16-port) switch speed expansion mode
- Proprietary 440 Mbps and 500 Mbps, eight high-speed transceiver logic (HSTL) pair, data-aligned synchronous link (DASL) switch interface
- 3.52 Gbps aggregate throughput per speed expanded port
- 32-bit ingress/egress protocol engine (PE) interface bus (UTOPIA-3-like bus)
- Implements switch plane redundancy system architecture with two independent paths
- Three-packet ingress and six-packet egress shared buffers
- Up to four priority levels in packet handling
- In-band flow control (IBFC) via packet header information
- Out-of-band flow control (OBFC) to the PE through an external serial bus
- Programmable packet length of 64 to 80 bytes
- Link-liveness yellow packet insertion
- 8-bit processor interface, with bursting option
- Internal array built-in self test (ABIST)
- IEEE 1149.1 standard boundary scan to facilitate circuit board testing
- 1.5 V differential inputs/outputs (I/Os) for data-aligned synchronous links
- 2.5 V supply voltage (3.3 V-tolerant I/Os) and 3.3 V low-voltage transistor-transistor logic (LVTTL) for the other signal I/Os
- 25 × 25 mm 360-lead ceramic ball grid array (CBGA) package
- IBM complementary metal-oxide semiconductor (CMOS) 6 SF SA-12E technology

1.2 Description

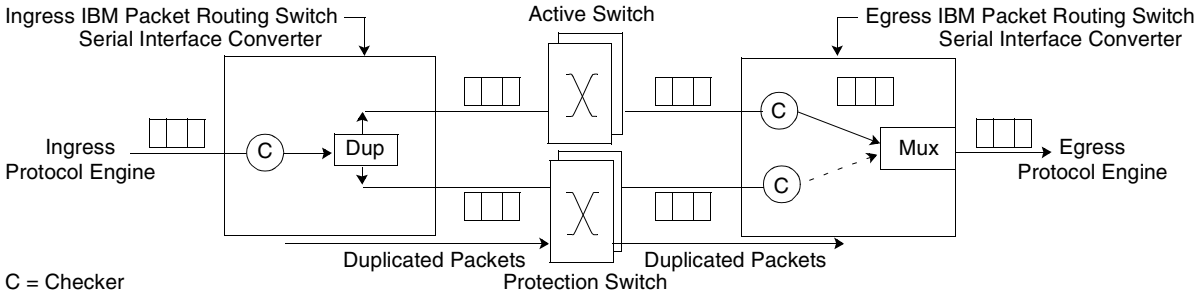
The IBM Packet Routing Switch Serial Interface Converter (the converter) is a companion device to the IBM Packet Routing Switch PRS28.4G and the IBM Packet Routing Switch PRS64G (the switch). It connects the switch's serial link to a Protocol Engine (PE) on a 32-bit interface bus. The converter attaches to a switch port operating at up to 4 Gbps in speed expansion mode, wired on eight DASL pairs running at up to 500 Mbps per pair.

No synchronization is required between input ports. However, packets on a given port are always received or transmitted at a fixed interval equal to the packet length. The converter ingress/egress packet length is programmable from 64 to 80 bytes in increments of four bytes. Input/output packets to and from the switch are mapped into blocks of four logical units (LUs), each of which consists of 16 to 20 bytes depending on the packet length.

The converter is composed of two fully independent data paths (X and Y) to provide a resilient switch fabric. These paths are clocked, reset, and controlled independently to support independent activation and deactivation of each switch plane.

Ingress traffic (packets received from a PE interface bus) is routed to both X and Y path switch planes, thereby duplicating packets on both planes. Egress traffic (packets received from switch plane X or Y) is routed to a bus. See Figure 1-1.

Figure 1-1. Overall Switch Subsystem Configuration

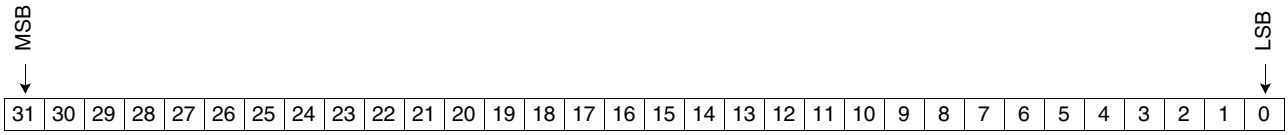


1.3 Ordering Information

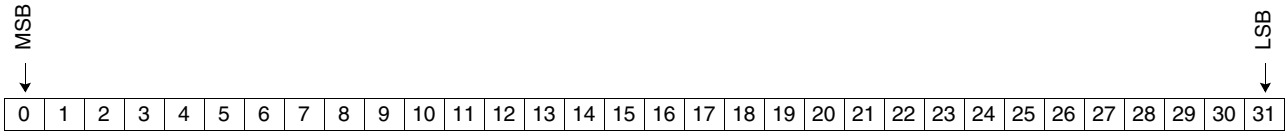
Part Number	Description
IBM3229P2035	IBM Packet Routing Switch Serial Interface Converter

1.4 Conventions and Notation

In this document, with the exception of Section 5, Data-Aligned Synchronous Link (DASL), bit notation is non-IBM, meaning that bits and bytes are numbered in descending order from left to right. Thus, for a four-byte word, bit 31 is the most significant bit (MSB) and bit 0 is the least significant bit (LSB).



In Section 5, Data-Aligned Synchronous Link (DASL), standard IBM notation is used, meaning that bits and bytes are numbered in ascending order from left to right. Thus, for a four-byte word, bit 0 is the MSB and bit 31 is the LSB.



DASL uses a big-endian architecture, that is, the left-most bytes (those with a lower address) are most significant. (In little-endian architectures, the right-most bytes are most significant.)

Notation for bit encoding is as follows:

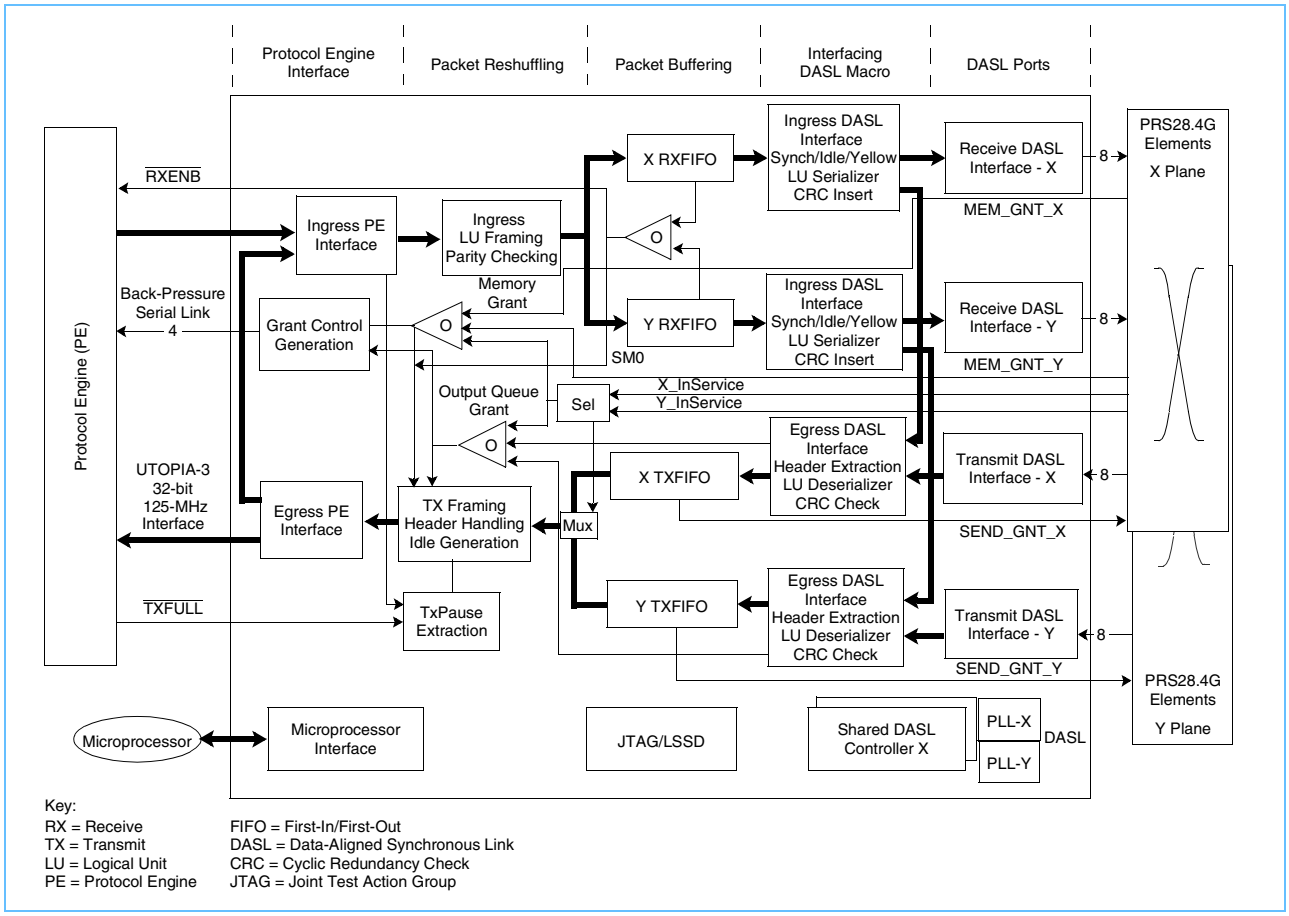
- Hexadecimal values are preceded by x and enclosed in single quotation marks. For example: x‘0B00’.
- Binary values appear in single quotation marks. For example: ‘1010’.

The use of overbars, for example $\overline{\text{DDEL\_OUT}}$, designates signals that are active low.

2. Converter Ingress and Egress Data Flow

The ingress block is the receive path between the Protocol Engine (PE) and the rest of the IBM Packet Routing Switch Serial Interface Converter logic. The egress block is the transmit path between the converter transmit logic and the PE. This section provides an overview of the functions implemented in the converter ingress and egress data flows. Some functions are duplicated to support two IBM Packet Routing Switch PRS28.4G planes (see Figure 2-1).

Figure 2-1. Converter Data Flow



2.1 Ingress Data Flow

2.1.1 Ingress PE Interface

The converter connects to the PE via a 32-bit bus. Ingress data packets are simultaneously routed to path X and path Y. Idle packets are inserted in the word stream when there is no data to transfer and are used to maintain a synchronous packet operation in the ingress PE interface. Idle packets are identified by a bit in the packet qualifier byte. A Receive Start of Packet (RXSOP) signal synchronized with the data packet is used to delineate packets.

Combined with the RXPRTY signal issued from the PE, the ingress interface checks the parity coherency on each incoming 32-bit word on RXDATA. A specific bit in the configuration table registers can be set so that each parity error issued from the parity checker is reported.

RXPRTY_error assertion, controlled by the configuration table, indicates that the cell currently pushed into the ingress reshuffling buffer will be optionally ignored and will not be sent to the ingress first-in/first-out (FIFO). Cells that are pushed into the ingress receive FIFOs (X/Y RXFIFOs) are always error-free and can be processed by the data flow.

2.1.2 Ingress Packet Reshuffling

The ingress logical unit (LU) framing block maps incoming data packets into the switch LUs by moving the five bytes (the packet qualifier and the bit map fields) selected from the configuration register into the master LU, which becomes the switch header information field. The framing block also extracts the in-band flow control (IBFC) information, discards idle packets, and performs parity checking on the switch header.

2.1.3 Ingress Receive FIFO

The ingress RXFIFOs provide packet synchronization between the 50- to 125-MHz PE interface and the 110- to 125-MHz switch core interface.

2.1.4 Ingress DASL Interface

The Ingress DASL Interface (IDI) sends packets continuously. Synchronization packets are sent during the DASL synchronization sequence. Data or idle packets are sent once the data mode is active. Yellow packets are requested through the configuration table. When the LU serializer is filled with a yellow packet, the incoming data packet is buffered while the yellow packet is sent. When there is no data packet to be transmitted to the switch core, the IDI inserts an idle packet, computes the inter idle Cyclic Redundancy Check (CRC) for each LU, and inserts it as the last byte of each LU.

2.1.5 DASL Port Serializer

The IDI feeds the DASL port serializer with packets compatible with the switch LU format. (The 16- to 20-byte LU width is set in the configuration register.) The DASL port serializer performs a multibit serialization for each LU. Each serial DASL interface line represents a nibble of the LU so that there are two data-aligned synchronous links per byte. The converter provides a total of eight serial links per port (one for each 4-bit nibble) representing a 32-bit wide word.

2.2 Egress Data Flow

2.2.1 DASL Port Deserializer

The egress DASL performs 32-bit deserialization on incoming data and builds LUs for the Egress DASL Interface (EDI). It continuously monitors signal quality on the incoming high-speed serial link and performs continuous bit-positioning adjustment on the incoming data to maintain synchronization.

2.2.2 Egress DASL Interface

The DASL's receive data indicator line triggers the LU deserializer logic block, which receives a continuous stream of packets. Packet length is programmable from 64 to 80 bytes and is mapped on four-byte word boundaries. Therefore, a new packet is received from the DASL every 16 to 20 cycles.

The LU deserializer extracts the switch packet header from the master LU to determine packet type (idle or data) and priority. Idle packets are discarded. Data packets are forwarded (in LU format) to the egress buffer interface. The LU deserializer checks the LU CRC after each idle cell, the parity on the switch header, and the type of packet. When an error or yellow packet is detected, and the checker is enabled, the corresponding converter interrupt line is asserted.

2.2.3 Egress Transmit FIFO

The egress FIFO interface ignores any idle packets issued from the switch. Only data packets are pushed into the transmit FIFOs (TXFIFOs) for a further word-formatting packet operation. The TXFIFOs provide packet synchronization between the 110- to 125-MHz converter and the 50- to 110-MHz Protocol Engine.

2.2.4 Egress Path Selection

The egress path selection multiplexes packets coming from the X and Y paths to the egress PE interface bus. The data is selected from the path in service through two interface lines (X_InService and Y_InService) received from the switch core.

2.2.5 Egress Transmit Framing

The packet formatter translates custom-formatted packet LUs, reversing the operation performed in the ingress path. Header byte swapping moves the header bytes back to their original position. The converter simultaneously takes and moves the latest available output queue grant (OQG) flow control data from the EDI into the corresponding byte positions that were used for output port addressing in the ingress path. The most recent shared memory grant and the OQG priority (related to the bit map field's OQG) are both stored in the packet qualifier byte that is sent to the PE so it can perform virtual output queuing scheduling for the ingress packets. Idle packets are also generated and sent to the PE in order to maintain continuous flow control information.

2.2.6 Egress PE Interface

The egress PE interface connects the converter to the PE's 32-bit bus. Data and idle packet transfer is controlled by egress transmit framing. The egress PE interface monitors the behavior of $\overline{\text{TXFULL}}$, controls $\overline{\text{TXENB}}$ accordingly, and generates the Transmit Start of Packet (TXSOP) signal to the PE. A parity bit covering a 32-bit word can be generated according to a dedicated bit in the configuration table registers.

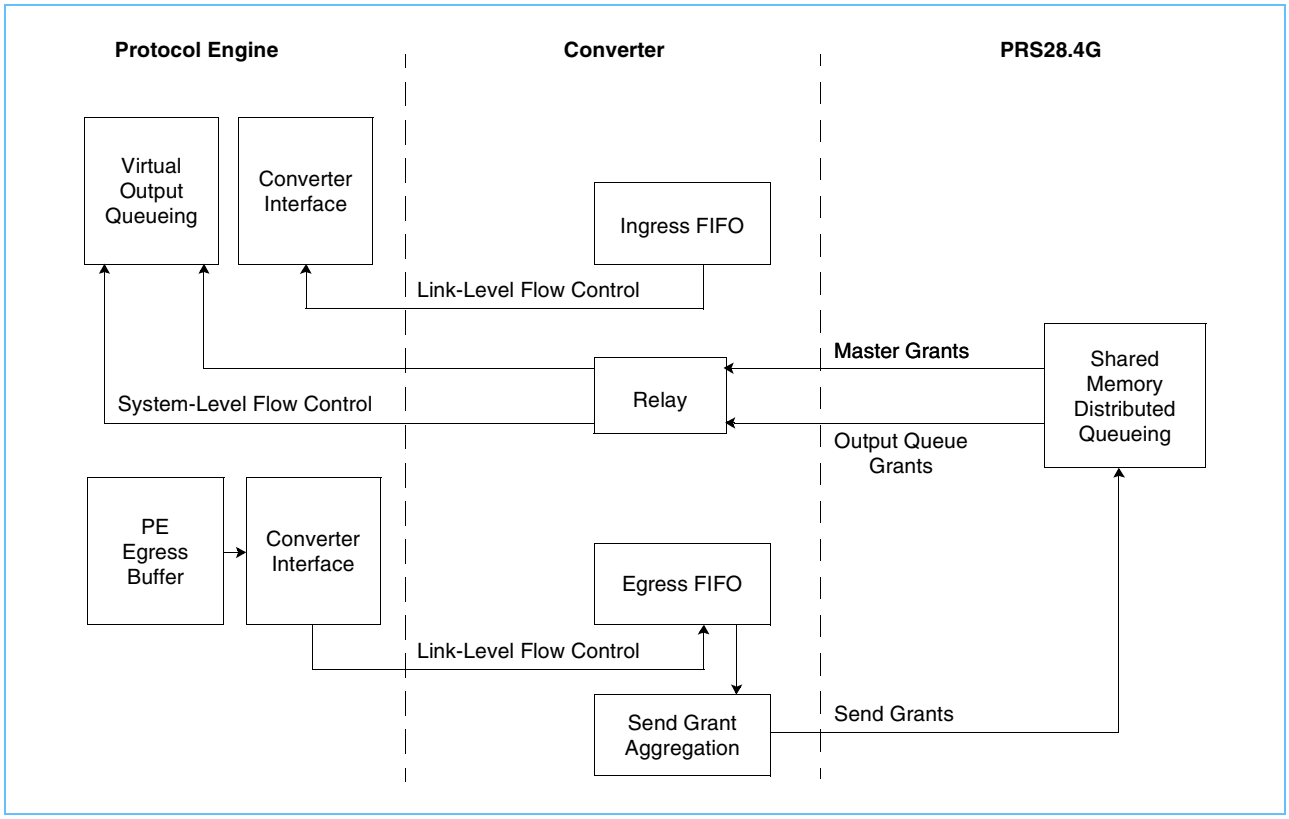
2.3 Converter Flow Control

The PRS28.4G is a shared output buffer switch. In the switch subsystem architecture, the input adapter provides a multiple input queuing structure with one queue per output adapter and per priority. From an architecture standpoint, this queuing structure is a virtual extension of the switch shared output queue and is generally known as virtual output queuing (VOQ).

From a queuing standpoint, the converter does not perform any VOQ; it simply provides a unique ingress FIFO queue and a unique egress FIFO queue. From a throughput standpoint, the converter is nonblocking with regard to the switch. Contrarily, the Protocol Engine (PE), which is attached to the switch through the converter, usually has a lower throughput capacity, thus providing a switch speedup factor at the system level.

Consequently, this architecture requires two levels of flow control: system-level flow control between the switch (multiple queuing structure) and the PE (VOQ structure), and link-level flow control between the converter and the PE. Additional flow control exists between the converter and the switch. Figure 2-2 is an overview of the two levels of flow control.

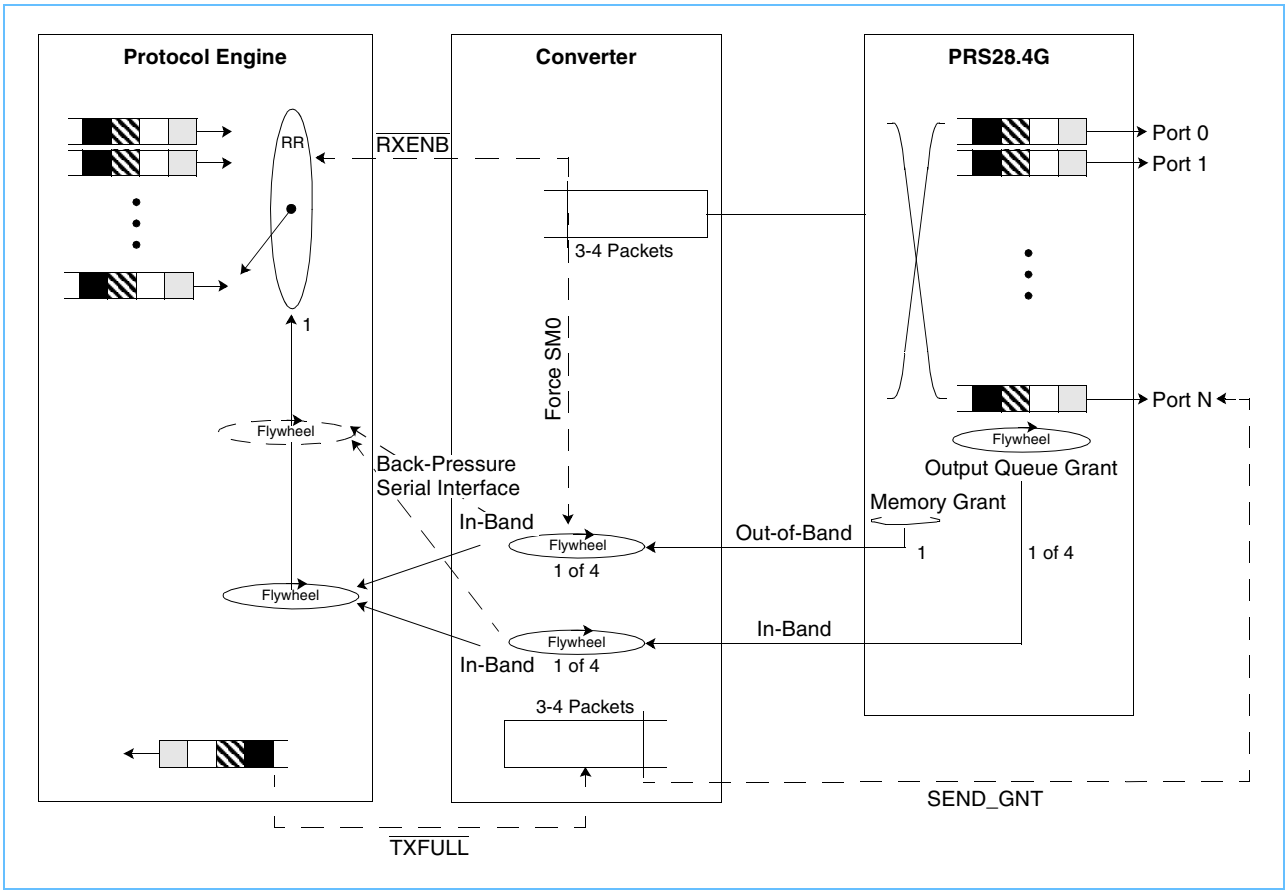
Figure 2-2. Flow Control Overview



2.3.1 System-Level Flow Control

System-level flow control regulates the ingress traffic from the PE to the switch (see Figure 2-3).

Figure 2-3. System-Level Flow Control



System-level flow control is the flow control issued by the switch towards the VOQ entity. The latter is usually implemented in the PE, which is attached to the switch by means of the converter. System-level flow control information is composed of switch shared memory occupancy information and switch output queue occupancy information. The converter does not process this information, but transparently relays it to the PE.

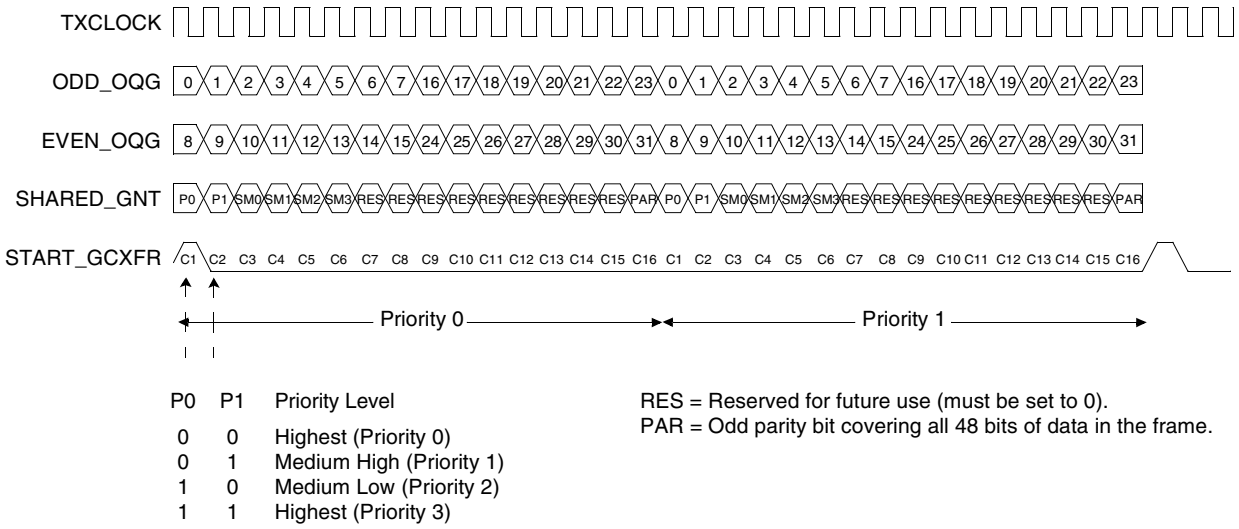
The converter provides two relay modes: one consists of mapping the flow control into the header of the egress packets, the other consists of mapping the flow control onto a dedicated bus—the selective back-pressure bus. Note that the two modes are mutually exclusive.

2.3.1.1 Out-of-Band Flow Control (OBFC)

Flow control information from the switch is mapped on the back-pressure interface—a dedicated serial bus made up of four signals. The per-port grant and shared memory grant information from the switch plane in service are combined and passed via the back-pressure interface to the attached protocol engine. Back-pressure signaling consists of shared memory and per-port back-pressure information for up to four priority levels. The four shared memory priorities are always reported, while the number of per-port priorities reported is a function of the converter configuration in either the 16- or 32-port mode.

An example of the back-pressure bus timing is given in Figure 2-4. In this example, the converter is configured for two priorities only.

Figure 2-4. Timing of OBFC Grant Control Signaling



The framing of the back-pressure serial link is independent of the length of the LU; therefore, it repeats every 16 TXCLOCK (UTXCLK) cycles, providing the latest information about the output queue grant and memory grant status.

2.3.1.2 In-Band Flow Control (IBFC)

Flow control information from the switch is mapped into the header of the egress packets. In this mode, the converter generates a continuous packet flow towards the PE, transmitting idle packets in the absence of any data traffic. This continuous packet flow constantly refreshes the flow control information in the PE.

Mapping in the Packet Header

- Bits 6 and 7 of the packet qualifier (PQ) encode the priority for which master grant information is relayed. The bit encoding is as follows:

  00 high priority
  01 medium-high priority
  10 medium-low priority
  11 low priority

- Bit 5 of the PQ is the shared memory grant (master grant) information:

  0 hold (grant off)
  1 grant on

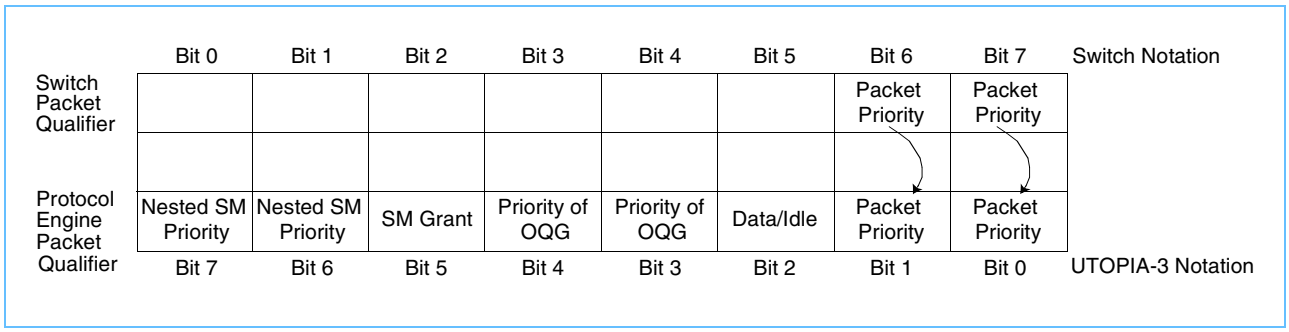
- Bits 3 and 4 of the PQ encode the priority for which output queue grant (OQG) information is relayed. The bit encoding is as follows:

  00 high priority
  01 medium-high priority
  10 medium-low priority
  11 low priority

The bit map bytes in the egress packets contain the OQG information. There are four bit map bytes for a 32 × 32 switch and two bit map bytes for a 16 × 16 switch.

The packet qualifier map in Figure 2-5 demonstrates the mapping of packet priorities from the switch packet qualifier byte into the PE packet qualifier. Because only one 2-bit packet priority can be transferred per byte, and there are up to four priority levels, four packets are required to fully refresh the priority information into the PE. With regard to latency, in the worst case of four priorities, up to four consecutive packets are necessary to provide the PE with a complete view of the switch queuing status.

Figure 2-5. Egress Data Packet Header



2.3.2 Link-Level Flow Control

Link-level flow control regulates the transfer of packets at the PE-converter interface. It allows the converter to stop transmission of packets from the PE when its ingress FIFO reaches a programmable threshold. Similarly, it allows the PE to stop transmission of packets from the converter when its buffering system becomes congested. In turn, this can trigger flow control from the converter to the switch.

Link-level flow control can use either the UTOPIA-3-like flow control signals or in-band procedures in which flow control information is conveyed in the packets transferred at the interface. As detailed hereafter, using an in-band scheme for the link-level flow control requires that the converter be configured in IBFC (system-level in-band flow control) mode.

2.3.2.1 Out-of-Band Link-Level Flow Control (OBLC)

PE to Converter Flow

When its ingress FIFO reaches the programmable almost full threshold, the converter requests the PE to stop packet transmission by means of the $\overline{\text{RXENB}}$ signal. When requested to stop data packet transmission, the PE can still transmit idle packets on the interface. $\overline{\text{RXENB}}$ operation is described in Section 3.2 , Functional Overview, on page 32.

Note: This flow control mechanism is rarely used in normal configuration in which the throughput of the PE is lower than the capacity of the converter-switch link capacity. This mechanism is used primarily when the PE throughput is higher than the converter-switch link capacity minus the rate of the generated yellow packets.

Converter to PE Flow

When the PE becomes congested, it can stop packet transmission from the converter by means of the $\overline{\text{TXFULL}}$/TXPAV signal. $\overline{\text{TXFULL}}$/TXPAV operation is described in Section 3.2.

Note: This flow control mechanism is generally used in normal configuration in which the throughput of the PE is lower than the capacity of the converter-switch link capacity. Controlling the egress flow in the converter can cause the egress FIFO to overflow, which triggers the SEND_GNT signal in the converter to stop packet transmission from the switch.

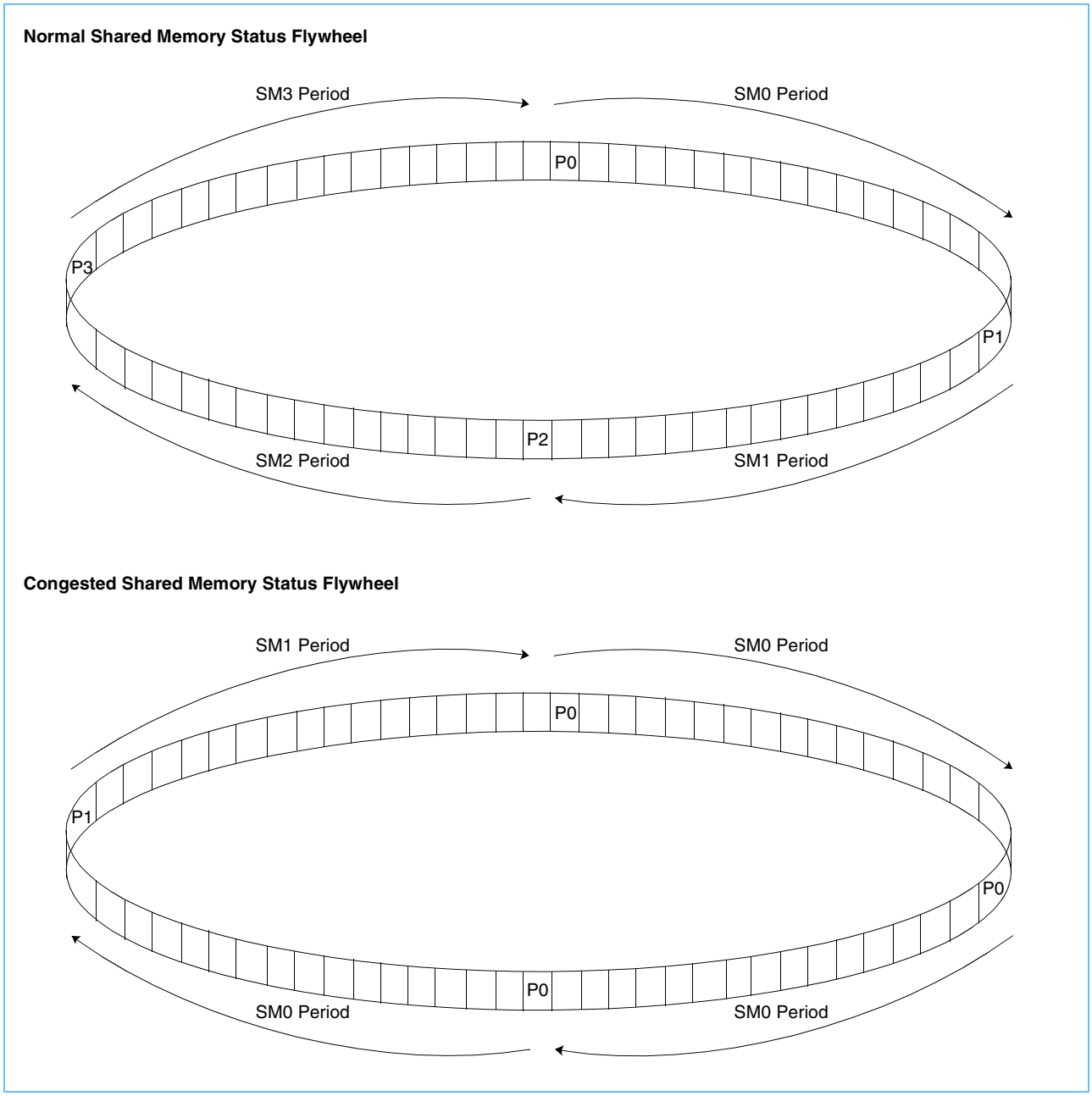
2.3.2.2 In-Band Link-Level Flow Control (IBLC)

PE to Converter Flow

Instead of using the UTOPIA-3 $\overline{\text{RXENB}}$ signal to perform link-level flow control, the converter can alter the content of the switch system-level flow control that it relays to the PE in the packet header. While congested, the converter reports a “grant-off” (grant value is ‘0’) for the master grant of the highest priority in the continuous egress packet flow (see Figure 2-6). This has two implications:

- The converter must be configured in the IBFC mode, and
- During the congestion phase, cyclical reporting of the master grants (from highest to lowest priority) is stopped and only the master grant of the highest priority is reported to the PE (forced “off”). When the congestion has passed, the converter resumes master grant cyclical reporting, reporting the first master grant that would have been reported if no congestion had occurred. In other words, the cyclical counter in the converter does not stop during the congestion phase. The cyclical reporting of the OQG is also maintained during congestion.

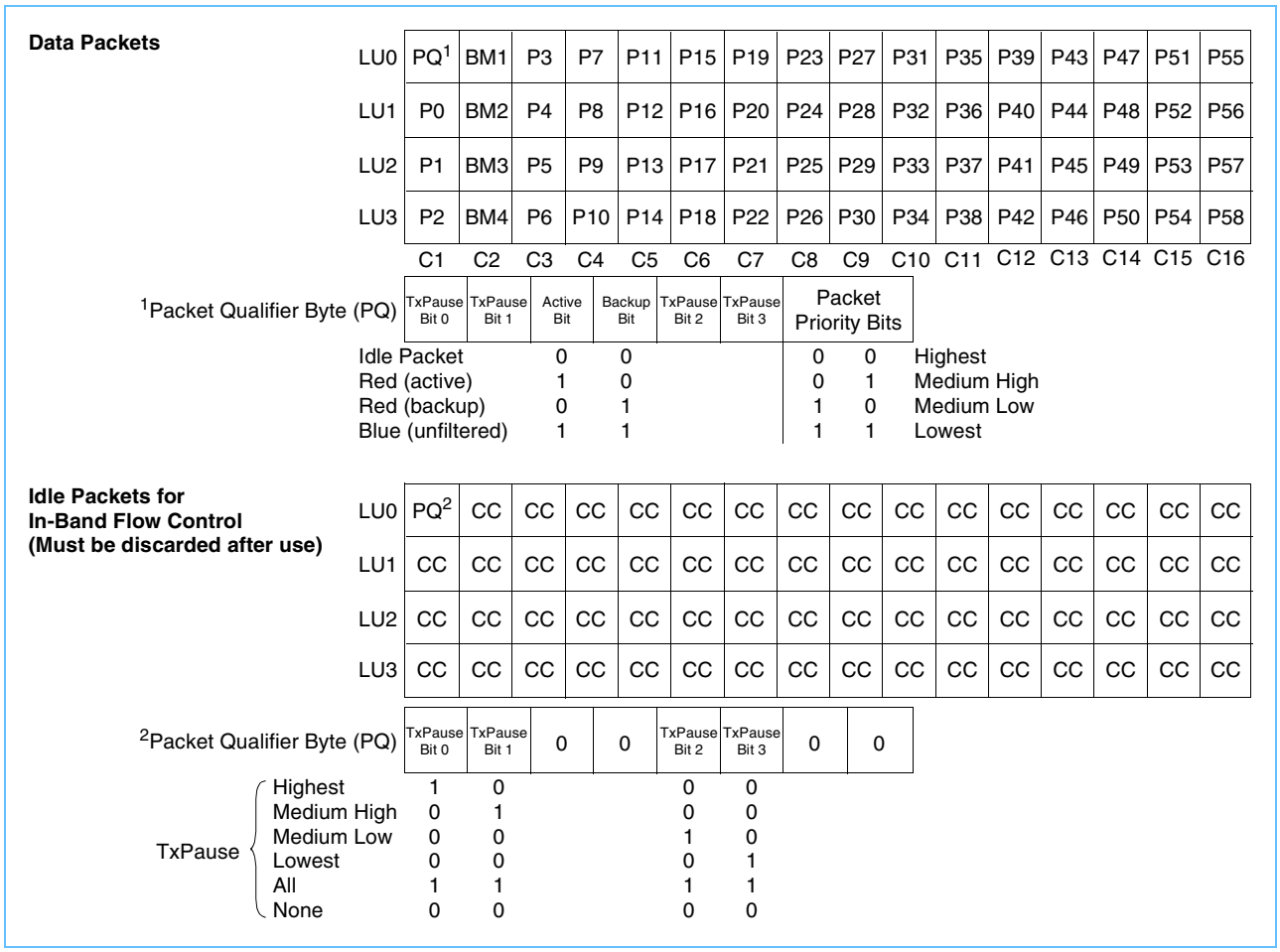
Figure 2-6. Shared Memory Flywheel Operation With Forced Memory 0



Converter to PE Flow

Instead of using the UTOPIA-3 $\overline{\text{TXFULL}}$/TXPAV signal, the PE can perform link-level flow control by setting the four TxPause bits defined in the packet qualifier of the ingress packets to '0' (see Figure 2-7). This in-band mechanism requires a continuous ingress packet flow for uninterrupted flow control; therefore, the PE must insert idle packets in the absence of any data packet. If any of the four TxPause bits are not at '0', the converter will not perform flow control.

Figure 2-7. Ingress TxPause Flow Control Insertion



2.3.3 Converter Configurations

Table 2-1 summarizes the various flow control configurations.

Table 2-1. Flow Control Configurations

Link-Level Flow Control	In-Band Flow Control (IBFC)[1]			Out-of-Band Flow Control (OBFC)		
	System-Level Flow Control	Link-Level Flow Control		System-Level Flow Control	Link-Level Flow Control	
		Protocol Engine	Converter		Protocol Engine	Converter
IBLC	Switch SMG and OQG mapped in packet header; cycling scheme	TxPause bits = '0000' in packet header	SMG of highest priority forced to '0'; cycling scheme disrupted for SMG	Not Applicable		
OBLC	Switch SMG and OQG mapped in packet header; cycling scheme	UTOPIA signal: TXFULL/TXPAV	UTOPIA signal: RXENB	Switch SMG and OQG mapped in dedicated back-pressure serial bus	UTOPIA signal: TXFULL/TXPAV	UTOPIA signal: RXENB

1. Continuous packet flow.

2.3.4 Latency

This section provides the latencies for the flow control procedures described above and for the data path. Figure 2-8 through Figure 2-15 must be taken into account in the system design (for example, threshold setting, etc.).

2.3.4.1 System-Level Flow Control

In-Band Flow Control (IBFC)

Figure 2-8. IBFC Output Queue Grant Latency

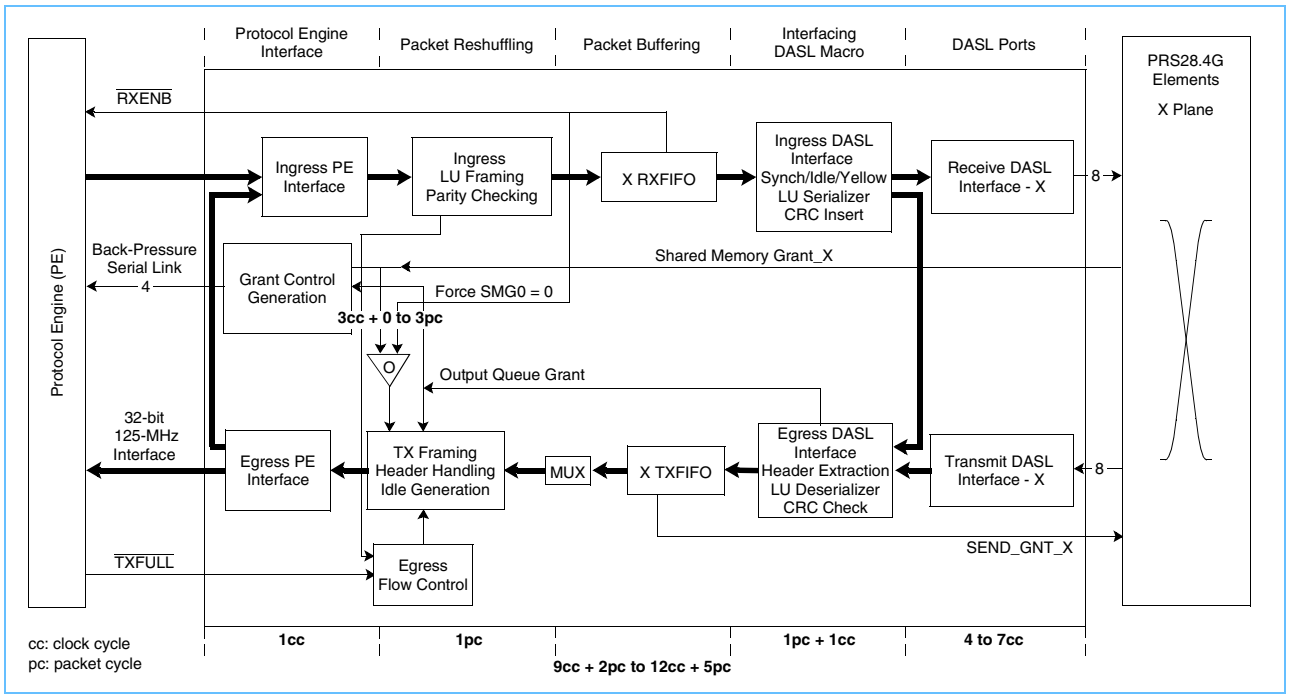
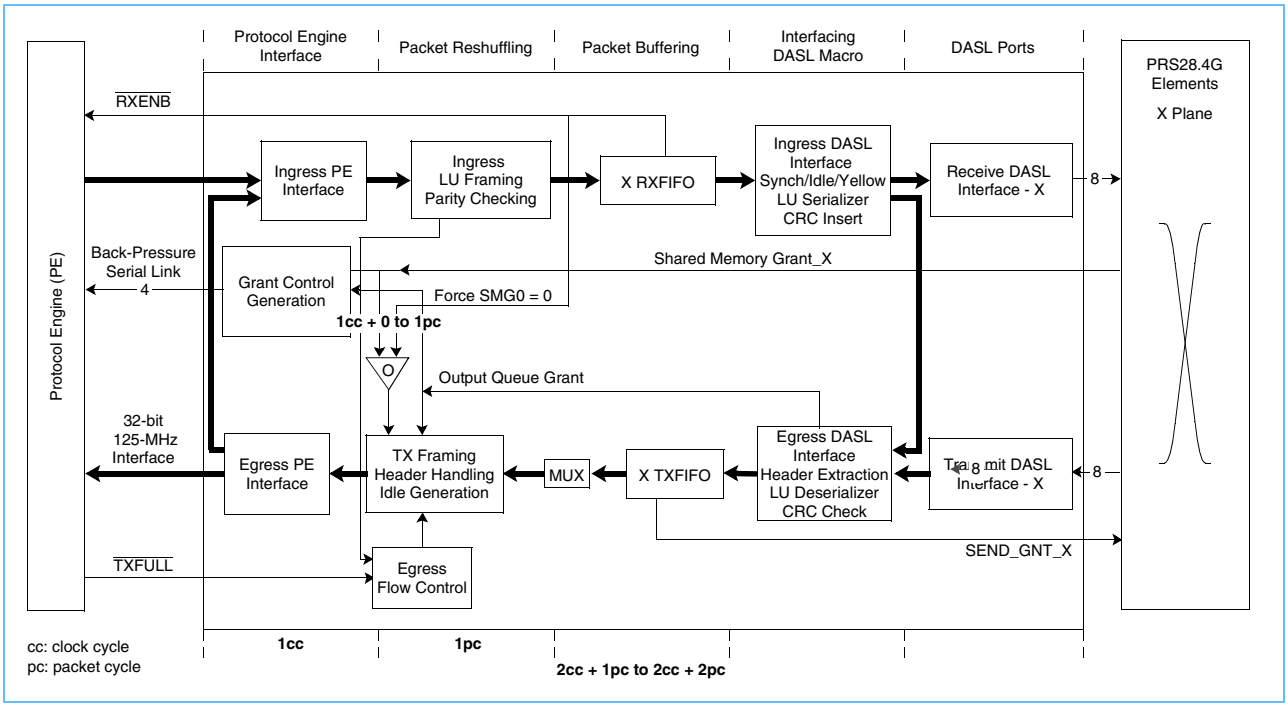


Figure 2-9. IBFC Memory Grant Latency



Out-of-Band Flow Control (OBFC)

Figure 2-10. OBFC Output Queue Grant Latency

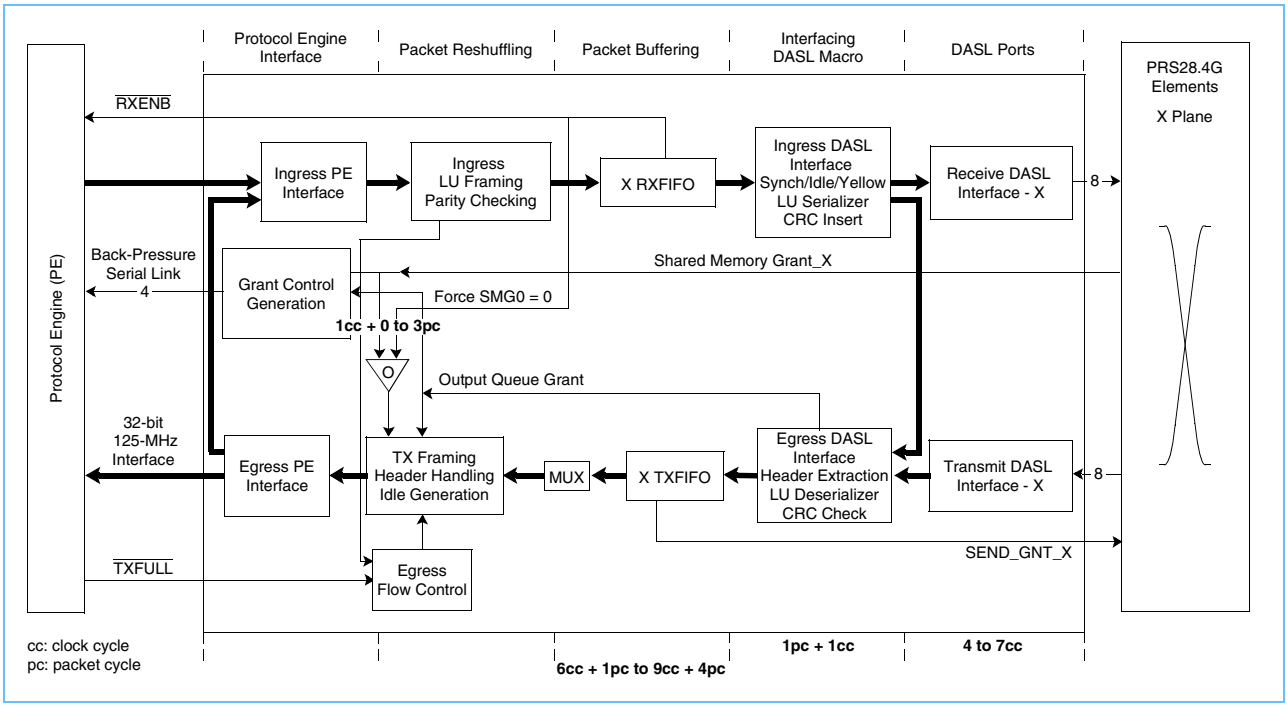
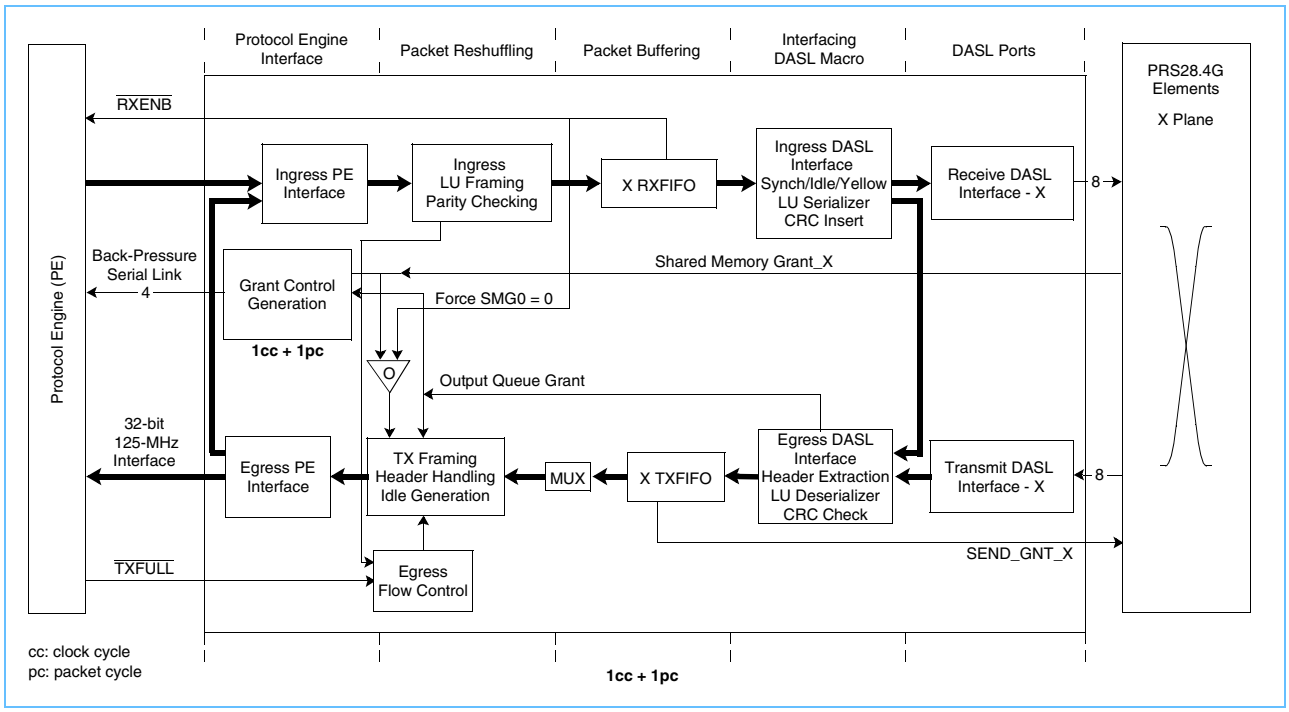


Figure 2-11. OBFC Memory Grant Latency



2.3.4.2 Link-Level Flow Control

In-Band Link-Level Flow Control (IBLC)

Figure 2-12. TxPause Latency

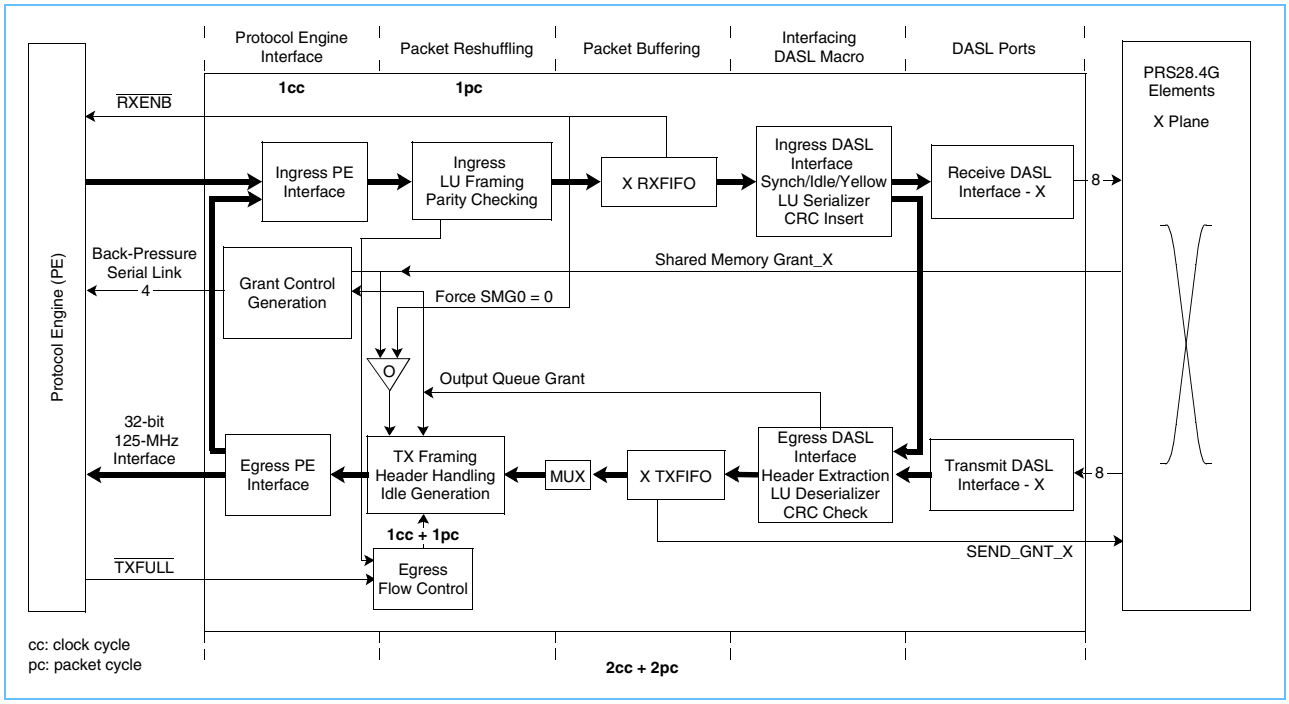
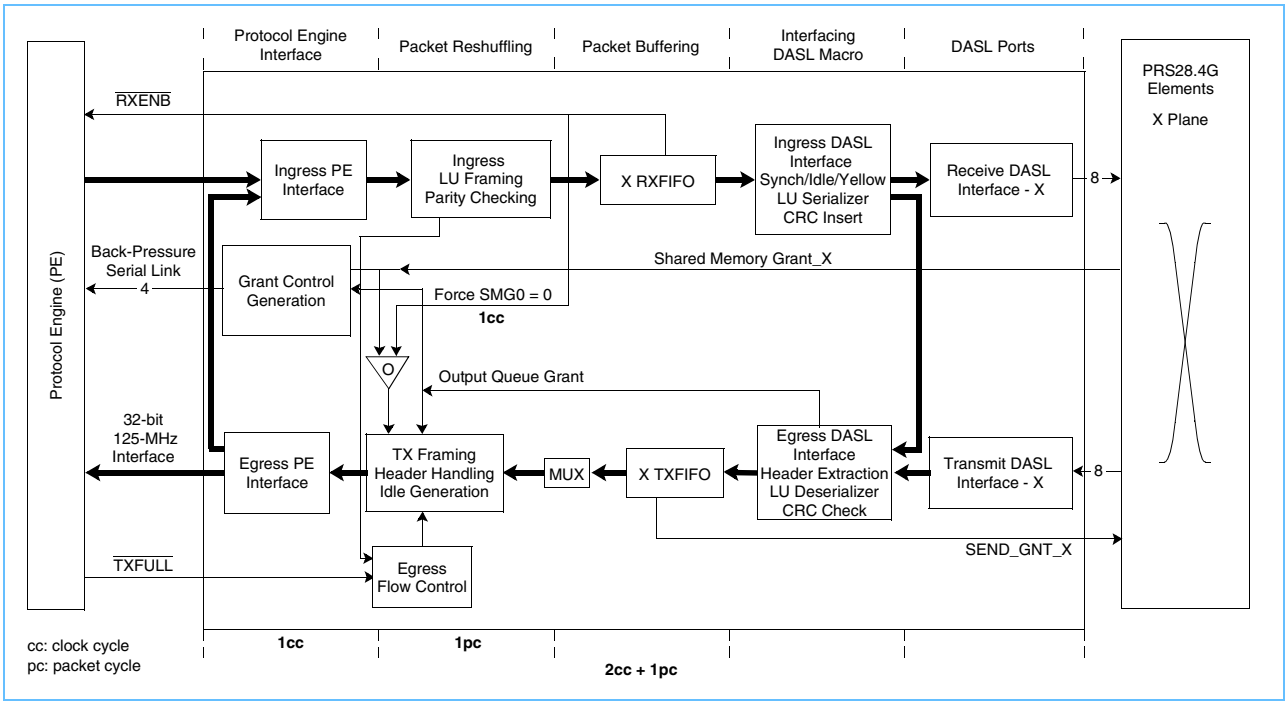


Figure 2-13. Force Shared Memory 0 Latency



Out-of-Band Link-Level Flow Control (OBLC)

See Section 3.2 , Functional Overview, on page 32 for a discussion of the UTOPIA-3-like interface timing.

2.3.4.3 Data Path

Figure 2-14. Ingress Data Latency

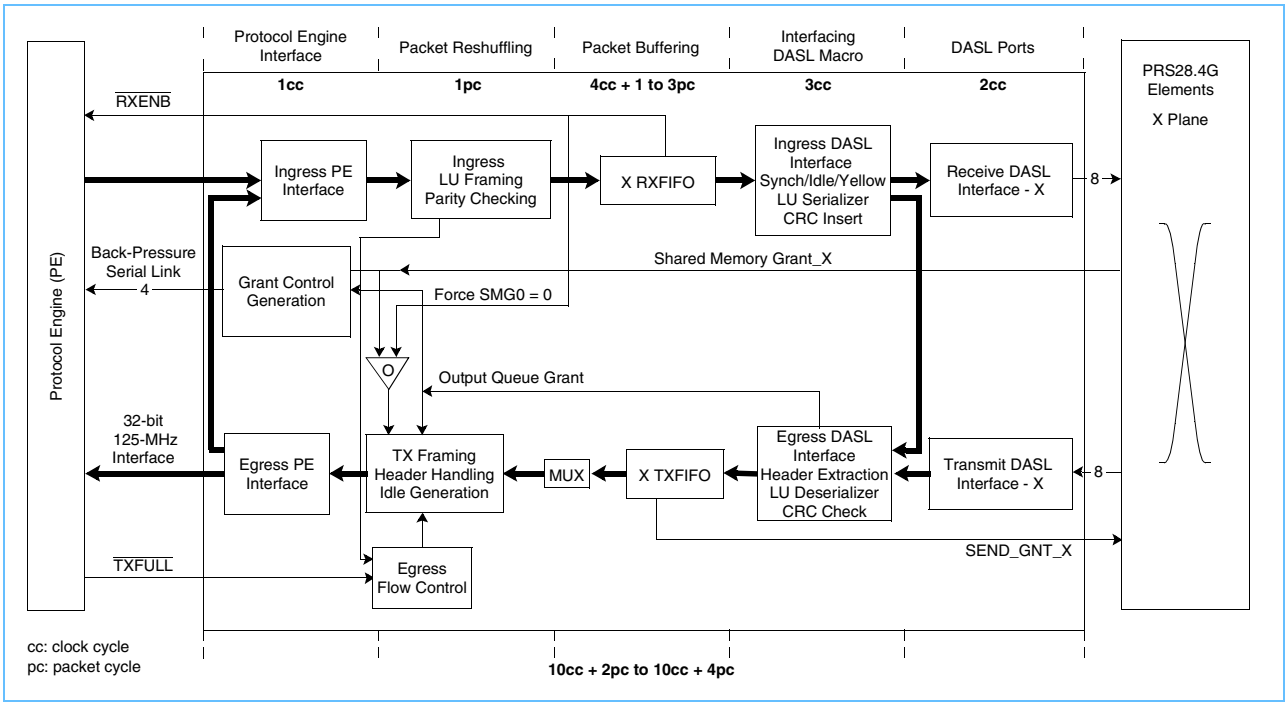
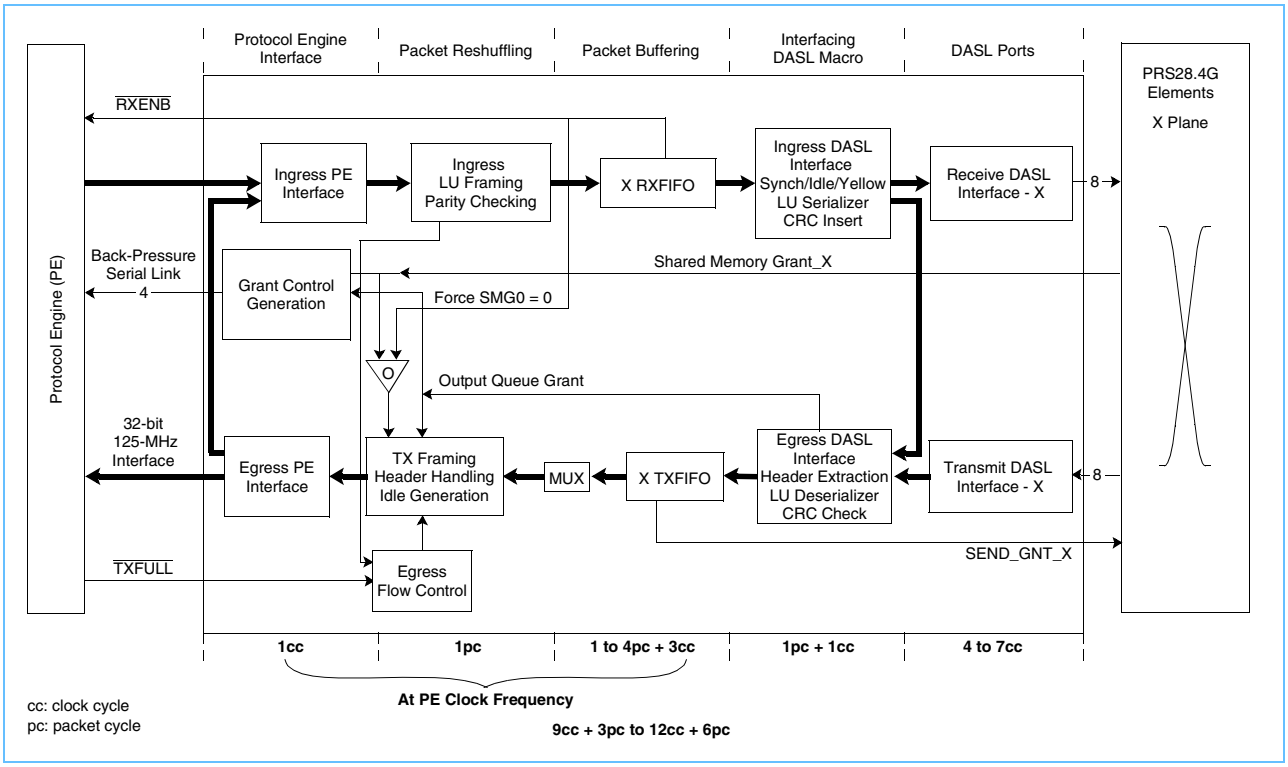


Figure 2-15. Egress Data Latency



2.4 Switch Flow Control

2.4.1 Latency

The latency within the PRS28.4G is:

Minimum: 3.4 LU size
Maximum: 4.6 LU size

Latency is measured from the LU first byte in to the LU first byte out. The latency figures above include both the DASL receive (RX) and transmit (TX) latencies.

The total latency of the switch port grant and memory grant flow control loops is the minimum/maximum across all possible phase relationships of input and output packet boundaries. The “loop” includes the following steps:

1. Updating the switch port fill
2. Updating the switch memory fill
3. Comparing the fill to a threshold
4. Resynchronizing to a grant coding scheme
5. Propagating grants to the attached device
6. Propagating a packet to the switch

Once the packet is in the switch core, the average latency delay (not including the DASL latency) is:

- Once a packet is in the input controller and its arrival changes the memory grant information, the MEM_GNT[3:0] pins are updated in [±1 LU Size] + [±4 Byte Clocks].
- Once a packet is in the input controller and its arrival changes the OQG information, the in-band OQG information appears in [±2 LU Size] + [±NbOfPriorities × LU Size].

DASL latency adds 4- to 7-byte clock cycles on ingress and a 2-byte clock cycle on egress.

The switch output port scheduling is not packet synchronized, so the output ports do not send the Transmit Start-of-Packet (TXSOP) signal at the same time. The TXSOP signals are shifted by one clock cycle. The output ports do not send the OQG information for the same priority at the same time, either. The output ports operate independently.

If an entering packet changes a grant status, then it takes at least *P* clock cycles (*P* ranging from 1 to 16) to align the output packet boundary, and may require the entry of another four packets (if using four priorities) before a packet carrying the priority of the updated grant enters. At the switch output port, the packet that forced the change triggers the start of the first packet that contains the updated grant. Therefore, the latency between a queue threshold being exceeded and the OQG information for that queue being sent out on all packets for all output ports is:

Minimum: $P + 16$
Maximum: $P + 64$

2.4.2 Threshold Setting

The shared memory thresholds within the switch must be set to low sharing and, consequently, the output queue thresholds must be set to their lowest thresholds (that is, priority 3 set to 16 packets, priority 2 set to 32 packets, priority 1 set to 48 packets, and priority 0 set to 64 packets).

The PRS28.4G Shared Memory Threshold Registers 0 and 1 must be set according to the complete flow control loop: Converter + Protocol Engine + Switch Flywheel.

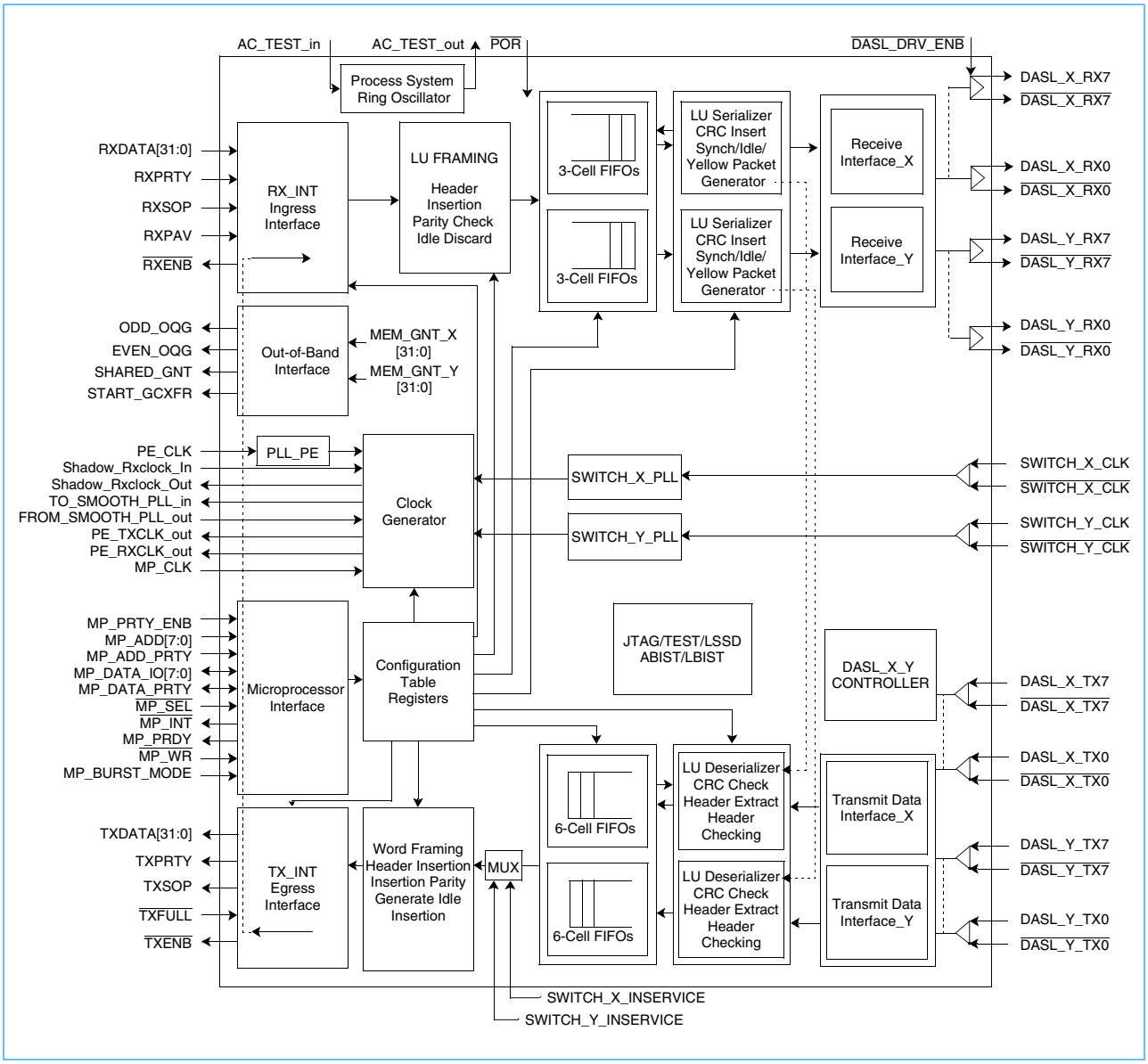
2.4.3 Flow Control Violation

For operation with the converter, the switch flow control check, bit 10 of the PRS28.4G Mode Register, must be disabled.

3. Functional Description

This section describes each functional block (see Figure 3-1) of the IBM Packet Routing Switch Serial Interface Converter (the converter). The description is by layer and covers both the ingress and the egress functions because, in general, they are completely symmetrical.

Figure 3-1. Converter Functional Block Diagram



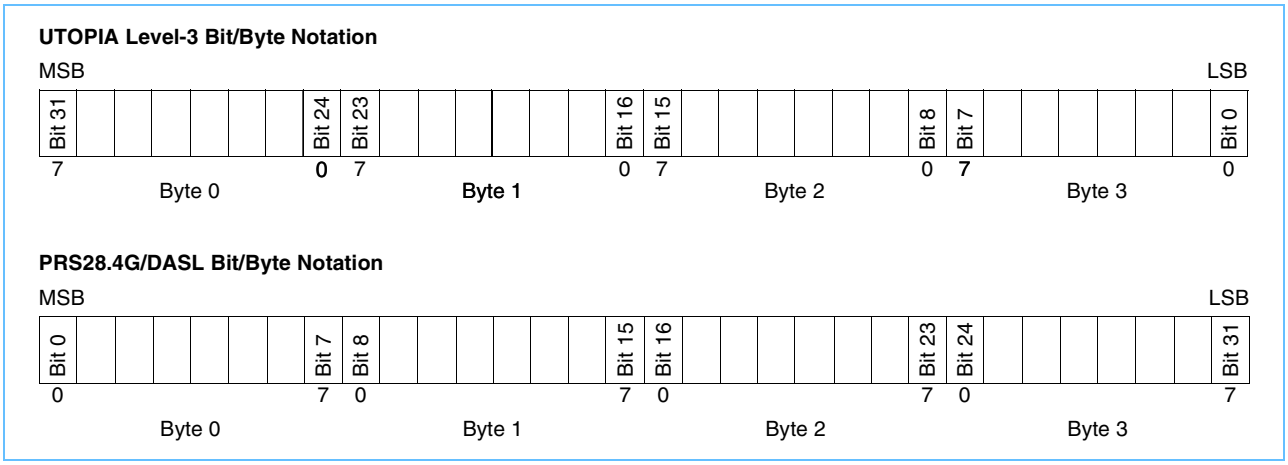
The ingress block is the receive path between the Protocol Engine (PE) and the rest of the converter logic. The egress block is the transmit path between the converter transmit logic and the PE.

The timing on the UTOPIA-3 interface is the same for out-of-band flow control (OBFC) and for in-band flow control (IBFC) modes. When operating in IBFC mode, the UTOPIA-3 flow control signals ($\overline{\text{RXENB}}$ at ingress and $\overline{\text{TXFULL}}$ at egress) are not normally used because the packet header carries all of the required information. However, if the PE performs OBFC, UTOPIA-3 signals can be used for performing the link-level flow control. In IBFC, idle packets flow through the interface to maintain a continuous stream of flow control information.

3.1 Data Interface Between the Converter and the Protocol Engine

UTOPIA-3 bit/byte notation is used throughout the PE interface description. After byte formatting (which reshuffles the byte position to match the PRS28.4G DASL interface), the switch DASL bit/byte notation is used. See Figure 3-2.

Figure 3-2. Bit and Byte Notation



3.2 Functional Overview

The converter ingress and egress interfaces are consistent with a subset of the UTOPIA-3 specifications:

- Single physical layer (PHY) interface mode (connection between one converter and one protocol engine).
- Typical operating clock range is 100 to 111 MHz to match the switch clock rate (up to 111 MHz), but an interface clock rate as low as 50 MHz is supported.
- Only 32-bit data paths.
- Packet format is 64 to 80 bytes (programmed in the converter during configuration).
- Only packet-level handshake mode (use of signals RXPAV in receive path and TXPAV in transmit path).
- $\overline{\text{RXENB}}$ and $\overline{\text{TXENB}}$ signals cannot be used to perform flow control at an octet level, which is allowed in UTOPIA-2 specifications. Each packet transfer initiated in either the ingress or egress direction will continue to flow until the current packet transfer is completed, eliminating the ability to insert wait states during the current packet transfer.

- The assertion of the $\overline{\text{RXENB}}$ signal depends only on the ingress FIFO filling status and so may be asserted while the RXPAV signal is deasserted.
- Wait state insertion on the bus is only allowed between transmission of two different packets.
- All input and output signals are latch-bound, meaning that inputs are clocked directly into latches and outputs emerge directly from latches. Therefore, a device (either the PE or the converter) responds in not less than two clock cycles after the initiating signal is sent across the interface.
- All output signals are generated and all input signals are sampled on low-to-high clock transitions.
- All signals are active high, unless the signal name has an overbar ($\overline{\text{xxx}}$).

3.2.1 Ingress Interface

3.2.1.1 Bus Protocol

The ingress block is the receive path between the PE and the converter. The PE sends data to the converter according to the following protocol:

- The converter provides the receive clock signal, PE_RXCLK_OUT.
- The PE asserts the RXPAV signal when it is ready to send at least one complete packet on the bus.
- The converter asserts the $\overline{\text{RXENB}}$ signal when it is ready to receive at least one complete packet.
- Receive packet transfer can start once the PE detects $\overline{\text{RXENB}}$ asserted while asserting RXPAV.
- The assertion of the RXSOP signal during one clock cycle indicates the start of a receive packet transfer.
- RXDATA[31:0] is transferred on each low-to-high clock transition, and the first data word of the packet is transferred simultaneously with the RXSOP signal.
- The converter deasserts the $\overline{\text{RXENB}}$ signal two clock cycles before the end of the current packet transfer if it cannot accept an immediate transfer of the subsequent packet from the PE.

This protocol applies when a user wishes to use OBLC procedures. If IBLC is used, there is no need for using the $\overline{\text{RXENB}}$ and RXPAV signals because all of the flow control is performed in band (through the packet header). Also under IBFC, if there is no data packet to be sent by the PE, the PE inserts an idle packet that is then discarded by the converter.

Table 3-1. Ingress I/O Pin Descriptions

Pin Name	Type	Function
PE_RXCLK_OUT	Output	Receive Clock is issued from two clock domains: • At power-on reset (POR), it is connected to the microprocessor clock until the POR is completed. • After POR is completed, it is generated by either the smooth Phase-Locked Loop (PLL) clock out (derived from the Switch_X_PLL or Switch_Y_PLL configuration register) or by an externally provided clock (e.g., the 50- to125-MHz PE clock). The PE_RXCLK_OUT source is selected according to the programming of the "PE_RXCLK_OUT_source_I[1:0]" bits in the configuration table registers.
RXDATA[31:0]	Input	Receive Data is transferred from the PE to the converter on a 32-bit word basis. LSB RXDATA[0] MSB RXDATA[31]
RXPRTY	Input	Receive Data Parity bit is the odd parity bit over the 32 RXDATA bits. The parity check mode is enabled or disabled by the RXPRTY_enb_I bit in the configuration table registers.
RXPAV	Input (active high)	The PE asserts Receive Packet Available when at least one complete packet is ready to be transmitted on the bus. The signal remains asserted during the current packet transfer (packet-level handshake) and indicates, in the cycle following the last word of the current packet, if there is (RXPAV asserted) or is not (RXPAV deasserted) a new packet to transfer. RXPAV must be asserted when operating in IBFC mode.
RXSOP	Input (active high)	The PE asserts Receive Start of Packet for one clock cycle when it starts a packet transfer to indicate the packet's first 32-bit data word.
$\overline{\text{RXENB}}$	Output (active low)	The converter asserts Receive Enable to indicate its readiness to receive at least one complete packet. The signal remains asserted during the transfer of the current packet (packet-level handshake) and, two cycles before the end of the current packet transfer, indicates whether it is ($\overline{\text{RXENB}}$ asserted) or is not ($\overline{\text{RXENB}}$ deasserted) ready to receive a new complete packet. As this signal is pipelined, the PE will respond at least two clock cycles after the $\overline{\text{RXENB}}$ is asserted or deasserted. The behavior of $\overline{\text{RXENB}}$ depends on the value of the RxEnabMode bit of the Ingress_PE_Interface register.

3.2.1.2 Ingress Operation and Timing

Figure 3-3. Ingress Timing for $\overline{\text{RXENB}}$ Deasserted by Converter for One Clock Cycle
Ingress Operation for 64-Byte Packet Flow Control with the RxEnabMode Bit of the Ingress_PE_Interface Register at '0'

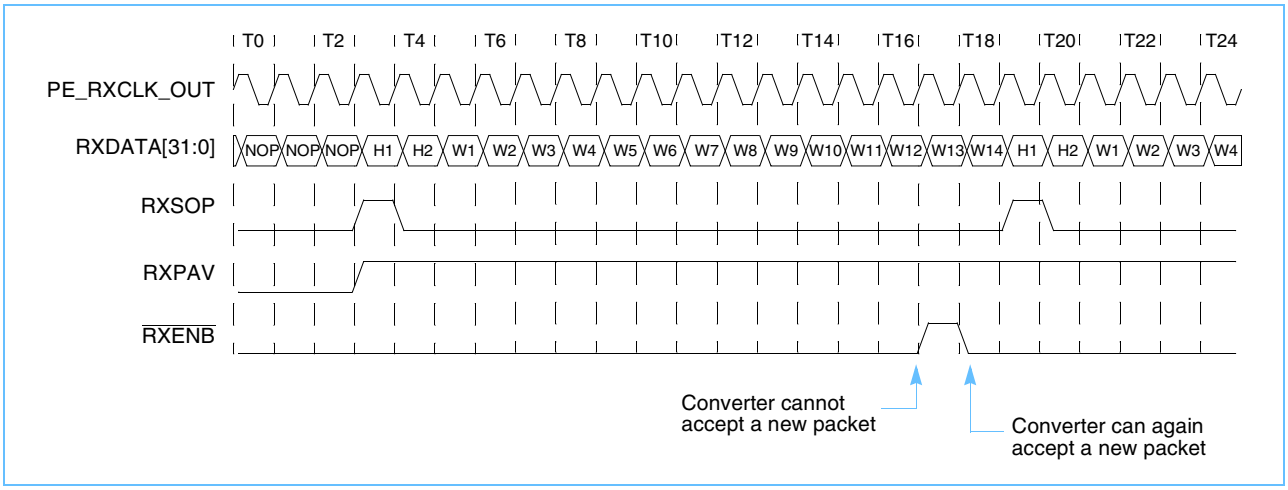


Figure 3-4. Ingress Timing for $\overline{RXENB}$ Deasserted by Converter When the RxEnabMode Bit of the Ingress_PE_Interface Register is High

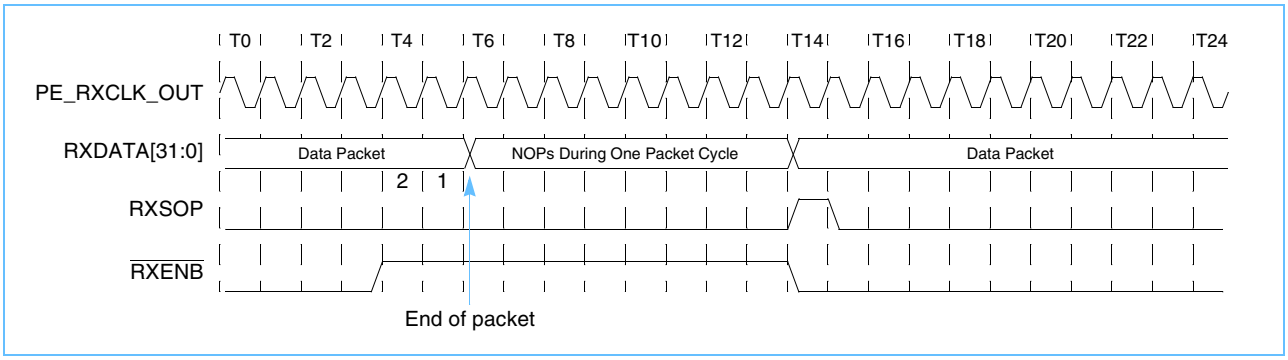


Figure 3-5. Ingress Timing for RXPAV Deasserted by Protocol Engine for One Clock Cycle
Ingress Operation for 64-Byte Packet Flow Control

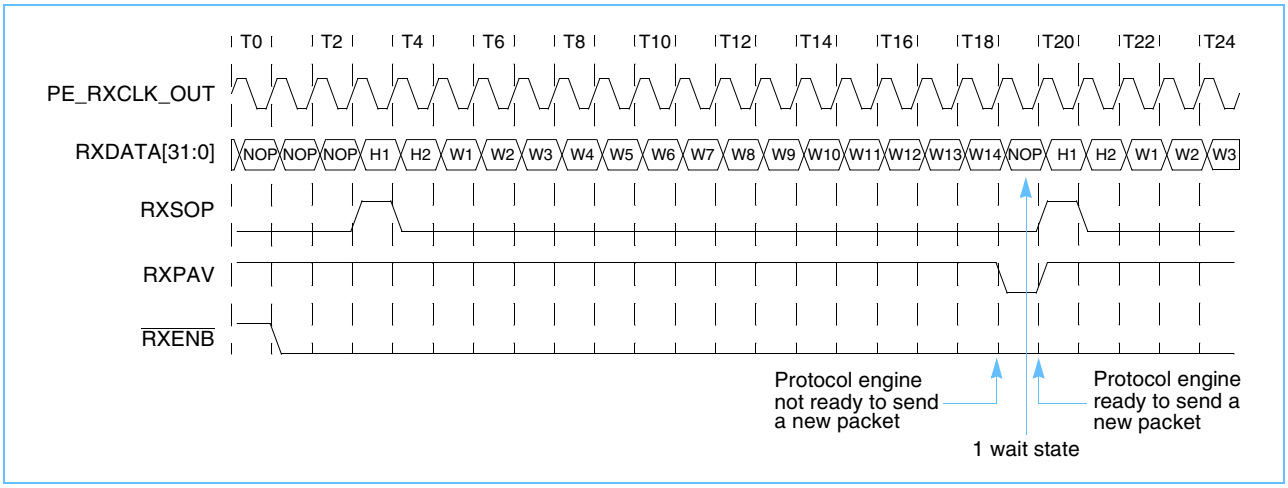


Figure 3-6. Ingress Timing for RXPAV Deasserted by Protocol Engine for Three Clock Cycles
Ingress Operation for 64-Byte Packet Flow Control

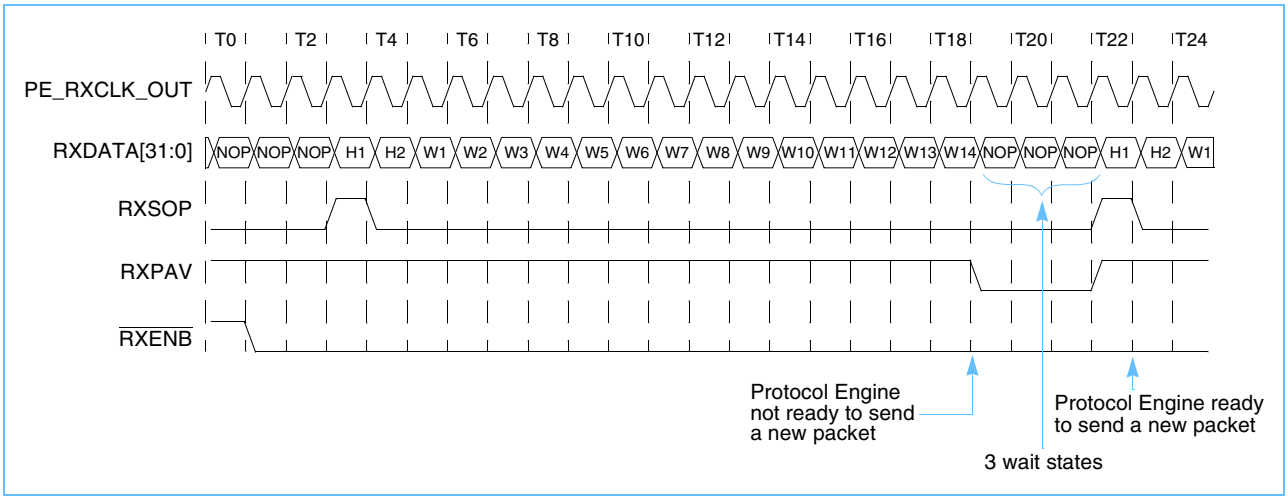
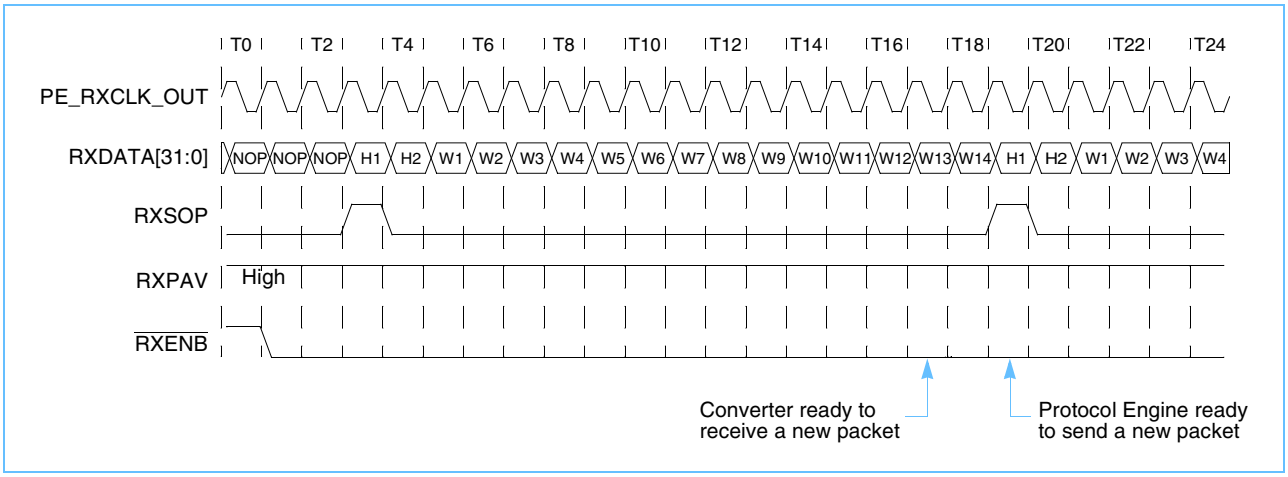


Figure 3-7. Ingress Timing for Back-to-Back Packets From Protocol Engine
Receive Operation for 64-Byte Back-to-Back Packets



3.2.2 Egress Interface

3.2.2.1 Bus Protocol

The egress block is the transmit path between the converter and the PE. The converter sends data to the PE according to the following protocol:

- The converter provides the transmit clock signal, PE_TXCLK_OUT.
- The PE asserts the TXPAV signal when it is ready to receive at least one packet from the converter.
- When the converter is ready to send at least one packet on the bus and the PE has asserted the TXPAV signal, the converter starts the transfer by simultaneously asserting the TXSOP and $\overline{\text{TXENB}}$ signals.
- TXDATA[31:0] is transferred on each low-to-high clock transition, and the first data word of the packet is transferred simultaneously with the TXSOP signal.
- The PE deasserts the TXPAV signal at least four cycles before the end of the current packet transfer if it cannot accept an immediate transfer of the subsequent packet from the converter.

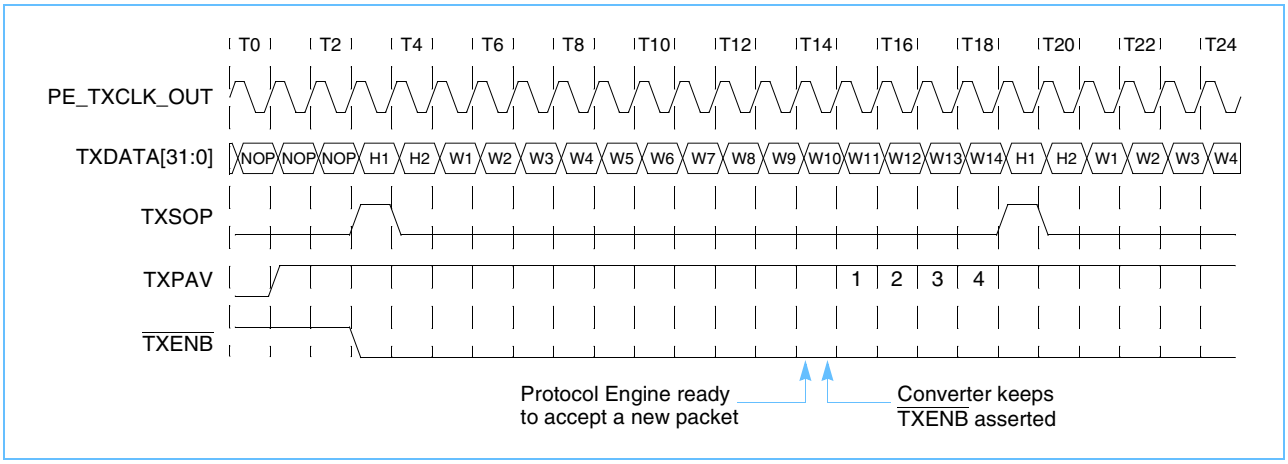
This protocol applies when a user wishes to use OBLC procedures. Under IBFC and IBLC operation, there is no need for using $\overline{\text{TXENB}}$/$\overline{\text{TXFULL}}$ (TXPAV) protocols because all of the flow control is performed in band (through the packet header). Also under IBFC, if there is no data packet to be sent by the converter, the converter inserts an idle packet that is then discarded by the PE.

Table 3-2. Egress I/O Pin Descriptions

Pin Name	Type	Function
PE_TXCLK_OUT	Output	Transmit Clock is issued from two clock domains: • At POR, it is connected to the microprocessor clock until the POR is completed. • After the POR is completed, it is generated by either the smooth PLL clock out (derived from the Switch_X_PLL or Switch_Y_PLL configuration register) or by an externally provided clock (e.g., the 50- to125-MHz PE clock). The PE_TXCLK_OUT source is selected according to the programming of the "PE_TXCLK_OUT_source_l[1:0]" bits in the configuration table registers.
TXDATA[31:0]	Output	Transmit Data is transferred from the converter to the PE on a 32-bit word basis. MSB TXDATA[31] LSB TXDATA[0]
TXPRTY	Output	Transmit Data Parity bit is the odd parity bit over the 32 TXDATA bits. The parity check mode is enabled and disabled by the TXPRTY_enb_l bit in the configuration table registers.
TXPAV $\overline{\text{TXFULL}}$	Input	These are two names for the same signal. The PE asserts Transmit Packet Available/$\overline{\text{TXFULL}}$ to an appropriately high level when it is ready to receive at least one complete packet. During a packet transfer, the PE has at least four cycles before the end of the current packet transfer to assert TXPAV if it can accept immediate transfer of the subsequent packet or to deassert TXPAV if it cannot. When the converter detects TXPAV deasserted, it may only transmit four more 32-bit data words to the PE. It is recommended that the PE keep TXPAV signal asserted until four cycles before the end of the packet transfer. TXPAV and $\overline{\text{TXFULL}}$ lines have the same timing. TXPAV asserted is equivalent to $\overline{\text{TXFULL}}$ deasserted.
TXSOP	Output	The converter asserts Transmit Start of Packet for one clock cycle when it starts a packet transfer to indicate the packet's first 32-bit data word.
$\overline{\text{TXENB}}$	Output	The converter asserts Transmit Enable to indicate that valid 32-bit data words are on the bus. When TXPAV is asserted during a packet transfer (at least four clock cycles before the end of the current packet transfer), the converter indicates, one clock cycle after the last word of the current packet, whether it is ($\overline{\text{TXENB}}$ asserted) or is not ($\overline{\text{TXENB}}$ deasserted) ready to send a new complete packet. When TXPAV is deasserted during a packet transfer (at least four clock cycles before the end of the current packet transfer), $\overline{\text{TXENB}}$ is deasserted four clock cycles afterwards to stop the transfer.

3.2.2.2 Egress Operation and Timing

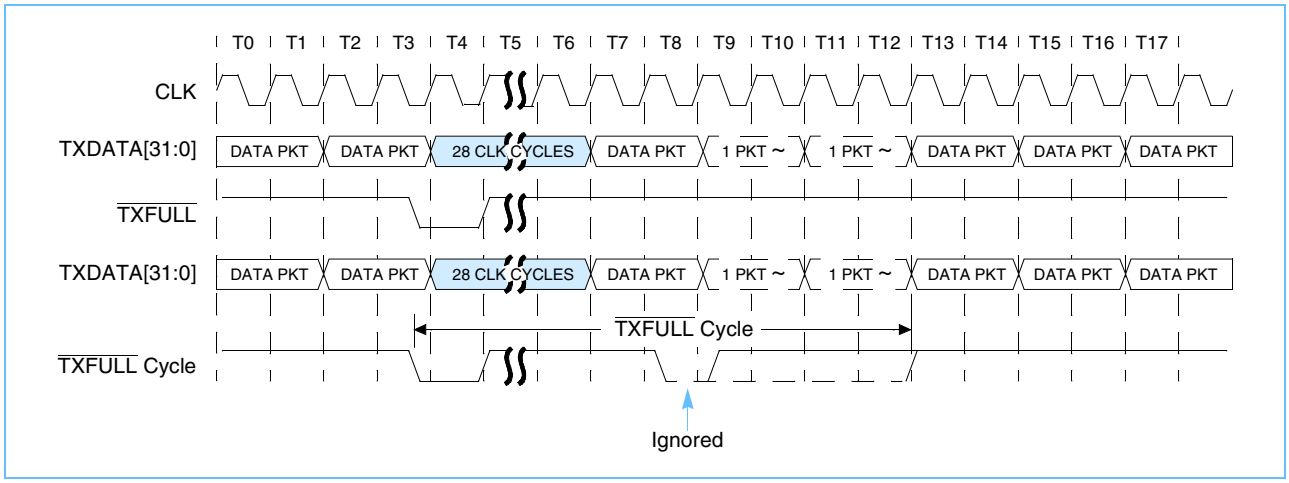
Figure 3-8. Egress Timing for Back-to-Back Packets
Transmit Operation for 64-Byte Back-to-Back Packet Transmission



3.2.3 $\overline{\text{TXFULL}}$ Timing Restriction

When the PE asserts $\overline{\text{TXFULL}}$ to stop the flow of packets, its effect is extended for 2 packet cycles from the end of the current packet. After the first packet following the deassertion of $\overline{\text{TXFULL}}$ by the PE, the converter inserts two empty slots of idle (no data) before traffic resumes. If the PE reasserts $\overline{\text{TXFULL}}$ upon the reception of the first packet during the $\overline{\text{TXFULL}}$ cycle, it will be ignored until the end of the complete cycle. See Figure 3-9.

Figure 3-9. $\overline{\text{TXFULL}}$ Timing Restriction



3.2.4 Timing for $\overline{\text{TXFULL}}$ Deasserted

If the PE deasserts $\overline{\text{TXFULL}}$ more than four clock cycles before the end of the current idle packet, the converter will transmit the packets after a wait of two packet cycles (see Figure 3-10). If the PE deasserts $\overline{\text{TXFULL}}$ less than four clock cycles before the end of the current idle packet, the converter will transmit the packets after a wait of three packet cycles (see Figure 3-11).

Figure 3-10. Timing for $\overline{\text{TXFULL}}$ Deasserted by PE More Than Four Clock Cycles Before the End of the Current Idle Packet

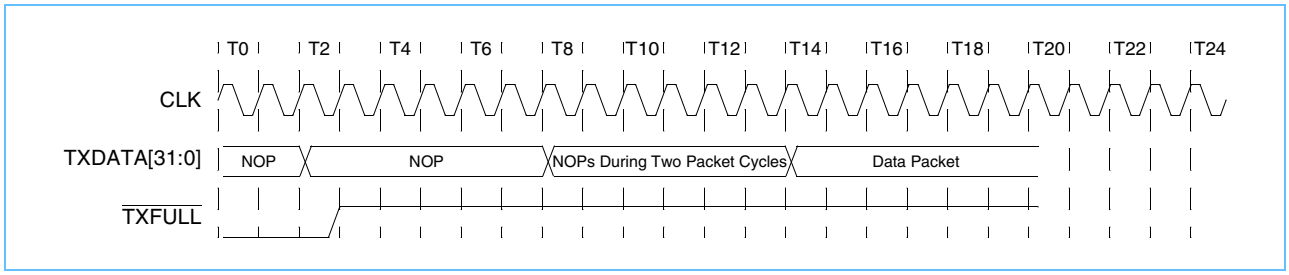
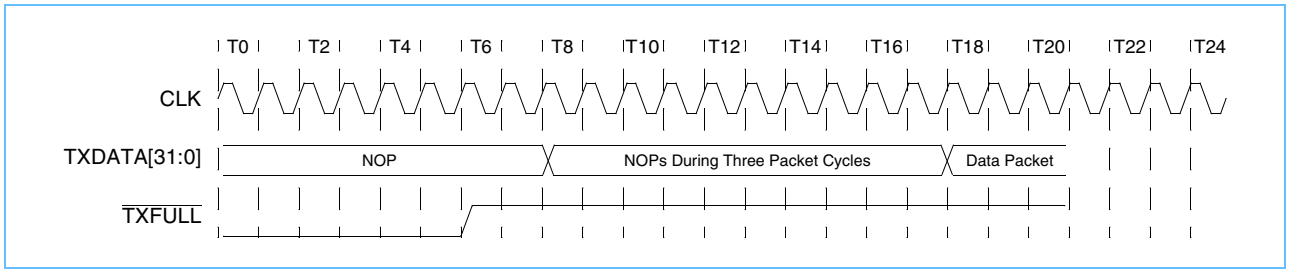


Figure 3-11. Timing for $\overline{TXFULL}$ Deasserted by PE Less Than Four Clock Cycles Before the End of the Current Idle Packet



3.3 Packet Reshuffling

3.3.1 Ingress Receive Logical Unit Framing

The ingress LU formatter is the interface between the PE interface logic and the ingress FIFO (RXFIFO) that translates various types of ingress packet formats into the switch LU format as defined in the converter configuration registers.

Data inputs are in a four-byte format. The ingress LU formatter extracts TxPause flow control information from the incoming packet qualifier byte. The incoming packet is comprised of 16 to 20 32-bit words. Packet reshuffling stores the packet in the switch format in four LUs that, when fully assembled, are forwarded to the RXFIFO.

The ingress LU formatter:

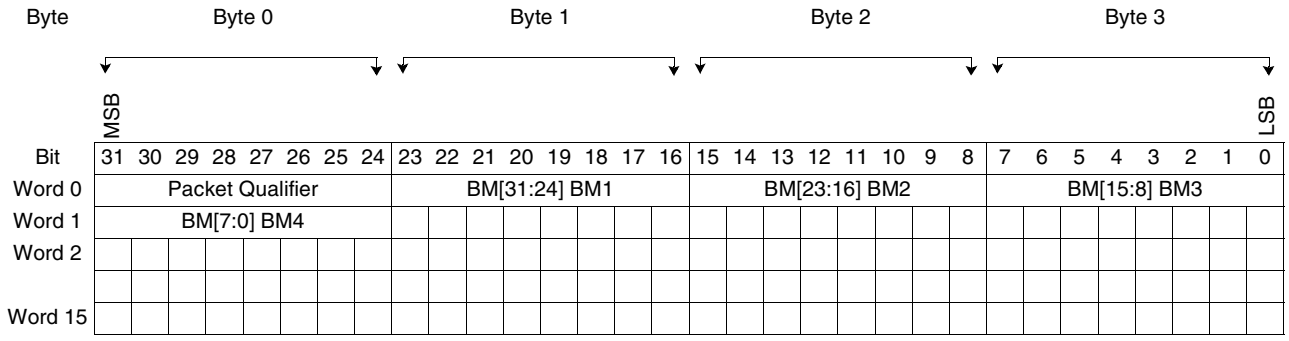
- Discards idle packets (IBFC mode only)
- Extracts send grant flow control information from the incoming packet qualifier byte (IBFC mode only)
- Modifies the packet qualifier byte into switch format and computes the associated parity (IBFC mode only)
- Changes the position of the bit map bytes in the packet header
- Recognizes any bus parity error reported on the PE interface signal RXPRTY_error
- Rejects the forwarding of a packet to the RXFIFOs in the event of any bus or header error (depending on the configuration register setting)
- Checks switch header parity bit in the packet qualifier byte (OBFC mode only)

3.3.1.1 Header Byte Reshuffling

The header bytes are moved according to the content of the “byte positioning in LU formatter” configuration fields. These allow any byte contained in the first four words of a packet to be moved to any other byte position in the master LU.

3.3.1.2 Input/Output Packet Format

The following tables highlight the position of the different information fields in an incoming packet. All bytes in the first four words of a packet can be repositioned in the switch header according to the formatter field in the configuration registers. The data source is based on a word/byte coordinate in a nibble. The first two bits correspond to the word selection; the last two bits correspond to the byte selection.



When the bit map (BM) field is defined for 32 bits and only 16 bits are used, only bits 31:16 of the bit map field are required to identify the 16 switch core ports. The other bits are considered to be part of the payload. The parity subfield of the packet qualifier field is calculated across the first three or five bytes (depending on the configuration).

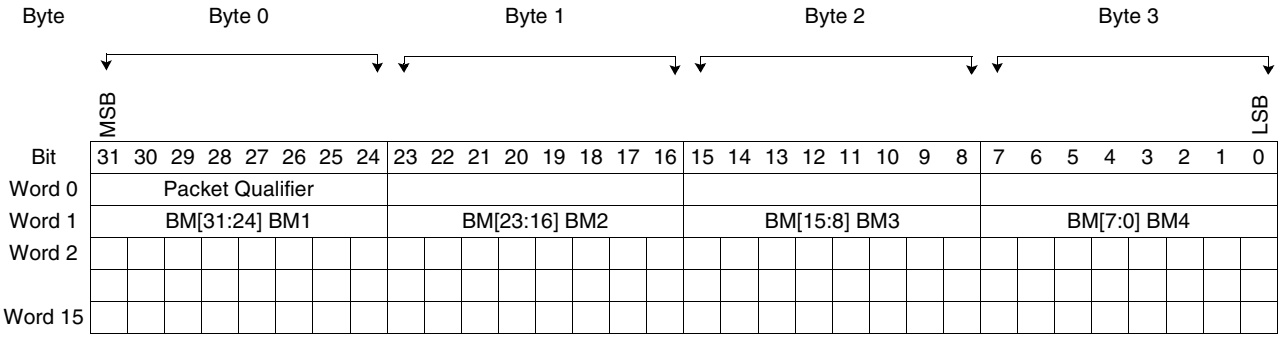
For example, with header bytes in sequence, the content of the bit-positioning registers (the PE_Common register for ingress and the Egress_PE_Interface register for egress) will be 0, 1, 2, 3, 1, as shown in the table below:

Header Bytes	Header Bytes in Incoming Packets		Content of the Bit-Positioning Register	Notes
Packet Qualifier	Word 0	Byte 0	0	
Bit Map 1	Word 0	Byte 1	1	
Bit Map 2	Word 0	Byte 2	2	
Bit Map 3	Word 0	Byte 3	3	
Bit Map 4	Word 1	Byte 0	1	1

1. This last index is not 4 because, during the second move operation, this byte was moved from word 1 position 0 to word 0 position 1.

The full packet is stored in the ingress LU formatter. Reshuffling starts when the first five words are received. They are stored again in another set of five-word buffers. The header information on which the switch acts to route the packet to the appropriate output port is moved to the appropriate byte location in the master LU during the cycles required to store the current packet's remaining words.

Note: Byte swapping is a separate function that is executed according to the 16 bits stored in the PE_Common register (byte position in LU formatter).



When 16 (or 8)-port mode is used, only bits 31:16 of the bit map field are required to identify the 16 switch core ports. The other bits are considered to be part of the payload. The outgoing packet is made up of four logical units (LU0, LU1, LU2, and LU3), each 16 bytes wide. The following tables show how the incoming packet bytes are rearranged inside the four LUs. Each line represents the content of each LU.

8 × 8 and 16 × 16 Switch LU Output Format

Container		C00	C01	C02	C03	C04	C05	C06	C07	C08	C09	C10	C11	C12	C13	C14	C15
Master LU0	Byte 0	PQ	BM1	BM2	D	D	D	D	D	D	D	D	D	D	D	D	D
Slave LU1	Byte 1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Slave LU2	Byte 2	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Slave LU3	Byte 3	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

32 × 32 Switch LU Output Format

Container	C00	C01	C02	C03	C04	C05	C06	C07	C08	C09	C10	C11	C12	C13	C14	C15
Master LU0	PQ	BM1	BM2	BM3	BM4	D	D	D	D	D	D	D	D	D	D	D
Slave LU1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Slave LU2	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Slave LU3	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

In a 32 × 32 switch, all of the bit map bytes (BM1, BM2, BM3, and BM4) are used for port addressing and for computing header parity. In a 16 × 16 switch, only BM1 and BM2 are used. BM3 and BM4 are considered payload and are ignored for the computation of the header parity. In an 8 × 8 switch, only BM1 is used. BM2 is ‘00’ so that it does not impact the computation of the packet qualifier parity.

3.3.1.3 Port Addressing

The following table shows the switch output port addressing (a '1' in any of the 32 bit map fields indicates that the packet should be sent to the corresponding switch output port).

UTOPIA-3 Bit Notation	7	6	5	4	3	2	1	0
Switch/DASL Bit	0	1	2	3	4	5	6	7
Output Port Bit Map 1	Port 0	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7
Output Port Bit Map 2	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15
Output Port Bit Map 3	Port 16	Port 17	Port 18	Port 19	Port 20	Port 21	Port 22	Port 23
Output Port Bit Map 4	Port 24	Port 25	Port 26	Port 27	Port 28	Port 29	Port 30	Port 31

3.3.2 Nested TxPause Extraction

In IBFC, the packet qualifier bits (27:26 and 31:30) are monitored to extract the converter egress flow control information (TxPause). The PE uses TxPause information to control flow at the switch's output port. The converter interprets these bits and translates them into the SEND_GNT signal to the switch. TxPause is dependent on the setting of bit 30 of the PE_Common register. When bit 3 (SEND_GNT per priority) of the Egress_PE_Interface register is not enabled, any bit set to '0' in the TxPause field is sufficient to stop transmission to the attached PE. For example, for the PRS28.4G, if the four TxPause bits are equal to '0', DASL stops egress packet transmission to the PE. If at least one TxPause bit is equal to '1', then packet transmission to the PE continues. For the IBM Packet Routing Switch PRS64G, the four TxPause bits are serialized on the SEND_GNT signal. When the four bits are equal to '0', DASL stops egress packet transmission to the PE (similar to the PRS28.4G).

3.3.3 Ingress Packets for IBFC

Byte	Byte 0								Byte 1								Byte 2								Byte 3							
	MSB																															LSB
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word 0	Packet Qualifier								1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
Word 1	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
Word 2	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
Word 15	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0

Table 3-3. Packet Qualifier Byte for Ingress Idle Packet

Idle Packet	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Bit Meaning	TxPause Bit 0	TxPause Bit 1	0	0	TxPause Bit 2	TxPause Bit 3	0	0
TxPause Priority Bit Map								
Highest	1	0			0	0		
Medium High	0	1			0	0		
Medium Low	0	0			1	0		
Low	0	0			0	1		
All	1	1			1	1		
None	0	0			0	0		

Table 3-4. Packet Qualifier Byte for Ingress Data Packet

Data Packet	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Bit Meaning	TxPause Bit 0	TxPause Bit 1	Active Bit ‘1’	Backup Bit ‘1’	TxPause Bit 2	TxPause Bit 3	Packet Priority Bits	
TxPause Priority Bit Map								
Highest	1	0			0	0		
Medium High	0	1			0	0		
Medium Low	0	0			1	0		
Low	0	0			0	1		
All	1	1			1	1		
None	0	0			0	0		

3.3.3.1 Ingress Packets for OBFC

In OBFC, the packet qualifier byte remains unchanged when the switch processes the packet.

Table 3-5. Packet Qualifier Byte for Ingress Data Packet

Data Packet	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Bit Meaning	0	Header Parity	Color/Type	Color/Type	0	0	Packet Priority Bits	
Color/Type								
Red Complemented			0	1				
Red			1	0				
Blue			1	1				
Packet Priority								
Highest							0	0
Medium High							0	1
Medium Low							1	0
Lowest							1	1

3.3.4 Egress Packet Formatter

The egress packet formatter is the interface between the egress FIFO and the PE interface logic that translates the switch LU format into the egress packet format which matches the format expected by the PE.

The egress packet formatter:

- Changes the position of the proper data bytes in the packet that have been moved in the ingress path
- Inserts the switch output queue grant and shared memory flow control information at the byte position occupied by the bit map and some of the packet qualifier bits
- Inserts idle packets when there is no data packet to be sent

Byte	Byte 0								Byte 1								Byte 2								Byte 3							
	MSB																															LSB
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word 0	Packet Qualifier								1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
Word 1	Output Queue Grant [31:24]								Output Queue Grant [23:16]								Output Queue Grant [15:8]								Output Queue Grant [7:0]							
	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
Word 15	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0

Table 3-6. Packet Qualifier Byte for Egress Idle Packet

Idle Packet	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Bit Meaning	Shared Memory Grant Priority Level		Shared Memory Status Hold = '0' Grant = '1'	Output Queue Grant Priority Indicator		0	Forced to '0'	
Memory Grant Priority Level Definition								
Highest	0	0						
Medium High	0	1						
Medium Low	1	0						
Lowest	1	1						
Output Queue Grant Priority Indicator								
Highest				0	0			
Medium High				0	1			
Medium Low				1	0			
Lowest				1	1			

Table 3-7. Packet Qualifier Byte for Egress Data Packet

Data Packet	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Bit Meaning	Shared Memory Grant Priority Level		Shared Memory Status Hold = '0' Grant = '1'	Output Queue Grant Priority Indicator		1	Packet Priority	
Memory Grant Priority Level Definition								
Highest	0	0						
Medium High	0	1						
Medium Low	1	0						
Lowest	1	1						
Output Queue Grant Priority Indicator								
Highest				0	0			
Medium High				0	1			
Medium Low				1	0			
Lowest				1	1			

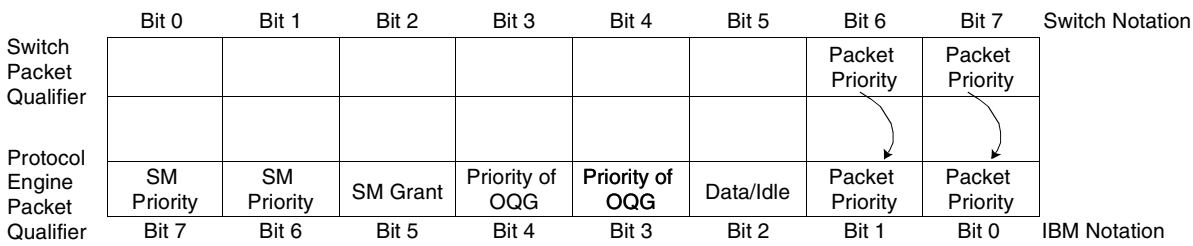
Table 3-7. Packet Qualifier Byte for Egress Data Packet

Data Packet	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Data Packet Priority Bit								
Highest							0	0
Medium High							0	1
Medium Low							1	0
Lowest							1	1

3.3.4.1 Building the Egress Packet Qualifier Byte

- Shared memory information:
  - The PQ-2 bit is replaced by the shared memory information (SM), which has a priority level that corresponds to shared memory grant priority levels PQ-0 and PQ-1 that cycle one priority after another.
- Output queue grant priority indicator:
  - The first two bits, PQ-3 and PQ-4, are loaded from the OQG priority-level values.
  - The other bits, PQ-6 and PQ-7, are unchanged because they belong to the data information contained in the packet.

Figure 3-12. Switch Packet Qualifier Bit Reshuffling



- Output queue grant byte description:
  - The converter egress block provides the OQG values. There are 16 or 32 bits for each priority.
  - For the PRS28.4G, the first OQG sent is an idle packet, priority level ‘00’. The OQG mechanism gives the priority level in the idle packet’s qualifier byte. The other OQGs are sent in data packets (or idle packets) and the process is looped. In every idle packet sent, the flywheel mechanism gives the priority level for checking the position in the loop.
  - The latest refreshed OQG bits are inserted into the packet header to the PE.

3.3.5 Egress Packets for OBFC

In OBFC, the packet qualifier byte remains unchanged when the switch processes the packet.

Table 3-8. Packet Qualifier Byte for Egress Data Packet

Data Packet	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Bit Meaning	0	Header Parity	Color/Type	Color/Type	0	0	Packet Priority Bits	
Color/Type								
Red Complemented			0	1				
Red			1	0				
Blue			1	1				
Packet Priority								
Highest							0	0
Medium High							0	1
Medium Low							1	0
Lowest							1	1

3.4 Packet Buffering

3.4.1 X and Y Path Receive FIFO (RXFIFO)

The RXFIFO block:

- Writes the data coming from the ingress formatter (clocked on the PE clock [URXCLK]) to the FIFO
- Reads the data from the FIFO to the X and Y paths to the Ingress DASL Interface (IDI) block, clocked on the X/Y path clock (accounting for the size of the packet in steps of four bytes)
- Detects and reports a FIFO almost full event, whose threshold is programmable through configuration registers
- Depending on the configuration table, RXFIFO either deasserts $\overline{\text{RXENB}}$ (if it is in use) or degrants shared memory priority 0 (highest) to create room in the RXFIFO when there is an indication of FIFO almost full

The FIFO is 256 bytes wide, or three 80-byte packets. A three-packet buffer temporarily stores incoming data packets, thereby allowing the insertion of a yellow packet without requiring any link-level flow control. This absorbs any clock difference between the PE and the switch.

3.4.2 X and Y Path Transmit FIFO (TXFIFO)

The X and Y path TXFIFO block:

- Writes the data from the X or Y path transmit extraction block as clocked on DASL_X_CLK or DASL_Y_CLK, respectively, to the FIFO
- Reads the data from the FIFO to the path selection block, clocked on UTXCLK (PE clock)
- Detects and reports a FIFO almost full event, whose threshold is programmable
- Detects and reports a FIFO not empty, whose threshold is programmable

- Stops its data flow when the path selection block decides to stop the data flow

Data packets are never written in a reserved path's FIFO.

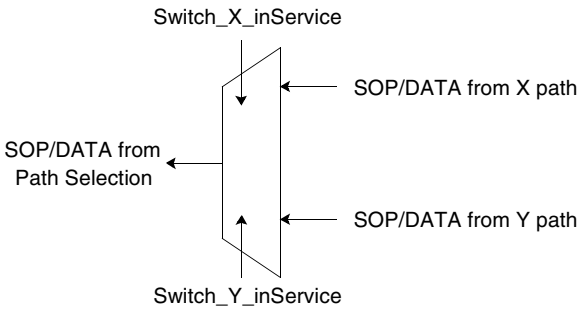
When the FIFO is almost full, SEND_GNT to the switch is deasserted.

The FIFO is 480 bytes wide, or six 80-byte packets. Six packets of buffer in the TXFIFO take into account the switch's latency in reacting to SEND_GNT (three packets, in the worst case). This is true when asserting or deasserting SEND_GNT.

3.5 Path Selection Block

This block selects the X or Y FIFO depending on the switch control's X_inService or Y_inService inputs (see Figure 3-13). Only the selected path's TXFIFO is filled with packets, the other one is empty. Switching from one path to the other is done on a packet boundary; however, this may result in duplicated or missing packets.

Figure 3-13. Path Selection



-X_inService	-Y_inService	Selector Status
True	False	Path X is selected.
False	True	Path Y is selected.
True	True	No Path is selected.
False	False	No Path is selected.

The attached microprocessor polls the bits to check the validity of the path selection. Use the following scheme to force any path with the force bit to perform a switch-over at the switch core level and to verify that the X_/Y_inService lines operate properly.

Force Path Selection	Select X/Y	Selector Status
0	X	Selection is based on physical wires.
1	0	Path X is selected.
1	1	Path Y is selected.
Note: When Select X/Y = 0, then path X is selected. When Select X/Y = 1, then path Y is selected.		

3.6 Interfacing the DASL Macro

3.6.1 Ingress DASL Interface

The Ingress DASL Interface (IDI) logic is the interface between the ingress FIFO and the DASL macro. The IDI feeds the DASL macro with data packets in response to a DASL packet request. When no packet is available to send to the DASL, the IDI provides an idle packet to the DASL macro. Data packets sent to the DASL macro come from the ingress FIFO. The IDI provides the packet clock to the output logic of the ingress FIFO and to the DASL macro. The IDI also triggers the ingress FIFO output scheduler operation.

During the initial training sequence required to synchronize the remote switch DASL, the IDI provides “synchronization packets.” The IDI is also designed to insert link liveness packets (liveness function covered by yellow packets) into the flow of packets sent to the DASL box following a request from the control interface. When data mode is activated, the IDI is fed with available data packets, otherwise it generates an idle packet (lack of data packet). Idle packets carry Cyclic Redundancy Checks (CRCs; one per LU) to protect logical unit transport media (converter and switch).

3.6.1.1 IDI Functions

- Generates an idle packet when no data is available from the ingress FIFO
- Generates a synchronization packet when the DASL training sequence is running
- Generates a yellow packet when requested by the control interface
- Forwards data packets
- Provides LU protection by inserting CRCs in idle packets
- Provides a packet clock to the ingress FIFO
- Provides a packet request to the ingress FIFO output scheduler
- Is compatible with the DASL interface LU/byte/bit map

3.6.1.2 Packet Formats

Idle Packet Format

Idle packets are generated by IDI logic when no data packet is available from the ingress path. Idle packets have the following format:

Master LU	PQ	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	CRC
Slave LU	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	CRC
Slave LU	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	CRC
Slave LU	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	CRC

The master LU must be routed to the master switch.

Note: Yellow packets sent to the switch are considered idle packets and, therefore, contain CRC trailers.

Idle packet CRCs detect physical media errors. The last byte of each of the four LUs within an idle packet carries a CRC byte that protects the LU.

The CRC polynomial is $X^8+X^4+X^3+X^2+1$. The CRC register is initialized (software configuration) depending on the LU depth. The CRC byte is computed from the end of the last idle packet on the DASL interface to just before the last byte of the current idle packet. In other words, the CRC computation is performed on one byte less than the LU size.

Synchronization Packet Format

Synchronization packets synchronize DASLs. Characteristics of this packet allow the remote DASL operating as receiver to recover bit transition and packet delineation (packet clock recovery). The synchronization packet format is as follows:

Master LU	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘33’
Slave LU	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘33’
Slave LU	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘33’
Slave LU	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘33’

Data Packet Format

- 8 × 8 and 16 × 16 Switch Data Packet Format

Master LU	PQ	BM0	BM1	D	D	D	D	D	D	D	D	D	D	D	D	D
Slave LU	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Slave LU	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Slave LU	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

- 32 × 32 Switch Data Packet Format

Master LU	PQ	BM0	BM1	BM2	BM3	D	D	D	D	D	D	D	D	D	D	D
Slave LU	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Slave LU	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Slave LU	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Note: PQ refers to a packet qualifier and BM refers to a bit mapping.

3.6.2 Egress DASL Interface

Converter packets have a fixed length of 64 to 80 bytes (based on the setting in the configuration register) and are mapped on four-byte words. Therefore, a new packet is received every 16 to 20 clock cycles from the DASL. When a complete packet has been received, the 16 to 20 words are transferred to the egress FIFO.

The Egress DASL Interface (EDI) analyzes the switch packet header from the master LU to indicate the presence of an idle packet or data packet and the packet priority. Idle packets are discarded when received (no packet write request is presented to the egress FIFO). The EDI block also checks the LU CRC (mapped into the idle packet’s LU trailer). When an error is detected, the converter interrupt line is asserted (if the checker is enabled) and the idle CRC error counter is incremented.

The EDI checks switch header parity. An error count is incremented when an error is detected and the processor interruption line is asserted (may be masked). An optional “error” packet discard function is provided.

The EDI performs switch grant extraction from the switch packet header. A grant information bit map is carried into the switch output packet header and is reported per priority. Grant information is refreshed over four packet periods (if the four priorities are in use) for a given priority. A flywheel counter mapped into the idle packet qualifier synchronizes the converter with the switch counter.

The EDI grant extraction mechanism is synchronized on the incoming idle packet grant flywheel counter. When a desynchronization problem is detected between the switch counter and the EDI grant flywheel counter, an error is reported and the EDI flywheel counter is automatically resynchronized. In order to minimize the latency of the switch grant mechanism, the grant vector is extracted before the completion of the packet reception.

The EDI performs switch memory grant synchronization. Memory grant information and destination grant vectors are passed to the in-band grant generation block for insertion into the egress packets. The EDI is also the PE interface wrap point.

3.6.2.1 EDI Functions

- Detects idle packets received from the switch
- Synchronizes itself to the switch output queue grant counter
- Performs output queue grant extraction (one to four priority traffic)
- Indicates when a yellow packet is received (maskable error interruption)
- Provides LU CRC checking (maskable error interruption)
- Provides header parity checking (maskable error interruption) with optional discard
- Detects when a data packet is received
- Provides a wrap indication input line (grant indication bypass)

3.6.2.2 Packet Formats

Idle Packet Format

Idle packets received from the EDI have the following format:

- 16 $\times$ 16 Switch Interface

Container	C00	C01	C02	C03	C04	C05	C06	C07	C08	C09	C10	C11	C12	C13	C14	C15
Master LU	PQ	OQG1	OQG2	x‘00’	x‘00’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘00’	x‘00’	x‘00’	x‘00’	CRC
Slave LU	x‘CC’	x‘00’	x‘00’	x‘00’	x‘00’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘00’	x‘00’	x‘00’	x‘00’	CRC
Slave LU	x‘CC’	x‘00’	x‘00’	x‘00’	x‘00’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘00’	x‘00’	x‘00’	x‘00’	CRC
Slave LU	x‘CC’	x‘00’	x‘00’	x‘00’	x‘00’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘00’	x‘00’	x‘00’	x‘00’	CRC

For idle packets, the packet qualifier is mapped as follows:

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	Header Parity PQ OQG1 OQG2	0	0	00 (Blue Colored Packet) 01 (Red Colored Packet)		00 Highest Priority 01 10 11 Lowest Priority Flywheel Counter Synchronization	

Parity bit is even parity over three bytes: PQ, OQG1, and OQG2.

- 32 × 32 Switch Interface

Master LU	PQ	OQG1	OQG2	OQG3	0QG4	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	CRC
Slave LU	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	CRC
Slave LU	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	CRC
Slave LU	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	x‘CC’	CRC

In the packet qualifier, the parity bit is even parity over five bytes: PQ, OQG1, OQG2, OQG3, and OQG4.

Note: The content of the packet qualifier byte for yellow packets received from the switch is ‘0p00 1000’ (p is the header parity bit computed on the PQ, BM1, and BM2 in the 16-port configuration and on PQ, BM1, BM2, BM3, and BM4 in the 32-port configuration). The packet qualifier byte does not contain flywheel synchronization information because it is generated by the switch control. In the switch, egress yellow packets are considered data packets and, therefore, do not contain link CRC information fields. Yellow packets are detected and an interruption is reported when the detection function is enabled. Yellow packets never carry CRC information whether yellow packet detection is enabled or not and are always discarded.

Idle packet CRCs detect physical media errors. The last byte of each of the four LUs within an idle packet carries a CRC byte that protects the LU. The four LU CRC bytes are cumulative between two idle packets. (The CRC generation latches are not reset between idle packets.)

The CRC polynomial is $X^8+X^4+X^3+X^2+1$. The CRC register is initialized (bits 31:24 of the Control_X_PATH and Control_Y_PATH registers) depending on the LU depth.

Data Packet Format

The data packet format can be made of LUs of 16 to 20 bytes long depending on the configuration register.

- 8 × 8 and 16 × 16 Switch Data Packet Format

Master LU	PQ	OQG0	OQG1	D	D	D	D	D	D	D	D	D	D	D	D	D
Slave LU	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Slave LU	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Slave LU	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

- 32 × 32 Switch Data Packet Format

Master LU	PQ	OQG0	OQG1	OQG2	OQG3	D	D	D	D	D	D	D	D	D	D	D
Slave LU	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Slave LU	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Slave LU	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

3.6.3 Switch In-Band Output Queue Grant Information

Bytes BM1 and BM2 carry the output queue grant from the switch. This information is carried for all 16 output ports simultaneously for a given priority. Consecutive packets, either data or idle, carry a different priority of output queue grant bits, cycling from 0 to the highest priority value that is enabled. For example, when two priorities are enabled, it takes two packets to transmit the output queue grant information.

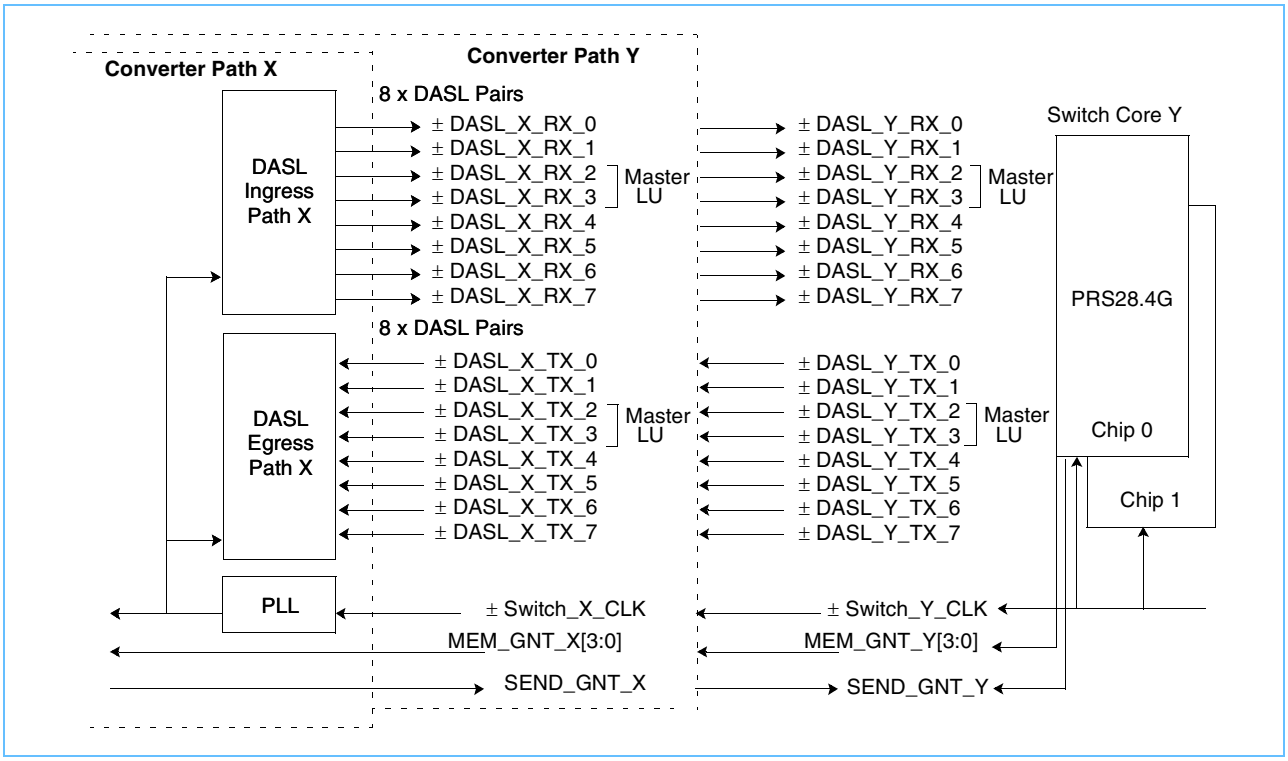
Table 3-9. Output Queue Grant Bit Map Fields

UTOPIA-3 Bit Notation	7	6	5	4	3	2	1	0
Switch/DASL Bit	0	1	2	3	4	5	6	7
Output Queue Grant 1	Port 0	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7
Output Queue Grant 2	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15

When an output queue grant field bit is set to ‘1’, data can be sent to the corresponding output queue. When set to ‘0’, no data should be sent to that output queue. The switch sets (8-port mode) OQG1 to x‘FF’ when operating in internal speed expansion mode. If a yellow packet is detected when detection is enabled, an interruption is reported. If detection is not enabled, the yellow packet is considered an idle packet.

3.6.4 Converter Switch Interface

Figure 3-14. Converter Interface Lines



3.7 Grant Control Generation

This section provides output queue grant information (side-band channel made of three serial links and one framing line and timed by the TXCLOCK).

The grant information is:

- The priority of each port (that is, the output queue grant information)
- Shared memory information
- The memory grant of the selected X or Y plane

The grant is removed (deasserted) when the fill is greater than or equal to the threshold. Note that the memory full thresholds and the output queue thresholds both operate with this scheme. The assertion of the grant uses the complement of the previous condition. Therefore, a grant is asserted when the fill is less than the threshold.

The integrity of the sent data is checked by an odd parity bit. The port priority data (converter OQG) is extracted from the header of all incoming packets in the TXFIFO block. The port priority data is also registered in the grant control generation block to send it in band via the transmit LU framing block.

3.7.1 Per Priority Side-Channel Modes

There are four priority modes:

- Priority 0
- Priority 1
- Priority 2
- Priority 3

Each priority description is sent in a distinct block over 16 clock periods. At the beginning of the first block, that is, the priority 0 block, the start_GCXFR pin is asserted.

Port grant odd describes ports 1 to 8 and 17 to 24. Port grant even describes ports 9 to 16 and 25 to 32.

For example, at the clock period number 5 in the priority 1 block, port grant odd is ‘0’, port grant even is ‘1’. This means that port 12 is granted and port 4 is not granted. All of the bits of port grant odd and port grant even in each block are written according to the OQG values.

3.7.2 Shared Memory Bits

Shared memory information is given in the SM_X_PADIN signal from the switch.

Mode	Bits	Description
Two Priorities	SM0, SM1	Written in bits C3 to C4, respectively, of the shared grant pin during each block.
Three Priorities	SM0, SM2	Written in bits C3 to C5, respectively, of the shared grant pin during each block.
Four Priorities	SM0, SM3	Written in bits C3 to C6, respectively, of the shared grant pin during each block.

3.7.3 Parity

Odd parity is computed on all 48 bits sent in each block (that is, the data bits sent on port grant odd, port grant even, and shared grant). The parity bit is given in the last bit of the shared grant pin (that is, C16) in each priority block.

3.7.4 Memory Grant

This is a copy of the selected memory grant Y or memory grant X, depending on the select_y_padin/ select_x_padin value.

3.8 Egress and Ingress Interface Diagnostic Functions

3.8.1 Loopbacks

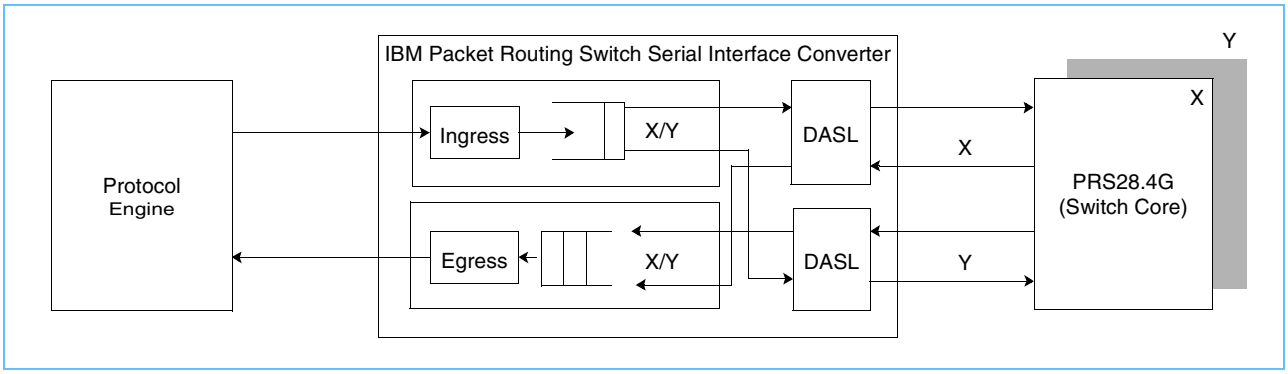
Loopbacks are controlled through configuration registers. There are two possible paths, X and Y, for each loopback. An exclusive choice must be made and a path reset executed before the loopback is performed. The converter supports two loopback modes:

- Protocol Engine X/Y loopback: the PE sends and checks data, and the grant mechanism must be bypassed (forced to all ones through the configuration register).
  - Protocol Engine X domain loopback (Setup_1_X_PATH register, bit 0 set to ‘1’).
  - Protocol Engine Y domain loopback (Setup_1_Y_PATH register, bit 0 set to ‘1’).
- Switch loopback: data is initiated from the switch and the switch control verifies the overall operation.
  - Switch X and switch Y domain loopbacks (Egress_PE_Interface register, bit 1 set to ‘1’). Depending on the status of the Forcepath and SelectX/Y bits, bits 22:21 of the Common_Control register, it is possible to use either the InService line or the Select X/Y (bit 22) to decide which plane is selected. In the latter case, plane X is used if set to ‘0’ and plane Y is used if set to ‘1’.

3.8.1.1 Normal Operating Mode

Data sent by the PE to the switch core is transferred to the ingress PE interface where it is parity checked, LU formatted, and queued to both planes for transmission by the DASL (see Figure 3-15). Data transmitted by the switch core is checked for framing consistency and header parity, queued, and word formatted for transmission by the egress PE interface.

Figure 3-15. Configuration in Normal Operating Mode

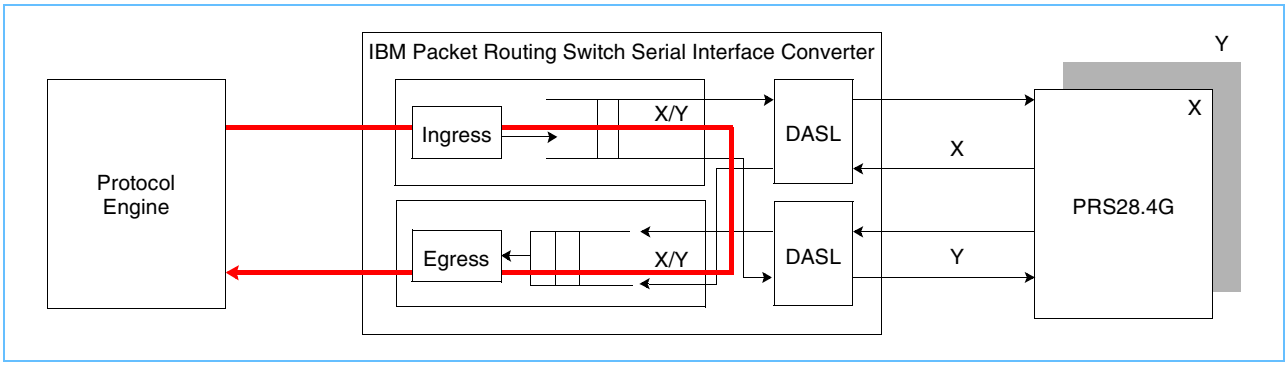


3.8.1.2 Protocol Engine X/Y Loopback

Protocol Engine X/Y loopback provides a connection from the ingress PE bus to the egress PE bus (see Figure 3-16). This loopback mode can be activated on either path X or path Y, but not on both simultaneously. In loopback mode, the converter is internally disconnected from the DASL macro for both the data and control buses and does not test the DASL macro. The loopback is initiated on a packet boundary.

Note: A switch plane (or substitute) clock must be present on the converter’s switch interface.

Figure 3-16. Protocol Engine Loopback Through Path X or Path Y



Perform the following procedure to execute the PE X/Y domain loopback (starting from operational mode):

1. Reset the path to be set in loopback.
2. Force X or Y switch plane in service (switch control can also decide in this mode).
3. Select the clock source (switch or microprocessor) for the plane to be wrapped.
4. Set the PE loopback bit corresponding to the plane to be set in loopback.
5. Initiate the traffic from the PE.

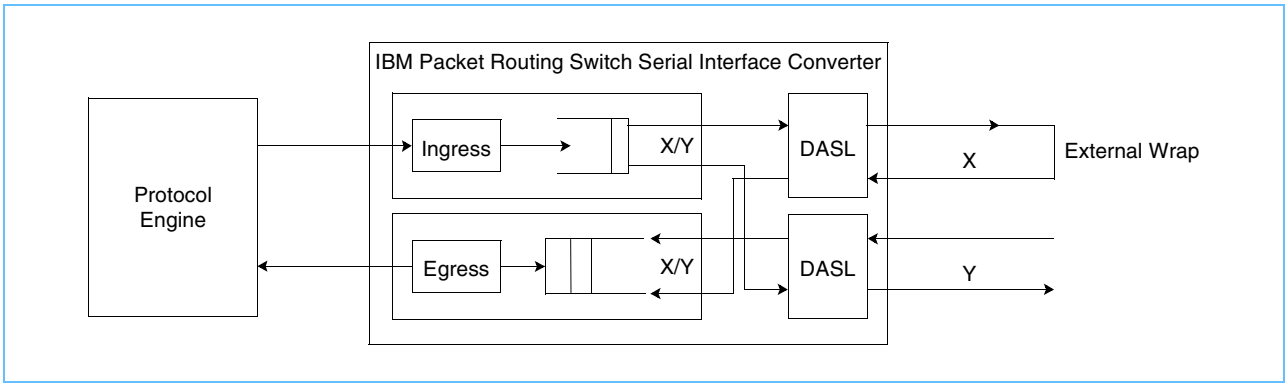
Data transfer must have been stopped for long enough and in such a way that all buffers are empty before the loopback is initiated. If the buffers are not empty, reset the path on which the loopback is to be performed. To execute the loopback, the converter must be set in OBFC mode to avoid modifying the packet qualifier byte.

3.8.1.3 Protocol Engine External Loopback

The PE bus is wrapped via the DASL interface. The switch is disconnected from the converter. A wrap plug is connected to the DASL port corresponding to the path to be tested. See Figure 3-17.

Note: The switch plane (or substitute) clock must be selected.

Figure 3-17. Protocol Engine External Loopback Through Path X



The following operational sequence must be performed to execute a PE external loopback:

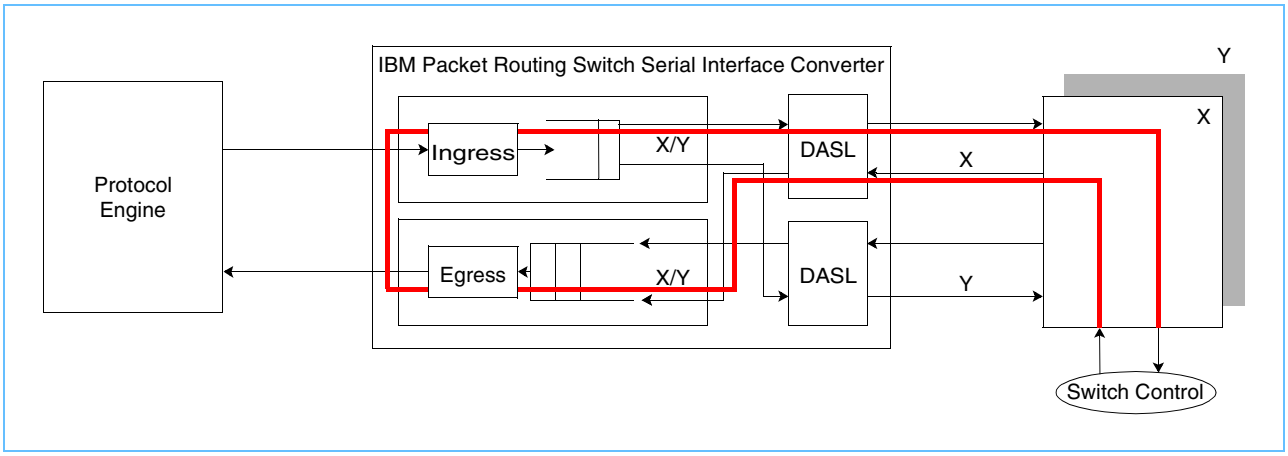
1. Reset the path to be set in loopback.
2. Force X or Y switch plane in service.
3. Select the clock source (switch or microprocessor) for the plane to be wrapped.
4. Synchronize the DASL.
5. Initiate the traffic from the PE.

The PE external loopback can be performed without the switch clock by using the microprocessor clock and properly programming the phase-locked loops (PLLs). (Each PLL must be reset to acquire its newly programmed value.) In all cases, the objective is to be in the frequency range of 100 to 125 MHz to allow DASL operation.

3.8.1.4 Switch X/Y Loopback

Switch X/Y loopback provides a connection from the egress input to the ingress output to the ingress input through either the X or the Y path (see Figure 3-18). During this test, $\overline{\text{RXENB}}$ is deasserted so that the PE cannot send data. The result of this test is obtained through the switch control.

Figure 3-18. Switch X Loopback



Perform the following operational sequence to execute the switch loopback (starting from operational mode):

1. Set the converter in OBFC mode.
2. Force X or Y switch plane in service or let the switch control decide which switch plane is in service.
3. Set the switch loopback bit corresponding to the plane to be set in loopback.
4. Initiate the traffic from the switch control.

Data transfer must have been stopped for long enough and in such a way that all buffers are empty before the loopback is initiated. If the buffers are not empty, reset the path on which the loopback is to be performed. To execute the loopback, the converter must be set in OBFC mode to avoid modifying the packet qualifier byte.

3.9 Clock Generator Description

Figure 3-19. Clock Distribution

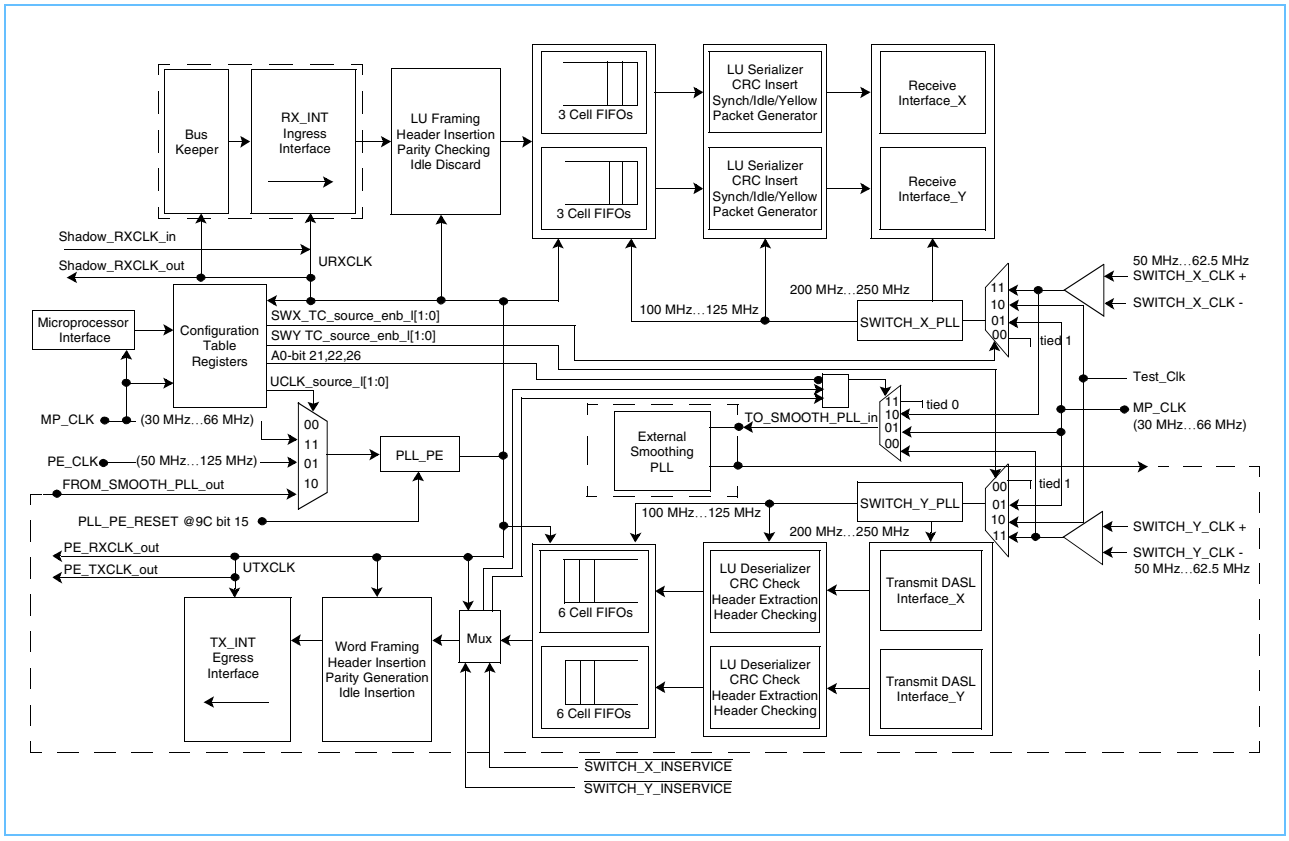


Table 3-10. Selecting the Signal That Appears on the TO_SMOOTH_PLL_IN Signal

SW_X_IN	SW_Y_IN	SelectX/Y (Common_Control Register, Bit 22)	Forcepath (Common_Control Register, Bit 21)	SMOOTH_select_enb_I (Common_Control Register, Bit 26)	TO_SMOOTH_PLL_IN
X	X	0	1	1	SWITCH_X
X	X	1	1	1	SWITCH_Y
0	0	X	0	1	MP_CLK
0	1	X	0	1	SWITCH_Y
1	0	X	0	1	SWITCH_X
1	1	X	0	1	MP_CLK
X	X	X	X	0	0

Table 3-11. External Clock Descriptions

Clock Name	Speed	Description
SWITCH_X_CLK ±	50 to 62.5 MHz	Differential input receiver clock lines. The associated PLL (SWITCH_X_PLL) delivers both 200 to 250 MHz (DASL_X250_CLK) and 100 to 125 MHz (DASL_X125_CLK) to clock the DASL_X and the path X glue logic. An additional input is provided to connect an external oscillator TEST_CLCK or the MP_CLK instead of the SWITCH_X_CLK on the PLL_X input. SWX_TC_source_enb_l[1:0] is located in the configuration table registers (Common_Control register, bits 25:24).
SWITCH_Y_CLK ±	50 to 62.5 MHz	Differential input receiver clock lines. The associated PLL (SWITCH_Y_PLL) delivers both 200 to 250 MHz (DASL_Y250_CLK) and 100 to 125 MHz (DASL_Y125_CLK) to clock the DASL_Y and the path Y glue logic. An additional input is provided to connect an external oscillator TEST_CLK or the MP_CLK instead of the SWITCH_Y_CLK on the PLL_Y input. SWY_TC_source_enb_l[1:0] is located in the configuration table registers (Common_Control register, bits 15:14).
PE_CLK	50 to 125 MHz	Single-ended receiver clock line. This is the transfer/synchronization clock issued from the PE to synchronize transfers on RXDATA[31:0]. It is connected to the PE_PLL that delivers the URXCLK/UTXCLK for the ingress/egress interfaces. The PE_CLK input is controlled by PLL_PE_RESET (PE_PLL register, bit 15) and is turned in bypass mode in case PLL_PE_RESET is equal to ‘1’. Programming PLL_PE_RESET at ‘1’ disables the PE PLL from delivering the necessary clocks for the ingress and egress interfaces.
MP_CLK	30 to 66 MHz	Single-ended receiver clock line. This is a free running clock that must be available at POR when the MP_CLK directly clocks the configuration table registers to provide correct register map initialization.
PE_RXCLK_out PE_TXCLK_out		Protocol engine clocks. These are single-ended output driver clock lines that allow the transfer and synchronization of the RXDATA[31:0] and the TXDATA[31:0] to and from the converter. They are derived from clock sources selected through the setting of the Common_Control register, bits 22:21 and 26 (SMOOTH_select_enb_l) and bits 31:30 (UCLK_Source_l).
Shadow_RXclock_In	50 and 125 MHz	Single-ended receiver clock line. It is applied to the ingress interface by programming the RXDATA_KEEPER field (bit 2) of the Ingress_PE_Interface register, to ‘1’. When the RXDATA_KEEPER is equal to ‘0’, Shadow_RXclock_Out is routed to the ingress PE interface (this setting is used for switch loopback application).
Shadow_RXclock_Out		A single-ended output driver clock line derived directly (not going through any clock tree) from PE PLL output. It connects to Shadow_RXclock_In through either the PE device or the board (via a delay) to provide the best sampling point of the received data from the protocol engine.

3.9.1 Converter Internal Clock Description

The converter clock tree centers around three PLLs and the microprocessor clock (MP_CLK). Seven clock domains exist to clock the converter. The clock generator acts as a programmable selector. UTXCLK and URXCLK internal clock trees are generated from several clock sources that are selected by programming the “UCLK_source_l[1:0]” and “XY_SW_source_enb_l[1:0]” in the configuration table registers.

3.9.2 Converter External Traffic

External traffic from the converter and the switch is timed using the two edges of the clock issued from the switch X PLL or the switch Y PLL. Switch X and switch Y PLLs deliver two clocks that are 100 to 125 MHz (DASL_X125_CLK) and 200 to 250 MHz (DASL_X250_CLK), respectively. The X/Y transmit and the X/Y receive DASLs are clocked by the DASL_X250_CLK and DASL_Y250_CLK, respectively. Receive and transmit data are then input and output at a frequency of 400 to 500 MHz. At each occurrence of the DASL_X/Y250_CLK clock edge, transition data is sent to or received from the switch.

3.10 Converter Reset Scheme Description

The converter allows total and selective reset. Path X and path Y can be reset together or independently. The ingress and egress interfaces and their associated FIFOs are reset independently. External reset, programmable reset, and power-on reset (POR) are implemented in the converter.

3.10.1 Reset Strategy

The converter is reset when POR is active. POR forces tri-state drivers to the high impedance state and sets bidirectional I/Os in the receive state. The microprocessor interface and configuration table register are reset, and then the PE interface, FIFOs and their associated logic, and path X/Y are reset.

When RESET_X is active, path X is reset. When RESET_Y is active, path Y is reset. DASL X/Y differential drivers are set to a high impedance state.

MP_INTERFACE initiates the reset by a write access to the bit that needs to be reset. A second write access is necessary to restore the bit to its inactive position.

The following table shows the different reset cases:

Module	Power-On Reset	Common_Control Register		Configuration	
		Bit 0	Bit 1	Register Name	Bit
Configuration Table Registers	X				
MP_INTERFACE	X				
PE_PLL	X			PE_PLL	15
UTOPIA-3 PE Interface	X			Common_Control	8
LU_FRAMING	X			Common_Control	8
PATH_X INGRESS FIFO	X	X		Control_X_PATH	10
PATH_Y INGRESS FIFO	X		X	Control_Y_PATH	10
WORD_UNFRAMING	X			Common_Control	8
SWITCH_X_PLL	X			Switch_X_PLL	15
PATH_X EGRESS FIFO	X	X		Control_X_PATH	11
PATH_Y EGRESS FIFO	X		X	Control_Y_PATH	11
RESET PATH_X_SDC	X	X		Common_Control	4
RESET PATH_Y_SDC	X		X	Common_Control	5
SWITCH_Y_PLL	X			Switch_Y_PLL	15
RESET X_DASL	X	X		Common_Control	2
RESET Y_DASL	X	X		Common_Control	3

Note: "X" indicates that activating the reset function or writing to the Common_Control register bit will reset the indicated module.

3.10.2 Power-On Reset Procedure

The POR action uses the external MP_CLK microprocessor clock to reset the device. All drivers are set to high impedance during the POR. The register table controlling those output lines must be reconfigured after POR.

After POR action, the converter must be reconfigured via the microprocessor interface. The PLLs are switched into bypass mode and neither path X nor path Y are configured.

The POR external signal is an asynchronous signal. Power-on reset occurs while the POR signal is low. Power-on reset terminates when the POR signal is high. POR must be asserted for at least ten MP_CLK cycles to insure proper device reset.

The following table shows pin/pad test I/O initialization values (the values during and after reset):

Pin Name	Value in System	Description
CE1_A	1	Level-sensitive scan design (LSSD) test A clock.
CE1_B	1	LSSD test B clock.
CE1_C1	1	LSSD test C clock.
CE1_C2	1	LSSD test C clock.
CE0_IO	0	Used to force the JTAG EXTEST operation.
CEO_Scan	0	A and B clock gating, used also as clock splitter gate input.
CE0_TEST	0	Used to control boundary scan feature.
TEST_B2	1	LSSD test B clock (if required).
TEST_C3	1	LSSD test C clock (if required).
DI1	1	Driver inhibit (for non-test I/O).
DI2	1	Driver inhibit (for test I/O).
RI	1	Receiver inhibit.
TDI	1	JTAG serial input.
TCK	1	JTAG clock.
TMS	1	JTAG control signal.
TRST	1	JTAG asynchronous reset.

3.10.3 Path Reset

Individual path X and path Y resets are performed by addressing an appropriated bit in the Common_Control register (CCR). SWITCH_X_PLL or SWITCH_Y_PLL must run during the path X/Y reset action. PLLs are not affected by path X/Y resets, but the PLL must be reset when an external loopback is initiated with a new clock source (the PLL needs a delay to lock). Once a reset is established, the software must reconfigure bits 3:0 of the Common_Control register into system mode.

Reset Name	Impact	Reset
Xreset	No impact on path Y	Program CCR, bit 0, to ‘1’ in the configuration table registers.
YReset	No impact on path X	Program CCR, bit 1, to ‘1’ in the configuration table registers.
XDASLReset	No impact on Y DASL	Program CCR, bit 2, to ‘1’ in the configuration table registers.
YDASLReset	No impact on X DASL	Program CCR, bit 3, to ‘1’ in the configuration table registers.

3.10.4 PLL Reset

Once a reset is established, the software must reconfigure bit 15 of the Switch_X_PLL, Switch_Y_PLL, or the PE_PLL register to ‘0’ (system mode).

Reset Name	Impact	Reset
Switch X PLL	Exclusive - No impact on other PLLs	Program bit 15, PLL_SWX_RESET, to ‘1’ in the Switch_X_PLL register.
Switch Y PLL	Exclusive - No impact on other PLLs	Program bit 15, PLL_SWY_RESET, to ‘1’ in the Switch_Y_PLL register.
PE PLL	Exclusive - No impact on other PLLs	Program bit 15, PLL_PE_RESET, to ‘1’ in the PE_PLL register.

3.10.5 Ingress/Egress Interface Reset

Ingress and egress interfaces are reset upon software request. An interface reset restores the internal scheduler to the idle phase. Transfer data is lost and internal registers are swapped to their reset position. Signals that drive the PE outputs are switched to hold the PE interface drivers in inactive state.

Both ingress and egress PE interfaces are reset simultaneously by programming bit 8 of the Common_Control register to ‘1’ in the configuration table registers. Once the reset is established, the software must reconfigure bit 8 of the Common_Control register to ‘0’ (system mode).

3.11 Microprocessor Interface Description

The converter is initialized and controlled via a processor interface that works on an 8-bit data bus and operates in two modes. The external input pin MP_BURST_SEL selects the operational mode (low 8-bit mode and high 32-bit mode):

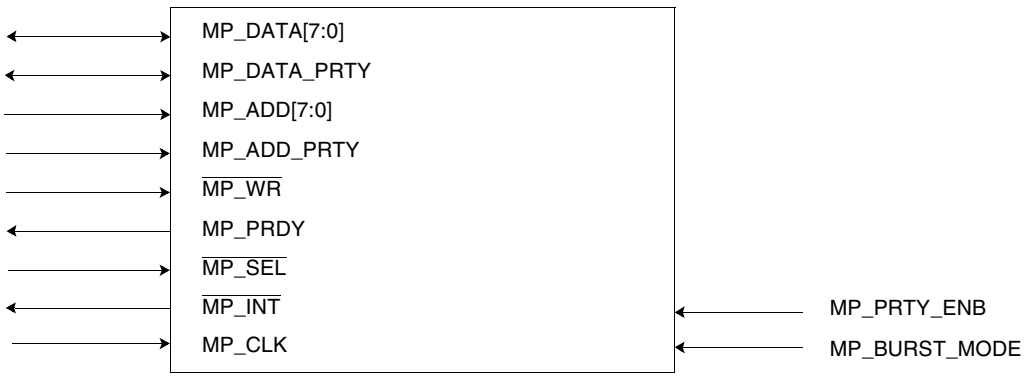
- 8-bit mode (byte mode): The converter registers are considered single 8-bit registers and are addressed via MP_ADD[7:0] address bus signals. Each register access is a single-cycle access of one byte.
- 32-bit mode (burst mode): The converter registers are considered as single 32-bit registers and are addressed via MP_ADD[7:2] address bus signals. Each access is a burst access of four bytes. The burst order is data bits 7:0, data bits 15:8, data bits 23:16, and data bits 31:24.

The microprocessor interface:

- Provides read/write access to all device registers
- Provides DASL picocode downloading
- Provides error reporting
- Collects the converter interrupts and passes them to the attached processor
- Monitors all interrupt signals generated by other converter functional blocks and, when one is asserted, latches and holds the value until the interrupt event register is read and reset.
- Provides the necessary handshake protocol to interface the attached processor, including address bus decoding, wait state insertion, data bus driver control, and optional parity checking on both the data and address buses.

3.11.1 Processor Interface Lines

Figure 3-20. Converter Processor Interface Lines



3.11.2 Processor Interface I/O Line Descriptions

The processor interface is synchronized to the external processor clock. This clock operates at a different frequency than the switch fabric clock.

Pin Name	I/O	Width	Description
MP_DATA_[7:0]	BiDi	8 bits	Bidirectional Data Bus. Hi-Z when no access is being processed. MSB 7 LSB 0
MP_DATA_PRTY	BiDi	1 bit	Data Byte Odd Parity. Hi-Z when no access is being processed. The converter checks during write operation and generates during read operation. Parity checker can be disabled.
MP_ADD[7:0]	In	8 bits	Address Bus MSB 7 LSB 0
MP_ADD_PRTY	In	1 bit	Address Bus Odd Parity. Converter checks during read and write access. Default is parity checker disabled.
$\overline{\text{MP\_RNW}}$	In	1 bit	Read/Write Line Low Read operation. High Write operation.
MP_PRDY	Out		Ready Signal. Asserted high when data is valid on the bus (for read) or when data is written into converter (for write). Driven by converter. Hi-Z when converter is not selected.
$\overline{\text{MP\_SEL}}$	In		Converter selected when low.
MP_CLK	In		Processor interface clock (maximum frequency of 66 MHz).
$\overline{\text{MP\_INT}}$	Out		Converter Processor Interrupt. Asserted low when interruption is pending.
MP_PRTY_ENB	In	1 bit	Low Disables generation and checking of processor data and address parity. High Enables generation and checking of processor data and address parity.
MP_BURST_MODE	In	1 bit	Low 8-bit byte mode. High 32-bit burst mode.

3.11.3 32-Bit Mode Processor Interface Timing

Figure 3-21. Processor Read Access in 32-Bit Burst Mode

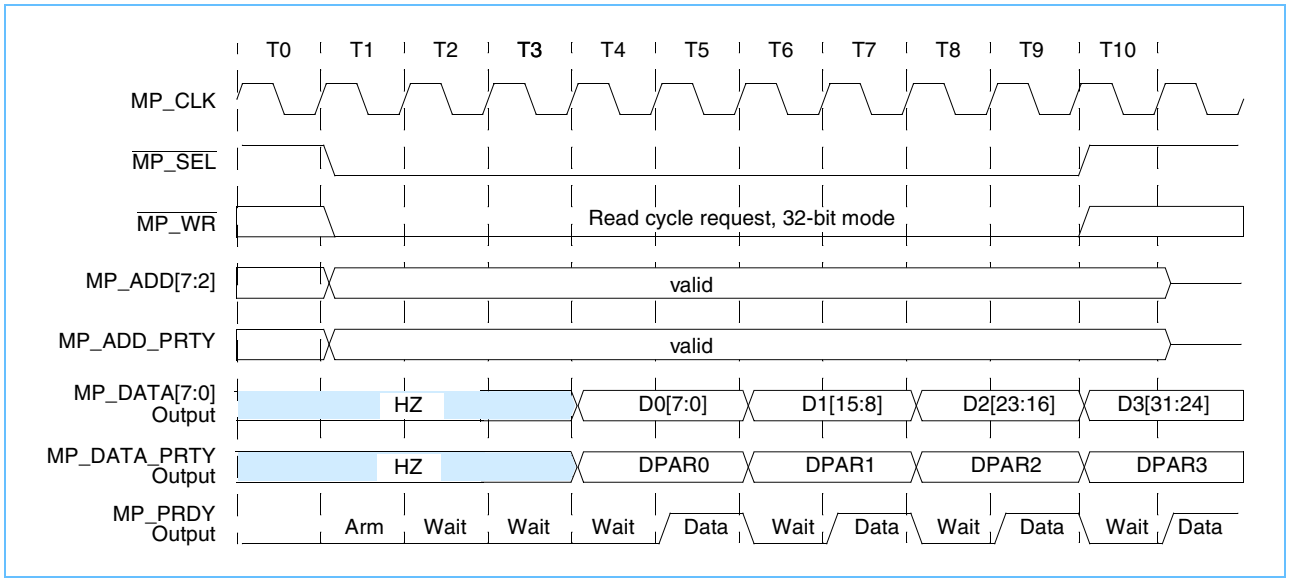
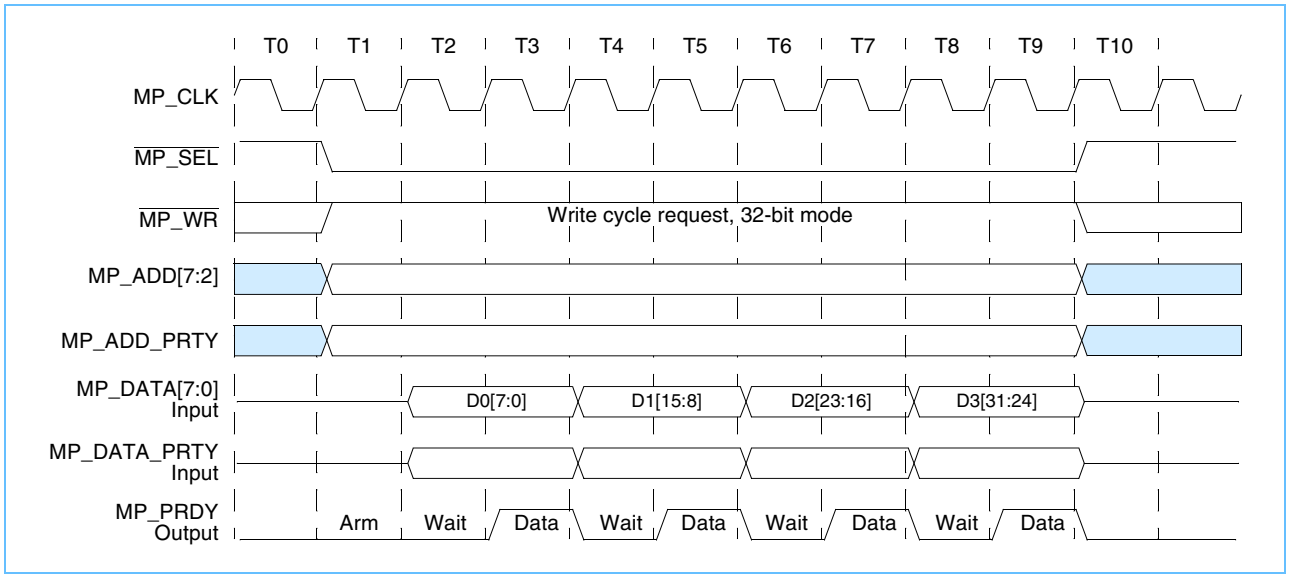


Figure 3-22. Processor Write Access in 32-Bit Burst Mode



3.11.4 8-Bit Mode Processor Interface Timing

Figure 3-23. Processor Read Access in 8-Bit Byte Mode

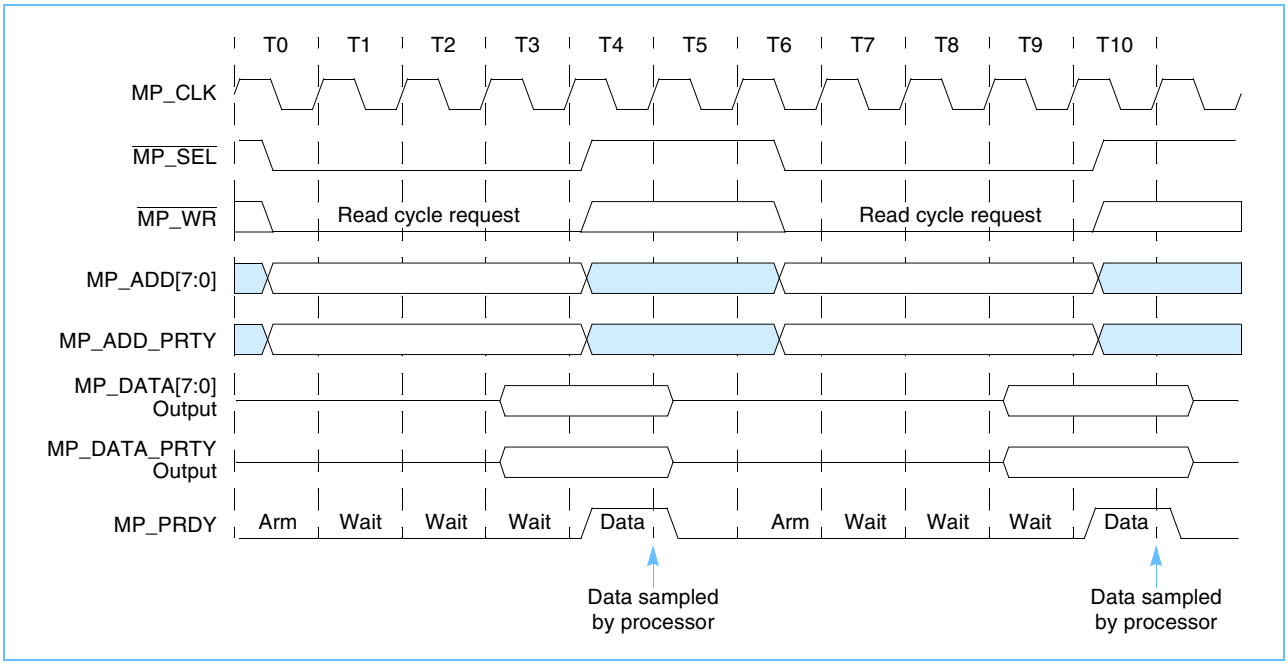
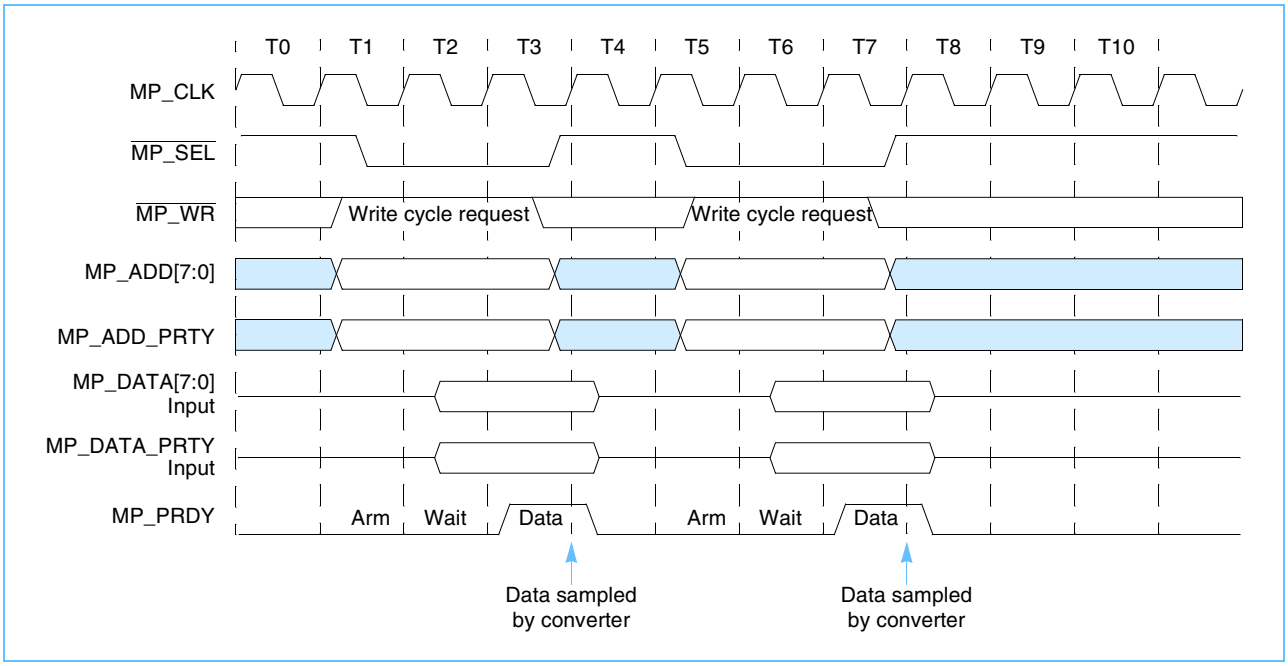


Figure 3-24. Processor Write Access in 8-Bit Byte Mode



Note: MP_SEL can be active one more cycle without affecting the processor access; however, the minimum deactivate time must remain two clock cycles. MP_PRDY is asserted high when data is valid (after stabilization for one clock cycle) on the bus (for read) or when data is written into the converter (for write). The data is sampled while the MP_PRDY signal is high.

4. Registers

This section defines all of the registers required for operating the converter.

- Registers are addressed from x‘00’ to x‘FF’.
- There are two ways to access the converter’s registers:
  - During the power-on reset (POR) procedure, some registers can be preset to start the system according to predetermined settings.
  - The register can be read or written through the microprocessor interface.
- Write access to a read-only register is not valid and does not change the value of that register.
- All errors are logged (not first failure data capture [FFDC]).
- All bits in all registers are active when set to ‘1’.
- Registers can be accessed in 8-bit (byte) mode, or in 32-bit (burst) mode through bursts of four 8-bit modes (for Intel i960® processors). In byte mode, the least significant byte (7:0) is sent in response to the lowest byte address, and the most significant byte (31:24) is sent in response to the highest byte address. In burst mode, the least significant byte is sent first, then the second least significant byte, and so forth (see Figure 4-1).
- The registers are based on little-endian notation (that is, the highest addressed byte is most significant).

Figure 4-1. Individual Register Mapping

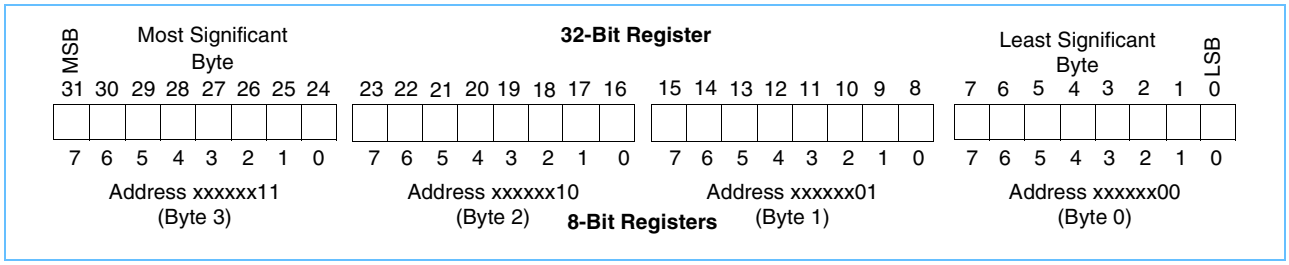
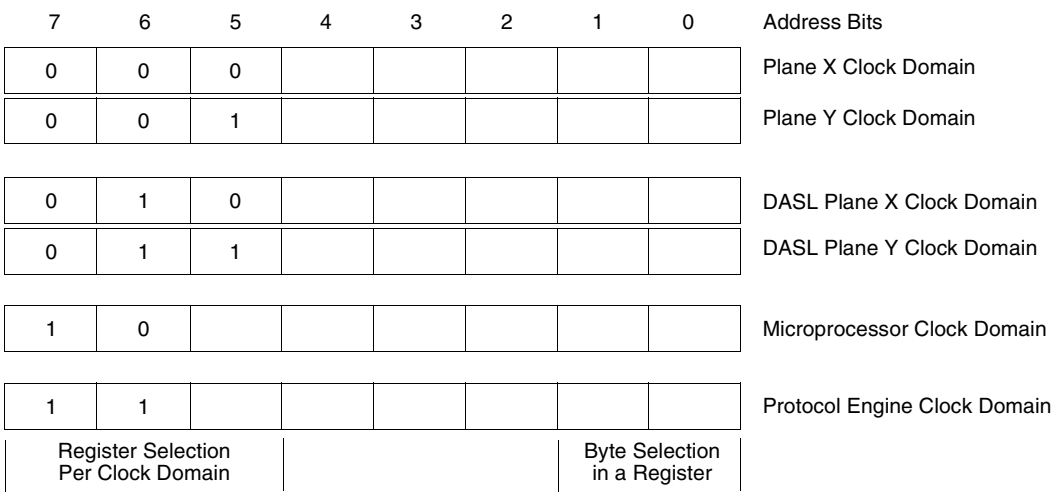


Figure 4-2 shows the direct correlation between the high-order address bit value and the register domain.

Figure 4-2. Register Addressing



4.1 Error Detection, Reporting, and Interrupt Registers

The converter uses a common strategy for error detection, error reporting, and interrupt generation:

- Each error is detected by an individual checker (e.g., the parity checker).
- An error must be individually enabled in the Checker Enable register to be reported into the corresponding Event register.
- An error must be individually enabled in the Interrupt Enable register to generate an interrupt.
- The Interrupt_Register_Indirection register is the first register to read when an interrupt is raised. The interrupt cause can be either present in the register itself or exist via an indirection to another Event register.
- For some specific errors (parity only), it is possible to either discard or not discard the corresponding packet, depending on the setting of the corresponding Setup_1_PATH register and the Ingress_PE_Interface register.

One recommended way of handling interrupts follows:

1. The processor reads the Interrupt_Register_Indirection register for the interrupt cause (either directly or indirectly via a second read into the Event register flagged by the Interrupt_Register_Indirection register).
2. After servicing the cause of the interrupt, the processor resets only the Event register. There are two ways to clear Event register bits:
   - One bit at time, by writing ‘1’ to the bit to be cleared. This method is intended for use in normal operation, because it does not clear events that occur while a prior event is being processed.
   - One byte at time, by writing x‘ff’ to the byte to be cleared (Event registers are considered to be four separate bytes). This method is intended for use when a global clear is needed (for example, to clear events that occur during chip initialization).

   Other techniques (such as writing zeroes or writing multiple bits in the same byte) have no effect.

Table 4-1. Register Map (Page 1 of 2)

Register Name	Addresses		Page
	Word Mode	Byte Mode	
Setup_1_X_PATH	x‘00’	x‘00’ to x‘03’	71
Setup_2_X_PATH	x‘04’	x‘04’ to x‘07’	73
Control_X_PATH	x‘08’	x‘08’ to x‘0B’	75
CRC_Error_Count_X	x‘0C’	x‘0C’ to x‘0F’	77
Event_1_X	x‘10’	x‘10’ to x‘13’	78
Event_1_Checker_Enable_X	x‘14’	x‘14’ to x‘17’	81
Interrupt_Enable_X	x‘18’	x‘18’ to x‘1B’	82
Setup_1_Y_PATH	x‘20’	x‘20’ to x‘23’	83
Setup_2_Y_PATH	x‘24’	x‘24’ to x‘27’	84
Control_Y_PATH	x‘28’	x‘28’ to x‘2B’	85
CRC_Error_Count_Y	x‘2C’	x‘2C’ to x‘2F’	88
Event_1_Y	x‘30’	x‘30’ to x‘33’	89
Event_1_Checker_Enable_Y	x‘34’	x‘34’ to x‘37’	91
Interrupt_Enable_Y	x‘38’	x‘38’ to x‘3B’	92
DASL_M3_Picocode_X	x‘40’	x‘40’ to x‘43’	93
SDC_Debug_CNTL_X	x‘44’	x‘44’ to x‘47’	95
SDC_Debug_Data_In_X	x‘48’	x‘48’ to x‘4B’	96
SDC_Debug_Data_Out_X	x‘4C’	x‘4C’ to x‘4F’	97
SDC_Debug_Data_Address_X	x‘50’	x‘50’ to x‘53’	97
SDC_Status_Reg_X	x‘54’	x‘54’ to x‘57’	98
DASL_M3_Picocode_Y	x‘60’	x‘60’ to x‘63’	99
SDC_Debug_CNTL_Y	x‘64’	x‘64’ to x‘67’	100
SDC_Debug_Data_In_Y	x‘68’	x‘68’ to x‘6B’	100
SDC_Debug_Data_Out_Y	x‘6C’	x‘6C’ to x‘6F’	101
SDC_Debug_Data_Address_Y	x‘70’	x‘70’ to x‘73’	101
SDC_Status_Reg_Y	x‘74’	x‘74’ to x‘77’	102
Event_2_Checker_Enable_X_and_Y	x‘80’	x‘80’ to x‘83’	103
Event_2_Interrupt_Enable_X_and_Y	x‘84’	x‘84’ to x‘87’	104
Event_2_X_and_Y	x‘88’	x‘88’ to x‘8B’	105
Test_Status_X_Y	x‘8C’	x‘8C’ to x‘8F’	107
Switch_X_PLL	x‘90’	x‘90’ to x‘93’	108
Switch_Y_PLL	x‘94’	x‘94’ to x‘97’	109
Chip_ID	x‘98’	x‘98’ to x‘9B’	110
PE_PLL	x‘9C’	x‘9C’ to x‘9F’	111
Common_Control	x‘A0’	x‘A0’ to x‘A3’	112

Table 4-1. Register Map (Page 2 of 2)

Register Name	Addresses		Page
	Word Mode	Byte Mode	
Interrupt_Register_Indirection	x‘A4’	x‘A4’ to x‘A7’	115
Ingress_PE_Interface	x‘C0’	x‘C0’ to x‘C3’	116
Egress_PE_Interface	x‘C4’	x‘C4’ to x‘C7’	118
PE_Common	x‘C8’	x‘C8’ to x‘CB’	120
PARITY_Error_count	x‘CC’	x‘CC’ to x‘CF’	122

4.2 Register Definitions

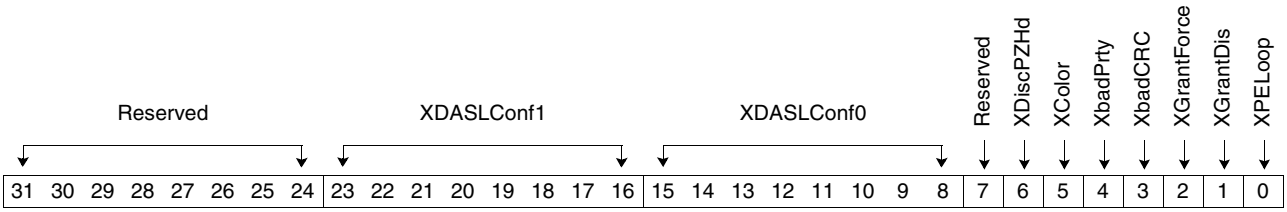
4.2.1 Setup_1_X_PATH Register

Reset Output Status x‘0000 0000’ (Power-On Reset, Software Reset Path X)

Address in Word Mode x‘00’

Address in Byte Mode x‘00’ to x‘03’

Access Type Read/Write



Bit(s)		Field Name	Description	Notes
Word Mode	Byte Mode			
31:24	7:0	Reserved	Reserved.	
23:16	7:0	XDASLConf1	DASL configuration register (physical subport = 32-bit port, unique hardware version number, synchronization mode). Configure to x‘07’.	1
15:8	7:0	XDASLConf0	DASL configuration register (physical subport, unique hardware version number ‘10001’, synchronization mode ‘1’). Configure to x‘89’.	1
7	7	Reserved	Reserved.	
6	6	XDiscPZHd	1 Does not discard PRS28.4G packets on the egress side that have a header parity error. 0 Discards packets.	
5	5	XColor	1 Forces red idle packets in PRS28.4G header to switch core. 0 Forces blue idle packets at IDI.	
4	4	XbadPrty	1 Forces a bad parity on idle packets in the PRS28.4G header to switch core. 0 Normal operation.	
3	3	XbadCRC	1 Forces a bad switch Cyclic Redundancy Check (CRC) insertion on ingress side. 0 Normal operation.	
2	2	XGrantForce	1 Forces output queue and memory grant to ‘1’ (always granted) during PE loopback to bypass flow control. 0 Normal operation (uses flow control).	
1	1	XGrantDis	1 Forces output queue and memory grant to ‘0’ (no grant) during PE loopback to block the flow. 0 Normal operation.	

1. See Section 5, Data-Aligned Synchronous Link (DASL), on page 123.

Bit(s)		Field Name	Description	Notes
Word Mode	Byte Mode			
0	0	XPELoop	1 PE interface loopback via path X logic. 0 No loopback.	

1. See Section 5, Data-Aligned Synchronous Link (DASL), on page 123.

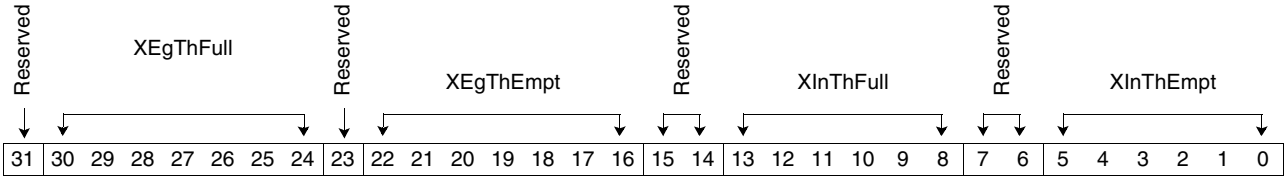
4.2.2 Setup_2_X_PATH Register

Reset Output Status x‘7807 3807’ (Power-On Reset, Software Reset Path X)

Address in Word Mode x‘04’

Address in Byte Mode x‘04’ to x‘07’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31	7	Reserved	Reserved.
30:24	6:0	XEgThFull	Egress FIFO almost full threshold (word). See programming examples below.
23	7	Reserved	Reserved.
22:16	6:0	XEgThEmpt	Egress FIFO almost empty threshold (word). See programming examples below.
15:14	7:6	Reserved	Reserved.
13:8	5:0	XInThFull	Ingress FIFO almost full threshold (word). See programming examples below.
7:6	7:6	Reserved	Reserved.
5:0	5:0	XInThEmpt	Ingress FIFO almost empty threshold (word). See programming examples below.

This register’s settings depend on the packet size, the PE clock, the switch clock, and the flow control mechanism in use.

Example 1: For a 64-byte packet and a PE and switch using the same range clock frequency, the setting might be:

- Ingress buffer with out-of-band flow control ($\overline{\text{RXENB}}$):
  - Almost empty: x‘10’ for a 16-word packet (packet of 64 bytes) or above to avoid underrun
  - Almost full: x‘2C’ or below to avoid overrun
- Egress buffer:
  - Almost empty: x‘10’ or above to avoid underrun
  - Almost full: x‘3D’ or below to avoid overrun

Example 2: For an 80-byte packet and a PE and switch clock at 110 MHz, the setting might be:

- Ingress buffer with out-of-band flow control ($\overline{\text{RXENB}}$):
  - Almost empty: x‘14’ for a 20-word packet (packet of 80 bytes) or above to avoid underrun
  - Almost full: x‘28’ or below to avoid overrun
- Egress buffer:
  - Almost empty: x‘14’ or above to avoid underrun
  - Almost full: x‘30’ or below to avoid overrun

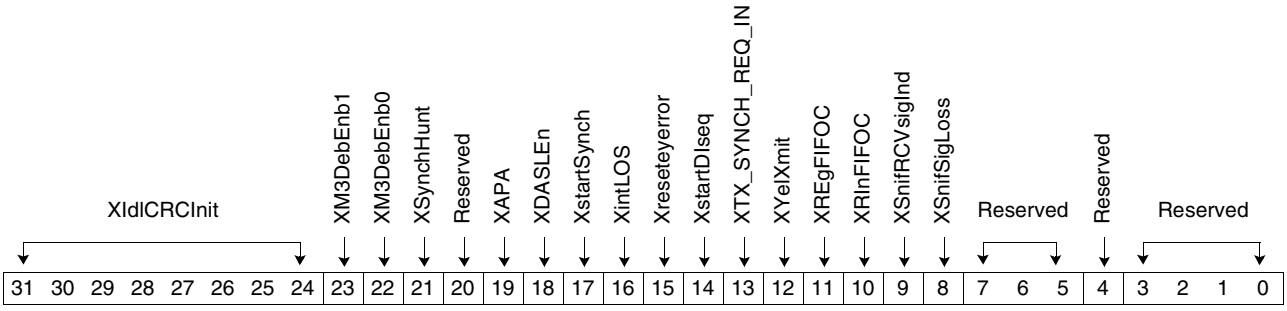
4.2.3 Control_X_PATH Register

Reset Output Status x‘0000 0C00’ (Power-On Reset, Software Reset Path X)

Address in Word Mode x‘08’

Address in Byte Mode x‘08’ to x‘0B’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	XIdlCRCInit	Initial frame check sequence (FCS) register value for idle packet CRC computation, ingress side (to match the LU size). LU LengthCRC Initial Register 16 x‘D0’ 17 x‘DD’ 18 x‘04’ 19 x‘FA’ 20 x‘07’
23	7	XM3DebEnb1	1 Enables DASL debug bus 1 (IBM reserved). 0 Disables DASL debug bus 1.
22	6	XM3DebEnb0	1 Enables DASL debug bus 2 (IBM reserved). 0 Disables DASL debug bus 2.
21	5	XSynchHunt	1 Starts receiver synchronization for bit/nibble/byte/packet alignment. 0 Stops the receiver synchronization process.
20	4	Reserved	Reserved.
19	3	XAPA	1 Indicates on APAN_X I/O that the port is not synchronized. 0 Indicates on APAN_X I/O that the port is fully synchronized.
18	2	XDASLEn	1 Enables DASL port operation for transmitter and receiver. 0 Disables DASL port operation.
17	1	XstartSynch	1 Starts transmission of ingress synchronization packets. 0 Stops transmission of ingress synchronization packets.
16	0	XintLOS	1 Enables DASL macro internal loss-of-signal (LOS) checker (IBM reserved). 0 Disables DASL macro internal LOS checker (normal operation).

Bit(s)		Field Name	Description
Word Mode	Byte Mode		
15	7	Xreseteyerror	1 Resets DASL *minimum eye* (see Section 12. , Glossary, on page 175) error detector (SDC port quality). See bit 6 of the Event_1_X register for error. 0 Normal operation.
14	6	XstartDIseq	1 Starts DASL interface sequencer (on during normal operation). This bit must be set for PE loopback. 0 Stops DASL interface sequencer.
13	5	XTX_SYNCH_REQ_IN	Must be written with a '1' for reset and then to a '0' to start the DASL transmitter. This action will emulate a pulse that resets the DASL transmitter-state machine.
12	4	XYelXmit	1 Tells IDI to send one yellow packet on the ingress path to the switch (must be reset [set to '0'] by software and rewritten afterwards to send the next yellow packet). 0 Normal operation.
11	3	XREgFIFOC	1 Resets egress FIFO counter (for debug purposes). 0 Normal operation.
10	2	XRInFIFOC	1 Resets ingress FIFO counter (for debug purposes). 0 Normal operation.
9	1	XSnifRCVsigInd	Sniffer in real time for the DASL receive data indicator. Reads the status (see bit 13 of the Event_1_X register). Used for debug purposes.
8	0	XSnifSigLoss	Sniffer in real time for DASL loss-of-signal detection. Reads the status (see bit 5 of the Event_1_X register). Used for debug purposes.
7:5	7:5	Reserved	Reserved.
4	4	Reserved	Reserved.
3:0	3:0	Reserved	Reserved.

4.2.4 X Plane Egress Parity and CRC_Error_Count_X Register

The microprocessor has the highest priority when writing to this register, so it may at any time overwrite the current value even if the counter is being incremented by an error source.

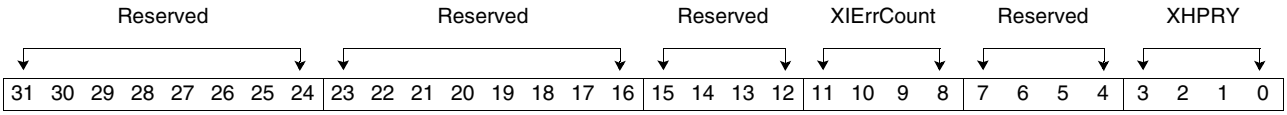
Note: The counters do not wrap around.

Reset Output Status x‘0000 0000’ (Power-On Reset, Software Reset Path X)

Address in Word Mode x‘0C’

Address in Byte Mode x‘0C’ to x‘0F’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	Reserved	Reserved.
23:16	7:0	Reserved	Reserved.
15:12	7:4	Reserved	Reserved.
11:8	3:0	XIErrCount	Switch egress idle packet CRC error counter. 0000 Reset
7:4	7:4	Reserved	Reserved.
3:0	3:0	XHPRY	PRS28.4G header parity error count (on egress from switch). 0000 Reset

4.2.5 X Plane Event 1 Register (Event_1_X)

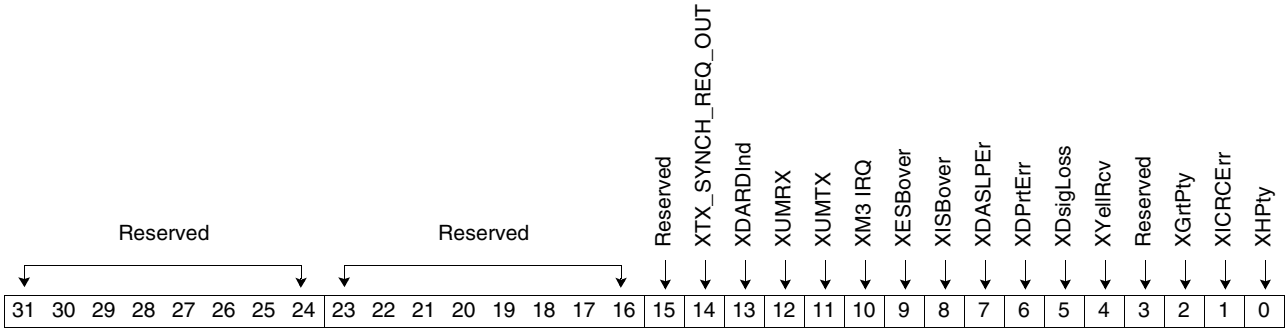
Note: For information about how to clear this register, see Section 4.1 , Error Detection, Reporting, and Interrupt Registers, on page 68.

Reset Output Status x‘0000 0000’ (Power-On Reset, Software Reset Path X)

Address in Word Mode x‘10’

Address in Byte Mode x‘10’ to x‘13’

Access Type Read/Write

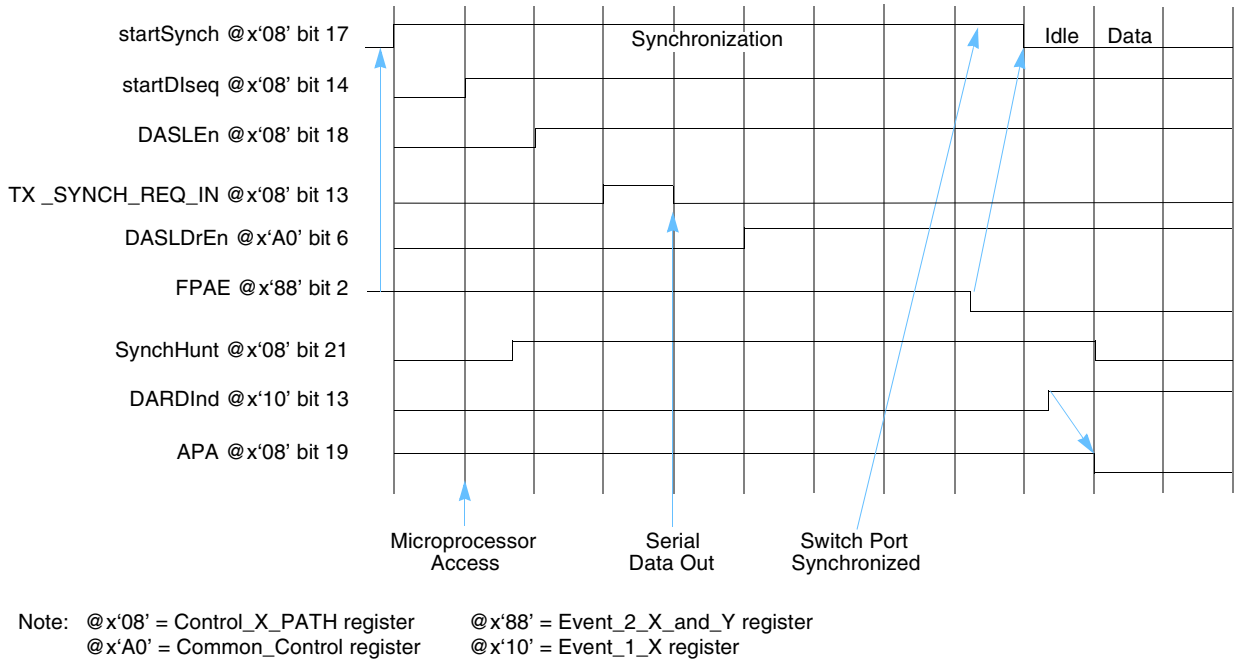


Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	Reserved	Reserved.
23:16	7:0	Reserved	Reserved.
15	7	Reserved	Reserved.
14	6	XTX_SYNCH_REQ_OUT	1 Transmits a synchronization request from the Shared DASL Controller (SDC) to observe the status of DASL (when the picocode needs to reset the DASL transmitter). 0 Normal operation.
13	5	XDARDInd	1 Indicates that the DASL receiver is synchronized and ready to receive data. Once determined, the microprocessor asserts Adapter Port Available (APA) at bit 19 of the Control_X_PATH register, which then informs the switch that converter synchronization has been completed, and the switch can stop sending synchronization packets. This bit remains set if DASL synchronization is maintained. 0 The DASL receiver is not synchronized.
12	4	XUMRX	1 At least one data packet has been sent by IDI to the switch (for debug purposes). 0 No data packet has been forwarded by IDI to the switch.
11	3	XUMTX	1 At least one data packet has been detected by EDI from the switch (for debug purposes). 0 No data packet has been detected by EDI.

Bit(s)		Field Name	Description
Word Mode	Byte Mode		
10	2	XM3 IRQ	1 SDC Interrupt Request. This bit indicates that a parity error has occurred during the transfer between the SDC and the instruction or data store, and remains on as long as the condition is present and the DASL is not reset. 0 SDC operation is error free.
9	1	XESBover	1 Egress Buffer Overrun. Set when the X egress buffer has sent more data than the FIFO can hold. In this event, all excess packets are discarded, and reinitialization of the device is required. 0 No buffer overrun (normal operation).
8	0	XISBover	1 Ingress Buffer Overrun. Set when the X ingress buffer has received more data than the FIFO can hold. In this event, all excess packets are discarded, and reinitialization of the device is required. 0 No buffer overrun (normal operation).
7	7	XDASLPEr	1 DASL Port Error. Returned when there is an error during port processing by the picocode. Remains on as long as the condition is present. 0 Port is synchronized and is not experiencing error.
6	6	XDPrtErr	1 DASL Eye Error. Returned when a port cannot be synchronized because the *minimum eye* (see Section 12. , Glossary, on page 175) criteria is not met. Remains on as long as the condition persists and bit 15 of the Control_X_PATH register is not activated. 0 No eye error (receiver eye is wide open).
5	5	XDsigLoss	1 DASL Loss of Signal. Remains on as long as the condition is present. 0 DASL receiver detects a valid signal.
4	4	XYellRcv	1 EDI has detected a yellow packet from the switch. This is an event, not a status, so the bit must be cleared before it can indicate the reception of a new yellow packet. 0 No yellow packet has been detected by EDI since this bit was last cleared.
3	3	Reserved	Reserved.
2	2	XGrtPty	1 Output queue grant flywheel counter is desynchronized. 0 Output queue grant flywheel counter is synchronized.
1	1	XICRCErr	1 LU CRC error has been detected in idle packet from switch (EDI). This is an event, not a status, so the bit must be cleared before it can indicate the detection of a new CRC error. 0 No LU CRC error has been detected since this bit was last cleared.
0	0	XHPty	1 Parity error has been detected on switch header on egress side (EDI). This is an event, not a status, so the bit must be cleared before it can indicate the detection of a new parity error. 0 No switch header parity error has been detected since this bit was last cleared.

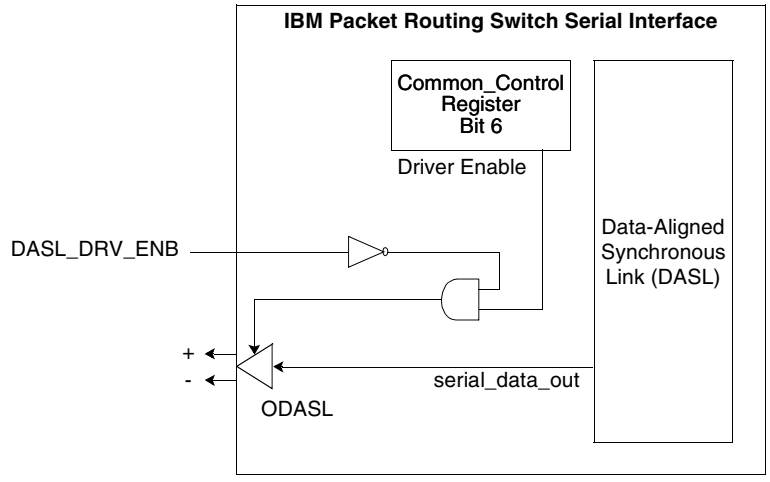
Figure 4-3 shows the timing of the interaction among the four registers required to activate a data-aligned synchronous link (DASL).

Figure 4-3. DASL Interface and DASL Startup Sequence Path X



Both internal enabling (bit 6 of the Common_Control register) and external enabling (DASL_DRV_ENB pin) are required to enable the DASL macro (see Figure 4-4).

Figure 4-4. Enabling of DASL Data Transmission and Reception Path X



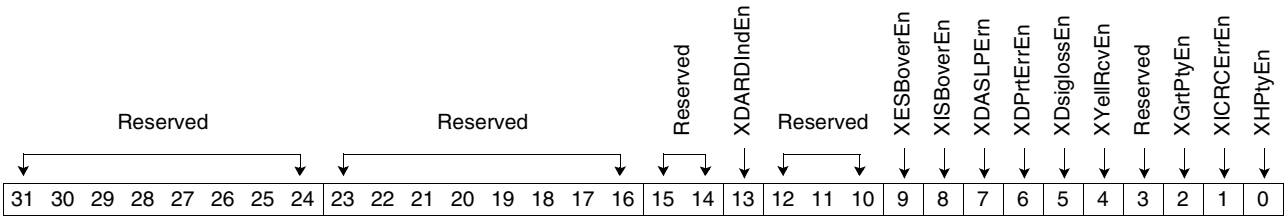
4.2.6 X Plane Event 1 Checker Enable Register (Event_1_Checker_Enable_X)

Reset Output Status x‘0000 0000’ (Power-On Reset, Software Reset Path X)

Address in Word Mode x‘14’

Address in Byte Mode x‘14’ to x‘17’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	Reserved	Reserved.
23:16	7:0	Reserved	Reserved.
15:14	7:6	Reserved	Reserved.
13	5	XDARDIndEn	When set to ‘1’, enables the DASL receive data indicator.
12:10	4:2	Reserved	Reserved.
9	1	XESBoverEn	When set to ‘1’, enables the egress buffer overrun checker.
8	0	XISBoverEn	When set to ‘1’, enables the ingress buffer overrun checker.
7	7	XDASLPErn	When set to ‘1’, enables the DASL port in error.
6	6	XDPrtErrEn	When set to ‘1’, enables the egress DASL interface minimum eye error flag.
5	5	XDsiglossEn	When set to ‘1’, enables the DASL loss-of-signal detection flag (bit 16 of the Control_X_PATH register must be set to ‘1’).
4	4	XYellRcvEn	When set to ‘1’, enables the egress yellow packet reception checker.
3	3	Reserved	Reserved.
2	2	XGrtPtyEn	When set to ‘1’, enables the egress grant priority error flag checker.
1	1	XICRCErrEn	When set to ‘1’, enables the egress PRS28.4G idle packet CRC error checker.
0	0	XHPtyEn	When set to ‘1’, enables the egress PRS28.4G header 0 parity error flag checker.

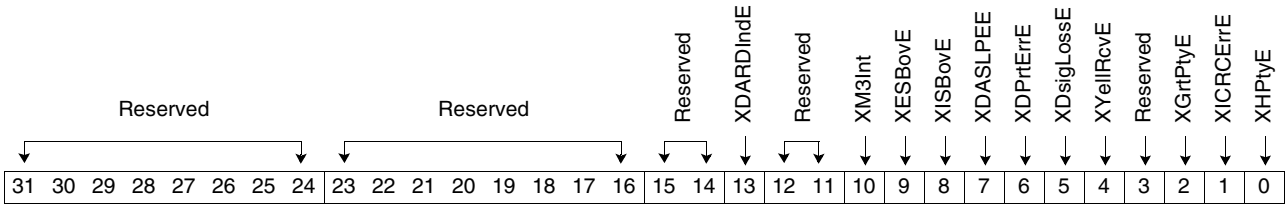
4.2.7 Interrupt_Enable_X Register

Reset Output Status x‘0000 0000’ (Power-On Reset, Software Reset Path X)

Address in Word Mode x‘18’

Address in Byte Mode x‘18’ to x‘1B’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	Reserved	Reserved.
23:16	7:0	Reserved	Reserved.
15:14	7:6	Reserved	Reserved.
13	5	XDARDIndE	When set to ‘1’, enables the DASL receive data indicator interrupt.
12:11	4:3	Reserved	Reserved.
10	2	XM3Int	When set to ‘1’, enables the M3 interrupt.
9	1	XESBovE	When set to ‘1’, enables the egress buffer overrun interrupt.
8	0	XISBovE	When set to ‘1’, enables the ingress buffer overrun interrupt.
7	7	XDASLPEE	When set to ‘1’, enables the DASL port in error interrupt.
6	6	XDPrtErrE	When set to ‘1’, enables the egress DASL interface minimum eye error flag interrupt.
5	5	XDsigLossE	When set to ‘1’, enables the DASL loss-of-signal detection interrupt.
4	4	XYellRcvE	When set to ‘1’, enables the egress yellow packet reception interrupt.
3	3	Reserved	Reserved.
2	2	XGrtPtyE	When set to ‘1’, enables the egress grant priority error flag interrupt.
1	1	XICRCErrE	When set to ‘1’, enables the egress PRS28.4G idle packet CRC error interrupt.
0	0	XHPtyE	When set to ‘1’, enables the egress PRS28.4G header 0 parity error flag interrupt.

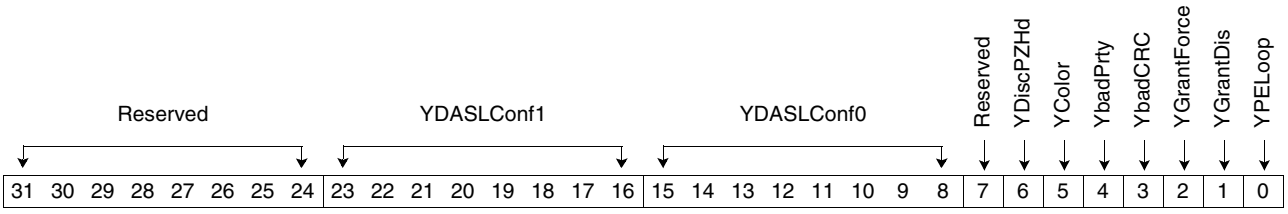
4.2.8 Setup_1_Y_PATH Register

Reset Output Status x‘0000 0000’ (Power-On Reset, Software Reset Path Y)

Address in Word Mode x‘20’

Address in Byte Mode x‘20’ to x‘23’

Access Type Read/Write



Bit(s)		Field Name	Description	Notes
Word Mode	Byte Mode			
31:24	7:0	Reserved	Reserved.	
23:16	7:0	YDASLConf1	DASL configuration 1 register (physical subport = 32-bit port, unique hardware version number, synchronization mode). Configure to x‘07’.	1
15:8	7:0	YDASLConf0	DASL configuration 0 register (physical subport, unique hardware version number = ‘10001’, synchronization mode = ‘1’). Configure to x‘89’.	1
7	7	Reserved	Reserved.	
6	6	YDiscPZHd	1 Does not discard PRS28.4G packets on the egress side that have a header parity error. 0 Discards packets.	
5	5	YColor	1 Forces red idle packets in PRS28.4G header to switch core. 0 Forces blue idle packets at IDI.	
4	4	YbadPrty	1 Forces a bad parity on idle packets in the PRS28.4G header to switch core. 0 Normal operation.	
3	3	YbadCRC	1 Forces a bad switch CRC insertion on ingress side. 0 Normal operation.	
2	2	YGrantForce	1 Forces output queue and memory grant to ‘1’ (always granted) during PE loopback to bypass flow control. 0 Normal operation (uses flow control).	
1	1	YGrantDis	1 Forces output queue and memory grant to ‘0’ (no grant) during PE Loopback to block the flow. 0 Normal operation.	
0	0	YPELoop	1 PE interface loopback via path Y logic. 0 Normal operation.	

1. See Section 5, Data-Aligned Synchronous Link (DASL), on page 123.

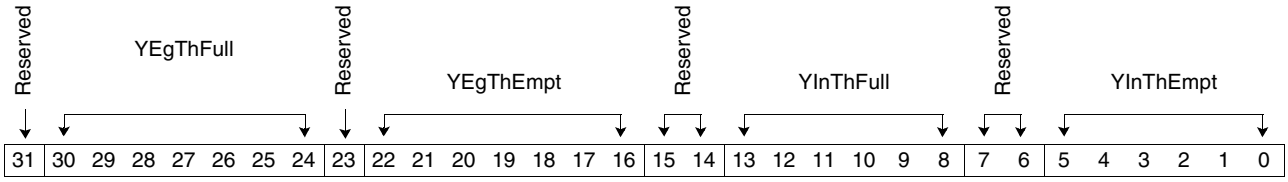
4.2.9 Setup_2_Y_PATH Registers

Reset Output Status x‘7807 3807’ (Power-On Reset, Software Reset Path Y)

Address in Word Mode x‘24’

Address in Byte Mode x‘24’ to x‘27’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31	7	Reserved	Reserved.
30:24	6:0	YEgThFull	Egress FIFO almost full threshold (word).
23	7	Reserved	Reserved.
22:16	6:0	YEgThEmpt	Egress FIFO almost empty threshold (word).
15:14	7:6	Reserved	Reserved.
13:8	5:0	YInThFull	Ingress FIFO almost full threshold (word).
7:6	7:6	Reserved	Reserved.
5:0	5:0	YInThEmpt	Ingress FIFO almost empty threshold (word).

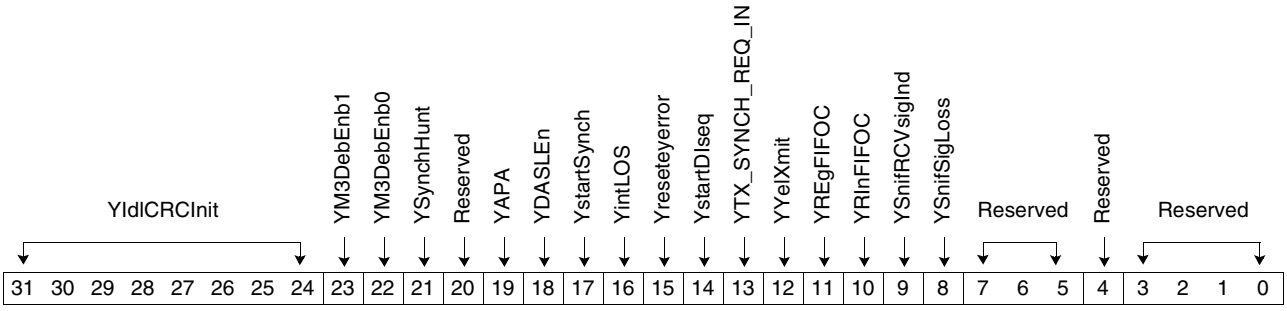
4.2.10 Control_Y_PATH Register

Reset Output Status x‘0000 0C00’ (Power-On Reset, Software Reset Path Y)

Address in Word Mode x‘28’

Address in Byte Mode x‘28’ to x‘2B’

Access Type Read/Write

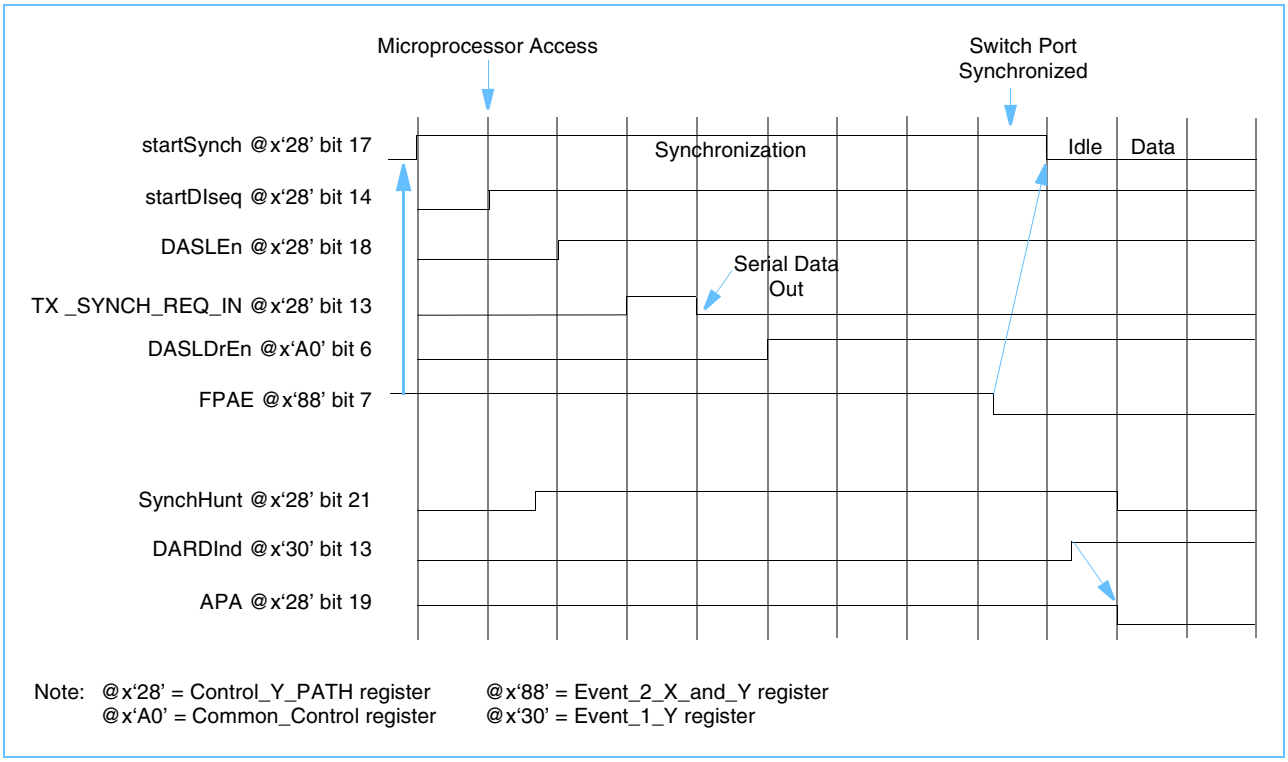


Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	YIdlCRCInit	Initial FCS register value for idle packet CRC computation, ingress side. LU LengthCRC Initial Register 16 x‘D0’ 17 x‘DD’ 18 x‘04’ 19 x‘FA’ 20 x‘07’
23	7	YM3DebEnb1	1 Enables DASL debug bus 1 (IBM reserved). 0 Disables DASL debug bus 1.
22	6	YM3DebEnb0	1 Enables DASL debug bus 2 (IBM reserved). 0 Disables DASL debug bus 2.
21	5	YSynchHunt	1 Starts receiver synchronization for bit/nibble/byte/packet alignment. 0 Stops the receiver synchronization process.
20	4	Reserved	Reserved.
19	3	YAPA	1 Indicates on APAN_X I/O that the port is not synchronized. 0 Indicates on APAN_X I/O that the port is fully synchronized.
18	2	YDASLEn	1 Enables DASL port operation for transmitter and receiver. 0 Disables DASL port operation.
17	1	YstartSynch	1 Starts transmission of ingress synchronization packets. 0 Stops transmission of ingress synchronization packets.
16	0	YintLOS	1 Enables DASL macro internal Loss-Of-Signal (LOS) checker. 0 Disables DASL macro internal LOS checker.

Bit(s)		Field Name	Description
Word Mode	Byte Mode		
15	7	Yreseteyerror	1 Resets DASL minimum eye error detector. See bit 6 of the Event_1_Y register for error. 0 Normal operation.
14	6	YstartDIseq	1 Starts DASL interface sequencer (on during normal operation). 0 Stops DASL interface sequencer.
13	5	YTX_SYNCH_REQ_IN	Must be written with a '1' for reset and then to a '0' to start the DASL transmitter. This action will emulate a pulse that resets the DASL transmitter-state machine.
12	4	YYelXmit	1 Tells the Ingress DASL Interface (IDI) to send one yellow packet on the ingress path to the switch (must be reset [set to '0'] by software and rewritten afterwards to send the next yellow packet). 0 Normal operation.
11	3	YREgFIFOC	1 Resets egress FIFO counter (for debug purposes). 0 Normal operation.
10	2	YRInFIFOC	1 Resets ingress FIFO counter (for debug purposes). 0 Normal operation.
9	1	YSnifRCVsigInd	Sniffer in real time for the DASL receive data indicator. Reads the status (see bit 13 of the Event_1_Y register). Used for debug purposes.
8	0	YSnifSigLoss	Sniffer in real time for DASL loss-of-signal detection. Reads the status (see bit 5 of the Event_1_Y register). Used for debug purposes.
7:5	7:5	Reserved	Reserved.
4	4	Reserved	Reserved.
3:0	3:0	Reserved	Reserved.

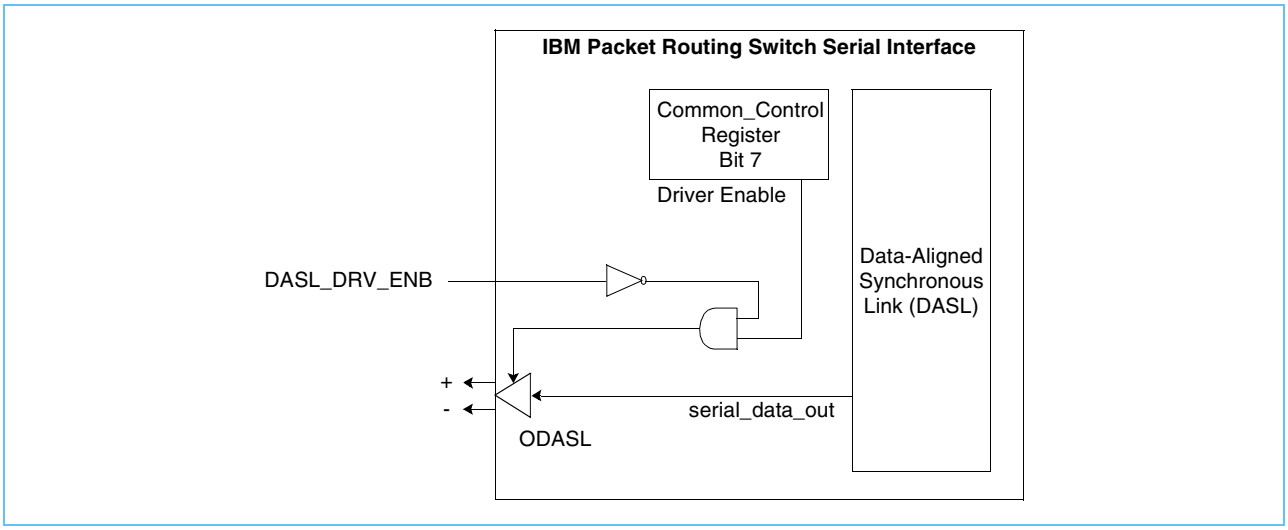
Figure 4-5 shows the timing of the interaction among the four registers required to activate a data-aligned synchronous link (DASL).

Figure 4-5. DASL Interface and DASL Startup Sequence Path Y



Both internal enabling (bit 6 of the Common_Control register) and external enabling (DASL_DRV_ENB pin) are required to enable the DASL macro (see Figure 4-6).

Figure 4-6. Enabling of DASL Data Transmission and Reception Path Y



4.2.11 Y Plane Egress Parity and CRC_Error_Count_Y Register

The microprocessor has the highest priority when writing into this register, so it may at any time overwrite the current value even if the counter is being incremented by the source of an error.

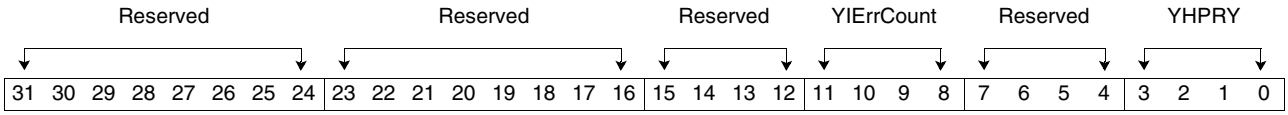
Note: All of the counters do not wrap around.

Reset Output Status x‘0000 0000’ (Power-On Reset, Software Reset Path Y)

Address in Word Mode x‘2C’

Address in Byte Mode x‘2C’ to x‘2F’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	Reserved	Reserved.
23:16	7:0	Reserved	Reserved.
15:12	7:4	Reserved	Reserved.
11:8	3:0	YIErrCount	Switch egress idle packet CRC error counter. 0 Reset
7:4	7:4	Reserved	Reserved.
3:0	3:0	YHPRY	PRS28.4G header parity error count (on egress from switch). 0 Reset

4.2.12 Y Plane Event 1 Register (Event_1_Y)

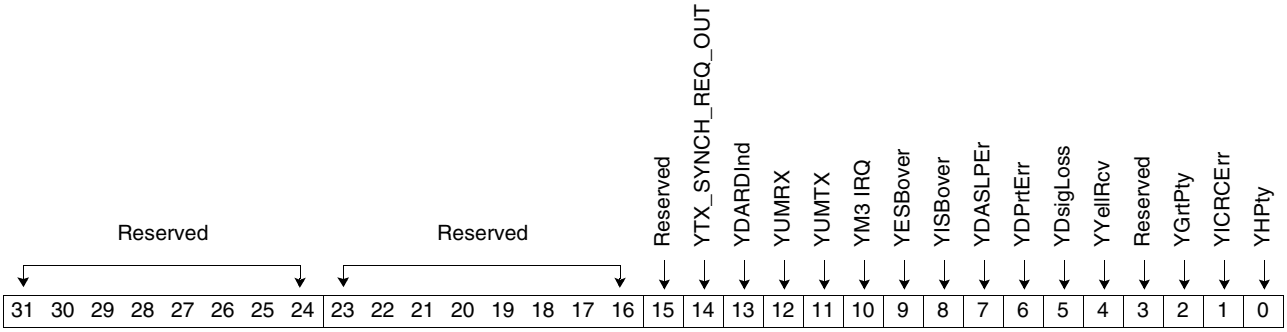
Note: For information about how to clear this register, see Section 4.1 , Error Detection, Reporting, and Interrupt Registers, on page 68.

Reset Output Status x‘0000 0000’ (Power-On Reset, Software Reset Path Y)

Address in Word Mode x‘30’

Address in Byte Mode x‘30’ to x‘33’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	Reserved	Reserved.
23:16	7:0	Reserved	Reserved.
15	7	Reserved	Reserved.
14	6	YTX_SYNCH_REQ_OUT	1 Transmits a synchronization request from the SDC to observe the status of DASL (when the picocode needs to reset the DASL transmitter). 0 Normal operation.
13	5	YDARDInd	1 Indicates that the DASL receiver is synchronized and ready to receive data. Once determined, the microprocessor asserts Adapter Port Available (APA) at bit 19 of the Event_1_Y register, which then informs the switch that converter synchronization has been completed, and the switch can stop sending synchronization packets. This bit remains set if DASL synchronization is maintained. 0 The DASL receiver is not synchronized.
12	4	YUMRX	1 At least one data packet has been sent by IDI to the switch (for debug purposes). 0 No data packet has been forwarded by IDI to the switch.
11	3	YUMTX	1 At least one data packet has been detected by EDI from the switch (for debug purposes). 0 No data packet has been detected by EDI.

Bit(s)		Field Name	Description
Word Mode	Byte Mode		
10	2	YM3 IRQ	1 SDC Interrupt Request. This bit indicates that a parity error has occurred during the transfer between the SDC and the instruction or data store, and remains on as long as the condition is present and the DASL is not reset. 0 SDC operation is error free.
9	1	YESBover	1 Egress Buffer Overrun. Set when the Y egress buffer has sent more data than the FIFO can hold. In this event, all excess packets are discarded, and reinitialization of the device is required. 0 No buffer overrun (normal operation).
8	0	YISBover	1 Ingress Buffer Overrun. Set when the Y ingress buffer has received more data than the FIFO can hold. In this event, all excess packets are discarded, and reinitialization of the device is required. 0 No buffer overrun (normal operation).
7	7	YDASLPEr	1 DASL Port Error. Returned when there is an error during port processing by the picocode. Remains on as long as the condition is present. 0 Port is synchronized and is not experiencing error.
6	6	YDPrtErr	1 DASL Eye Error. Returned when a port cannot be synchronized because the *minimum eye* (see Section 12. , Glossary, on page 175) criteria is not met. Remains on as long as the condition persists and bit 15 of the Control_X_PATH register is not activated. 0 No eye error (receiver eye is wide open).
5	5	YDsigLoss	1 DASL Loss of Signal. Remains on as long as the condition is present. 0 DASL receiver detects a valid signal.
4	4	YYellRcv	1 EDI has detected a yellow packet from the switch. This is an event, not a status, so the bit must be cleared before it can indicate the reception of a new yellow packet. 0 No yellow packet has been detected by EDI since this bit was last cleared.
3	3	Reserved	Reserved.
2	2	YGrtPty	1 Output queue grant flywheel counter is desynchronized. 0 Output queue grant flywheel counter is synchronized.
1	1	YICRCErr	1 LU CRC error has been detected in idle packet from switch (EDI). This is an event, not a status, so the bit must be cleared before it can indicate the detection of a new CRC error. 0 No LU CRC error has been detected since this bit was last cleared.
0	0	YHPty	1 Parity error has been detected on switch header on egress side (EDI). This is an event, not a status, so the bit must be cleared before it can indicate the detection of a new parity error. 0 No switch header parity error has been detected since this bit was last cleared.

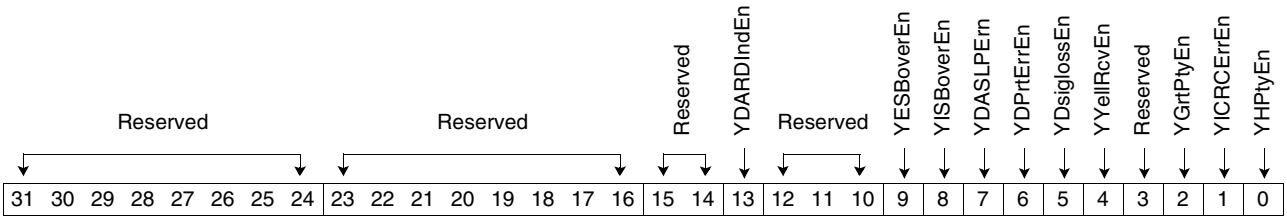
4.2.13 Y Plane Event 1 Checker Enable Register (Event_1_Checker_Enable_Y)

Reset Output Status x‘0000 0000’ (Power-On Reset, Software Reset Path Y)

Address in Word Mode x‘34’

Address in Byte Mode x‘34’ to x‘37’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	Reserved	Reserved.
23:16	7:0	Reserved	Reserved.
15:14	7:6	Reserved	Reserved.
13	5	YDARDIndEn	When set to ‘1’, enables the DASL receive data indicator.
12:10	4:2	Reserved	Reserved.
9	1	YESBoverEn	When set to ‘1’, enables the egress buffer overrun checker.
8	0	YISBoverEn	When set to ‘1’, enables the ingress buffer overrun checker.
7	7	YDASLPErn	When set to ‘1’, enables the DASL port in error.
6	6	YDPrtErrEn	When set to ‘1’, enables the egress DASL interface minimum eye error flag.
5	5	YDsiglossEn	When set to ‘1’, enables the DASL loss-of-signal detection flag (bit 16 of the Control_Y_PATH register must be set to ‘1’).
4	4	YYellRcvEn	When set to ‘1’, enables the egress yellow packet reception checker.
3	3	Reserved	Reserved.
2	2	YGrtPtyEn	When set to ‘1’, enables the egress grant priority error flag checker.
1	1	YICRCErrEn	When set to ‘1’, enables the egress PRS28.4G idle packet CRC error checker.
0	0	YHPtyEn	When set to ‘1’, enables the egress PRS28.4G header 0 parity error flag checker.

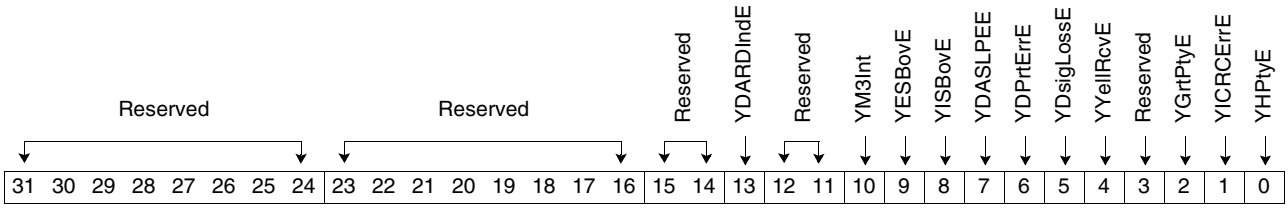
4.2.14 Interrupt_Enable_Y Register

Reset Output Status x‘0000 0000’ (Power-On Reset, Software Reset Path Y)

Address in Word Mode x‘38’

Address in Byte Mode x‘38’ to x‘3B’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	Reserved	Reserved.
23:16	7:0	Reserved	Reserved.
15:14	7:6	Reserved	Reserved.
13	5	YDARDIndE	When set to ‘1’, enables the DASL receive data indicator interrupt.
12:11	4:3	Reserved	Reserved.
10	2	YM3Int	When set to ‘1’, enables the M3 interrupt.
9	1	YESBovE	When set to ‘1’, enables the egress buffer overrun interrupt.
8	0	YISBovE	When set to ‘1’, enables the ingress buffer overrun interrupt.
7	7	YDASLPEE	When set to ‘1’, enables the DASL port in error interrupt.
6	6	YDPrtErrE	When set to ‘1’, enables the egress DASL interface minimum eye error flag interrupt.
5	5	YDsigLossE	When set to ‘1’, enables the DASL loss-of-signal detection interrupt.
4	4	YYellRcvE	When set to ‘1’, enables the egress yellow packet reception interrupt.
3	3	Reserved	Reserved.
2	2	YGrtPtyE	When set to ‘1’, enables the egress grant priority error flag interrupt.
1	1	YICRCErrE	When set to ‘1’, enables the egress PRS28.4G idle packet CRC error interrupt.
0	0	YHPtyE	When set to ‘1’, enables the egress PRS28.4G header 0 parity error flag interrupt.

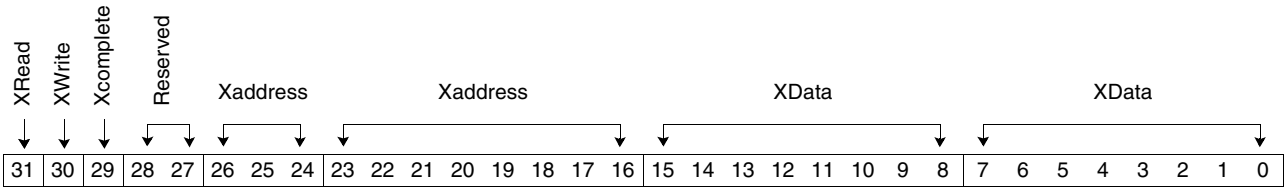
4.2.15 DASL_M3_Picocode_X Register

Reset Output Status x‘0000 0000’ (Power-On Reset, DASL Path X Reset, SDC Path X Reset)

Address in Word Mode x‘40’

Address in Byte Mode x‘40’ to x‘43’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31	7	XRead	Read enable. Does not reset by itself.
30	6	XWrite	Write enable.
29	5	Xcomplete	Read instruction complete flag (acknowledge). Must be reset after completion.
28:27	4:3	Reserved	Reserved.
26:16	2:0	Xaddress	The following table gives the mapping between bits 26:16 of this register, the bit locations in the picocode, and the DASL hardware bit ordering for each entity: MSB LSB This register26 16 Picocode10 0 DASL hardware0 10
	7:0	Xaddress	
15:8	7:0	XData	M3 read/write data.
7:0	7:0	XData	M3 read/write data.

Read and Write Operations

The read operation is performed as follows:

1. Set the address byte in the DASL_M3_Picocode_X register (x‘42’).
2. Set the remaining address byte and bit 31 in the register (x‘43’).
3. Poll bit 29 of the register (x‘43’) for read completion. Read valid data from the register (x‘40’ and x‘41’).
4. Reset read enable, bit 31 of the register (x‘43’), and read the complete bit by writing ‘0’ in bits 29 and 31.

The write operation is performed as follows:

1. Set the data byte in the DASL_M3_Picocode_X register (x‘40’).
2. Set the data byte in the register (x‘41’).
3. Set the address in the register (x‘42’).
4. Set the remaining bits of the address and bit 30 in the register (x‘43’) to issue the write operation.
5. Reset bit 30 in the register (x‘43’).

Repeat the above operational sequence as long as there is data to be loaded in the DASL. Bit 30 does not need to be reset between two successive write operations. For example, in the picocode file, the syntax in cmd file: WRITE (ADDRESS ≥ x‘40’, DATA ≥ x‘4000 900F’) means, at address x‘40’, write according to the x‘4000 900F’ pattern, where x‘4’ means write enable, x‘000’ is the start address, and x‘900F’ is the data pattern to write.

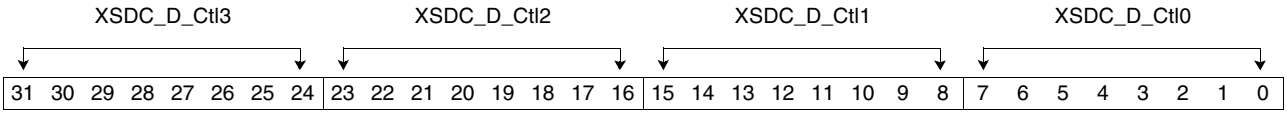
4.2.16 SDC Controller X Register (SDC_Debug_CNTL_X)

Reset Output Status x‘0000 0000’ (Power-On Reset, DASL Path X Reset, SDC Path X Reset)

Address in Word Mode x‘44’

Address in Byte Mode x‘44’ to x‘47’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	XSDC_D_Ctl3	Bit 31 (R/W): debug function trigger. Must be set to ‘1’ to trigger the operation defined in the debug_operation_select field (bits 19:16). Bit 31 is automatically reset when the operation is completed. Bits 30:24 (R/W): IBM reserved.
23:16	7:0	XSDC_D_Ctl2	Bits 23:20 (R/W): IBM reserved. Bits 19:16 (R/W): debug_operation_select. 0000 No operation. 0001 32-bit read request at the address given by the Debug_Data_Address Register. 0010 32-bit write request at the address given by the Debug_Data_Address Register. Others: IBM reserved.
15:8	7:0	XSDC_D_Ctl1	IBM reserved.
7:0	7:0	XSDC_D_Ctl0	Status Count Input. Function used for M3 keep alive checking. The value written into this field is incremented by one if the M3 picoprocessor works properly. The result is available in the SDC_ Status_Reg register, bits 7:0.

SDC_Debug_CNTL Register Purpose

The SDC_Debug_CNTL register must be used to access internal M3 resources (like the DASL local store). For all operations (except usage of the M3 keep alive counter), bit 31 (MSB) of the SDC_Debug_CNTL register must be set to ‘1’ to start the command that the picocode will perform using the debug_operation_select field (bits 19:16). Bit 31 of the SDC_Debug_CNTL register is reset when the operation is completed. The SDC_Debug_CNTL register is mainly used to give commands to the SDC. The SDC address and SDC data registers are used to pass address and data parameters, respectively, to the SDC command specified by the debug_operation_select field.

M3 Keep Alive Feature

To check the M3 picoprocessor, write a data byte value in bits 7:0 of the SDC_Debug_CNTL register and read bits 7:0 of the SDC_ Status_Reg register. Confirm that the data byte value is incremented by one. If the data byte value is not incremented by one, the M3 picoprocessor is not working properly.

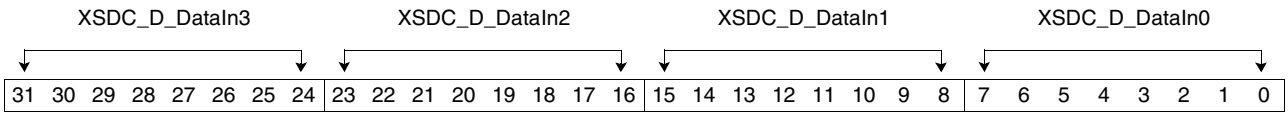
4.2.17 SDC Data In X Bus Register (SDC_Debug_Data_In_X)

Reset Output Status x‘0000 0000’ (Power-On Reset, DASL Path X Reset, SDC Path X Reset)

Address in Word Mode x‘48’

Address in Byte Mode x‘48’ to x‘4B’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	XSDC_D_DataIn3	Debug bus data in.
23:16	7:0	XSDC_D_DataIn2	Debug bus data in.
15:8	7:0	XSDC_D_DataIn1	Debug bus data in.
7:0	7:0	XSDC_D_DataIn0	Debug bus data in.

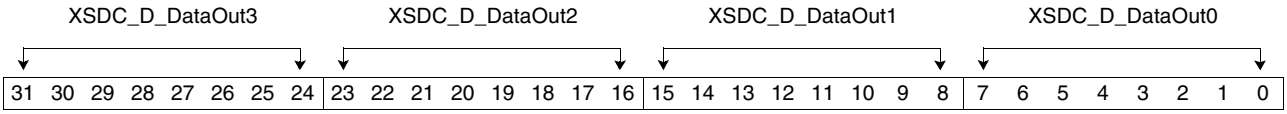
4.2.18 SDC Data Out X Bus Register (SDC_Debug_Data_Out_X)

Reset Output Status x‘0000 0000’ (Power-On Reset, DASL Path X Reset, SDC Path X Reset)

Address in Word Mode x‘4C’

Address in Byte Mode x‘4C’ to x‘4F’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	XSDC_D_DataOut3	Debug bus data out.
23:16	7:0	XSDC_D_DataOut2	Debug bus data out.
15:8	7:0	XSDC_D_DataOut1	Debug bus data out.
7:0	7:0	XSDC_D_DataOut0	Debug bus data out.

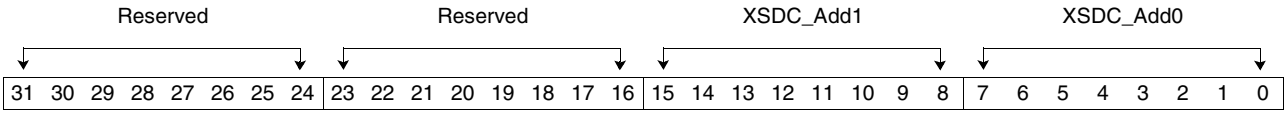
4.2.19 SDC Address X Bus Register (SDC_Debug_Data_Address_X)

Reset Output Status x‘0000 0000’ (Power-On Reset, DASL Path X Reset, SDC Path X Reset)

Address in Word Mode x‘50’

Address in Byte Mode x‘50’ to x‘53’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	Reserved	Reserved.
23:16	7:0	Reserved	Reserved.
15:8	7:0	XSDC_Add1	Debug bus address.
7:0	7:0	XSDC_Add0	Debug bus address.

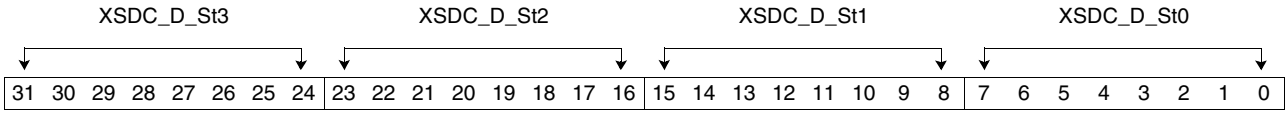
4.2.20 SDC Status X Register (SDC_Status_Reg_X)

Reset Output Status x‘0000 0000’ (Power-On Reset, DASL Path X Reset, SDC Path X Reset)

Address in Word Mode x‘54’

Address in Byte Mode x‘54’ to x‘57’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	XSDC_D_St3	DASL control code version.
23:16	7:0	XSDC_D_St2	DASL control code revision.
15:8	7:0	XSDC_D_St1	IBM reserved.
7:0	7:0	XSDC_D_St0	Status Count Output. This is the result of the M3 keep alive function triggered in the SDC_Status_Reg register.

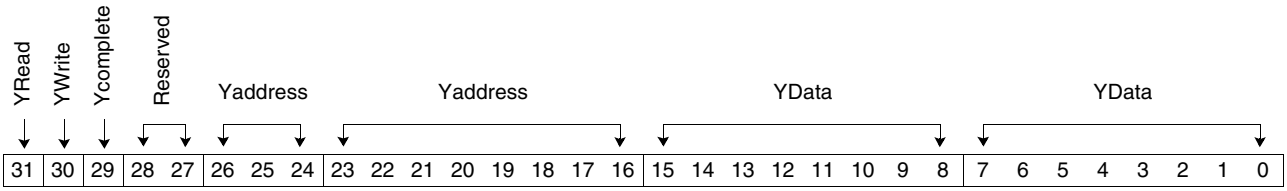
4.2.21 DASL_M3_Picocode_Y Register

Reset Output Status x‘0000 0000’ (Power-On Reset, DASL Path Y Reset, SDC Path Y Reset)

Address in Word Mode x‘60’

Address in Byte Mode x‘60’ to x‘63’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31	7	YRead	Read enable. Does not reset by itself.
30	6	YWrite	Write enable.
29	5	Ycomplete	Read instruction complete flag. Must be reset after completion.
28:27	4	Reserved	Reserved.
26:24	3:0	Yaddress	The following table gives the mapping between bits 26:16 of this register, the bit locations in the picocode, and the DASL hardware bit ordering for each entity: MSB LSB This register26 16 Picocode10 0 DASL hardware0 10
23:16	7:0	Yaddress	
15:8	7:0	YData	M3 read/write data.
7:0	7:0	YData	M3 read/write data.

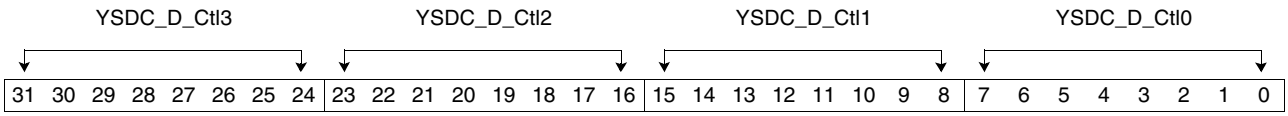
4.2.22 SDC Controller Y Register (SDC_Debug_CNTL_Y)

Reset Output Status x‘0000 0000’ (Power-On Reset, DASL Path Y Reset, SDC Path Y Reset)

Address in Word Mode x‘64’

Address in Byte Mode x‘64’ to x‘67’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	YSDC_D_Ctl3	Debug bus control.
23:16	7:0	YSDC_D_Ctl2	Debug bus control.
15:8	7:0	YSDC_D_Ctl1	Debug bus control.
7:0	7:0	YSDC_D_Ctl0	Debug bus control.

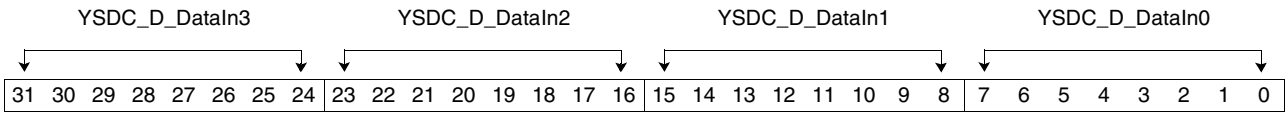
4.2.23 SDC Data In Y Bus Register (SDC_Debug_Data_In_Y)

Reset Output Status x‘0000 0000’ (Power-On Reset, DASL Path Y Reset, SDC Path Y Reset)

Address in Word Mode x‘68’

Address in Byte Mode x‘68’ to x‘6B’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	YSDC_D_DataIn3	Debug bus data in.
23:16	7:0	YSDC_D_DataIn2	Debug bus data in.
15:8	7:0	YSDC_D_DataIn1	Debug bus data in.
7:0	7:0	YSDC_D_DataIn0	Debug bus data in.

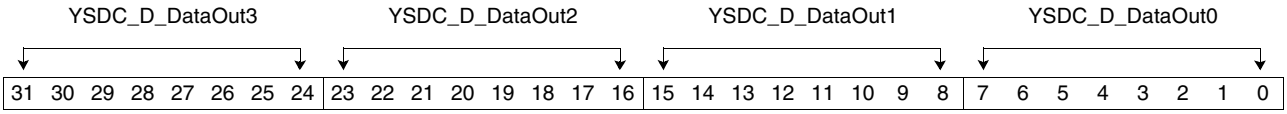
4.2.24 SDC Data Out Y Bus Register (SDC_Debug_Data_Out_Y)

Reset Output Status x‘0000 0000’ (Power-On Reset, DASL Path Y Reset, SDC Path Y Reset)

Address in Word Mode x‘6C’

Address in Byte Mode x‘6C’ to x‘6F’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	YSDC_D_DataOut3	Debug bus data out.
23:16	7:0	YSDC_D_DataOut2	Debug bus data out.
15:8	7:0	YSDC_D_DataOut1	Debug bus data out.
7:0	7:0	YSDC_D_DataOut0	Debug bus data out.

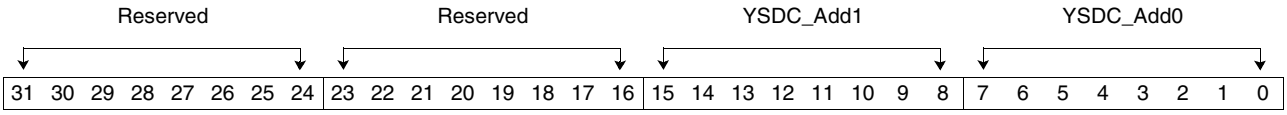
4.2.25 SDC Address Y Bus Register (SDC_Debug_Data_Address_Y)

Reset Output Status x‘0000 0000’ (Power-On Reset, DASL Path Y Reset, SDC Path Y Reset)

Address in Word Mode x‘70’

Address in Byte Mode x‘70’ to x‘73’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	Reserved	Reserved.
23:16	7:0	Reserved	Reserved.
15:8	7:0	YSDC_Add1	Debug bus address.
7:0	7:0	YSDC_Add0	Debug bus address.

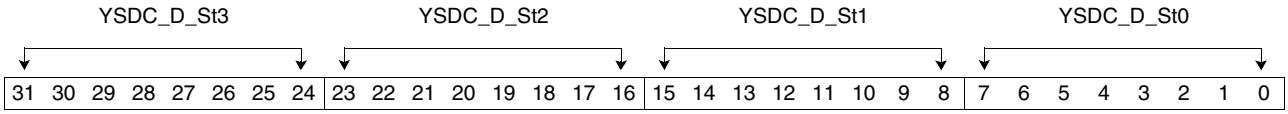
4.2.26 SDC Status Y Register (SDC_Status_Reg_Y)

Reset Output Status x‘0000 0000’ (Power-On Reset, DASL Path Y Reset, SDC Path Y Reset)

Address in Word Mode x‘74’

Address in Byte Mode x‘74’ to x‘77’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	YSDC_D_St3	Debug bus status.
23:16	7:0	YSDC_D_St2	Debug bus status.
15:8	7:0	YSDC_D_St1	Debug bus status.
7:0	7:0	YSDC_D_St0	Debug bus status.

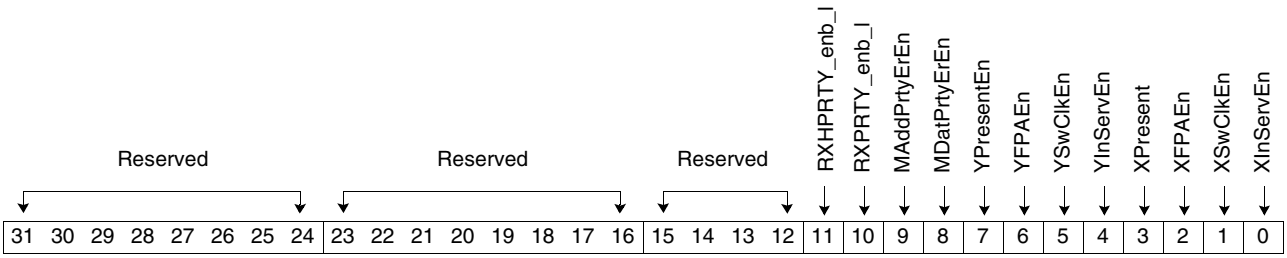
4.2.27 Event_2_Checker_Enable_X_and_Y Register

Reset Output Status x‘0000 0000’ (Power-On Reset, PE Reset)

Address in Word Mode x‘80’

Address in Byte Mode x‘80’ to x‘83’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	Reserved	Reserved.
23:16	7:0	Reserved	Reserved.
15:12	7:4	Reserved	Reserved.
11	3	RXHPRTY_enb_I	When set to ‘1’, enables the ingress switch header parity error checker.
10	2	RXPRTY_enb_I	When set to ‘1’, enables the ingress PE bus parity error checker.
9	1	MAddPrtyErEn	When set to ‘1’, enables processor address parity error detection.
8	0	MDatPrtyErEn	When set to ‘1’, enables processor data parity error detection.
7	7	YPresentEn	When set to ‘1’, enables Y path fabric present and fully inserted.
6	6	YFPAEn	When set to ‘1’, enables the Y path fabric port available checker.
5	5	YSwClkEn	When set to ‘1’, enables the switch clock Y missing checker.
4	4	YInServEn	When set to ‘1’, enables switch board Y in service (active/ready).
3	3	XPresent	When set to ‘1’, enables the X path fabric present and fully inserted.
2	2	XFPAEn	When set to ‘1’, enables the X path fabric port available (FPA) checker.
1	1	XSwClkEn	When set to ‘1’, enables the switch clock X missing checker.
0	0	XInServEn	When set to ‘1’, enables the switch board X in service (active/ready).

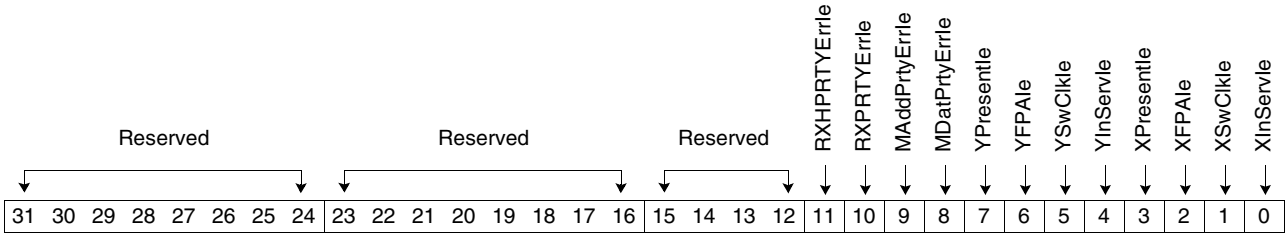
4.2.28 Event_2_Interrupt_Enable_X_and_Y Register

Reset Output Status x‘0000 0000’ (Power-On Reset, PE Reset)

Address in Word Mode x‘84’

Address in Byte Mode x‘84’ to x‘87’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	Reserved	Reserved.
23:16	7:0	Reserved	Reserved.
15:12	7:4	Reserved	Reserved.
11	3	RXHPRTYErrIe	When set to ‘1’, enables the ingress switch header parity error interrupt.
10	2	RXPRTYErrIe	When set to ‘1’, enables the ingress PE bus parity error interrupt.
9	1	MAddPrtyErrIe	When set to ‘1’, enables the processor address parity error interrupt.
8	0	MDatPrtyErrIe	When set to ‘1’, enables the processor data parity error interrupt.
7	7	YPresentIe	When set to ‘1’, enables the Y path fabric not present or not fully inserted interrupt.
6	6	YFPAIe	When set to ‘1’, enables the Y path fabric port not available interrupt.
5	5	YSwClkIe	When set to ‘1’, enables the switch clock Y missing interrupt.
4	4	YInServIe	When set to ‘1’, enables the switch board Y in service (active/ready) interrupt.
3	3	XPresentIe	When set to ‘1’, enables the X path fabric not present or not fully inserted interrupt.
2	2	XFPAIe	When set to ‘1’, enables the X path fabric port not available interrupt.
1	1	XSwClkIe	When set to ‘1’, enables the switch clock X missing interrupt.
0	0	XInServIe	When set to ‘1’, enables the switch board X in service (active/ready) interrupt.

4.2.29 Event_2_X_and_Y Register

Some of these register bits directly reflect the status of the device input lines, and their value depends on the device input lines.

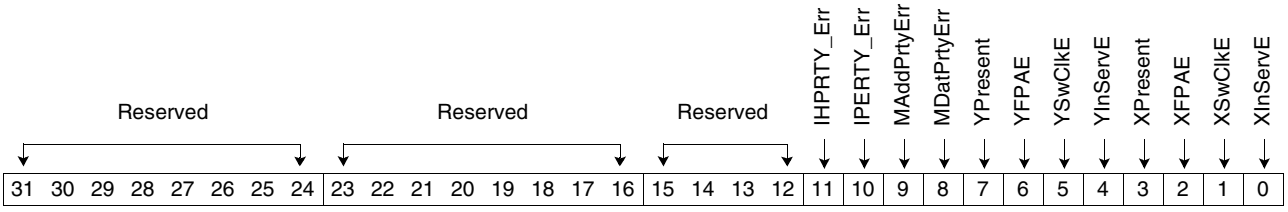
Note: For information about how to clear this register, see Section 4.1 , Error Detection, Reporting, and Interrupt Registers, on page 68.

Reset Output Status x‘0000 0000’ (Power-On Reset, PE Reset)

Address in Word Mode x‘88’

Address in Byte Mode x‘88’ to x‘8B’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	Reserved	Reserved.
23:16	7:0	Reserved	Reserved.
15:12	7:4	Reserved	Reserved.
11	3	IHPRTY_Err	1 Ingress switch header parity error. 0 Normal operation.
10	2	IPERTY_Err	1 Ingress PE (UTOPIA-3) bus parity error. 0 Normal operation.
9	1	MAddPrtyErr	1 Processor address parity error. 0 Normal operation.
8	0	MDatPrtyErr	1 Processor data parity error. 0 Normal operation.
7	7	YPresent	1 Y path fabric is not present or not fully inserted. Information is derived from the SWITCH_Y_PRESENT I/O pin. 0 Normal operation.
6	6	YFPAE	1 Y path fabric port is not available (the DASL receiver for that switch port is not synchronized). Information is derived from the FPAN_Y I/O pin. 0 Normal operation.
5	5	YSwClkE	1 Switch clock Y missing information is sensed at the output of the multiplexer that allows selection of the switch clock source. 0 Normal operation.
Note: Some of the bits in this register are directly forced by the hardware. Even if they are read/write, when the microprocessor writes a value different from the current bit content, the hardware immediately overwrites the microprocessor value.			

Bit(s)		Field Name	Description
Word Mode	Byte Mode		
4	4	YInServE	Switch board Y in service (active/ready). 1 When switch Y in service is detected, remains active as long as switch Y is in service. 0 Switch Y is in protection mode.
3	3	XPresent	1 X path fabric is not present or not fully inserted. Information is derived from the SWITCH_X_PRESENT I/O pin. 0 Normal operation.
2	2	XFPAE	1 X path fabric port is not available (the DASL receiver for that switch port is not synchronized). Information is derived from the FPAN_X I/O pin. 0 Normal operation.
1	1	XSwClkE	1 Switch clock X missing information is sensed at the output of the multiplexer that allows selection of the switch clock source. 0 Normal operation.
0	0	XInServE	Switch board X in service (active/ready). 1 When switch X in service is detected, remains active as long as switch X is in service. 0 Switch X is in protection mode.

Note: Some of the bits in this register are directly forced by the hardware. Even if they are read/write, when the microprocessor writes a value different from the current bit content, the hardware immediately overwrites the microprocessor value.

4.2.30 ABIST Failure Test_Status_X_Y Register

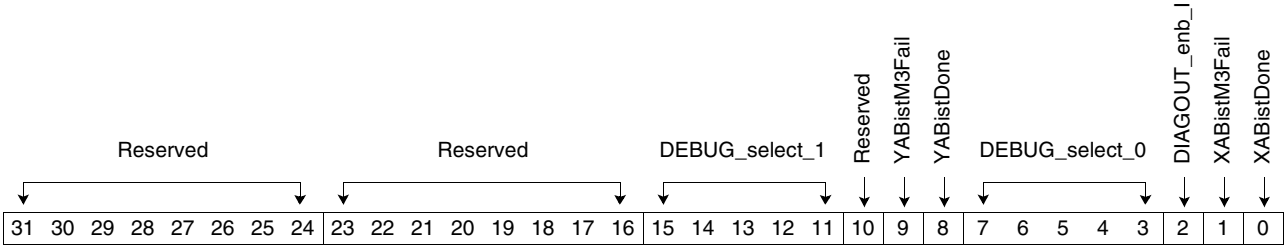
This register is not accessible by the user, and the bit should not be set to '1'. It is used only during manufacturing tests.

Reset Output Status x'0000 0000' (Power-On Reset)

Address in Word Mode x'8C'

Address in Byte Mode x'8C' to x'8F'

Access Type Read/Write



Bit(s)		Field Name	Description	Notes
Word Mode	Byte Mode			
31:24	7:0	Reserved	Reserved.	
23:16	7:0	Reserved	Reserved.	
15:11	7:3	DEBUG_select_1	This bit controls debug bus multiplexing. When set to '1', it selects debug bus 1.	1
10	2	Reserved	Reserved.	
9	1	YABistM3Fail	1 Array built-in self test (ABIST) failure flag on M3 RAM. 0 Normal operation.	
8	0	YABistDone	1 ABIST complete flag. 0 Normal operation.	
7:3	7:3	DEBUG_select_0	This bit controls debug bus multiplexing. When set to '1', it selects debug bus 0.	1
2	2	DIAGOUT_enb_l	This bit redirects the ABIST result on the ABIST_DiagOut I/O. 1 Y side. 0 X side.	
1	1	XABistM3Fail	1 ABIST failure flag on M3 RAM. 0 Normal operation.	
0	0	XABistDone	1 ABIST complete flag. 0 Normal operation.	

1. See debug bus definition, page 148, for details.

4.2.31 Switch_X_PLL Setting Register

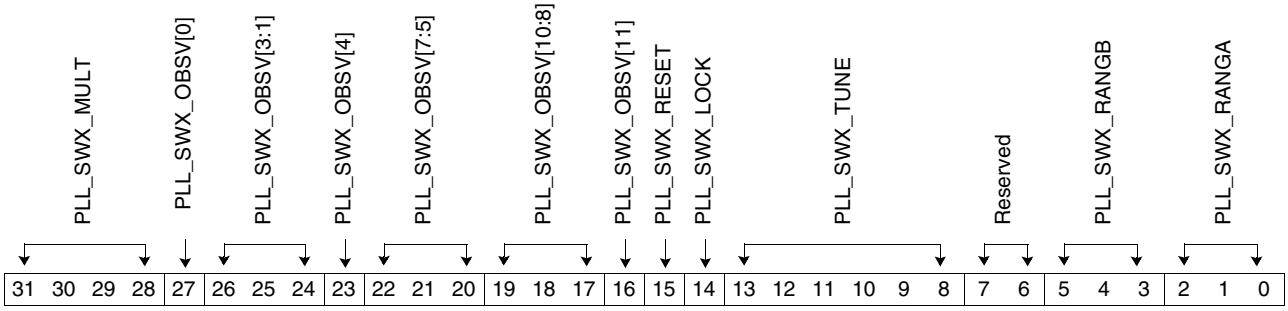
These settings correspond to a voltage-controlled oscillator (VCO) setting of 660 MHz. The PLL observe bits will automatically overwrite what has been written by the microprocessor.

Reset Output Status x‘0800 C000’ (Power-On Reset)

Address in Word Mode x‘90’

Address in Byte Mode x‘90’ to x‘93’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:28	7:4	PLL_SWX_MULT	Programmable switch X PLL multiplier. 0010 Normal operation. The reference clock is 55 to 62.5 MHz for a switch byte clock of 110 to 125 MHz.
27	3	PLL_SWX_OBSV[0]	Switch X PLL observe reset. Read only.
26:24	2:0	PLL_SWX_OBSV[3:1]	Switch X PLL observe. Multiplier bits 3:1. Read only.
23	7	PLL_SWX_OBSV[4]	Switch X PLL observe. Multiplier bit 0. Read only.
22:20	6:4	PLL_SWX_OBSV[7:5]	Switch X PLL observe. Buffered version of range B, bits 2:0. Read only.
19:17	3:1	PLL_SWX_OBSV[10:8]	Switch X PLL observe. Buffered version of range A, bits 2:0. Read only.
16	0	PLL_SWX_OBSV[11]	Switch X PLL observe reset (delayed by one clock cycle). Read only.
15	7	PLL_SWX_RESET	1 Resets switch X PLL. Equivalent to bypass mode. 0 Normal operation after PLL programming.
14	6	PLL_SWX_LOCK	1 Locks switch X PLL. 0 Unlocks switch X PLL.
13:8	5:0	PLL_SWX_TUNE	Programmable switch X PLL tune. 010011 Normal operation. The product of forward and feedback dividers is between (6/4)<M<6.
7:6	7:6	Reserved	Reserved.
5:3	5:3	PLL_SWX_RANGB	Programmable switch X PLL range B. 101 Normal operation. PLLOUTB frequency is 133 to 267 MHz.
2:0	2:0	PLL_SWX_RANGA	Programmable switch X PLL range A. 010 Normal operation. PLLOUTA frequency is 66 to 134 MHz.

4.2.32 Switch_Y_PLL Setting Register

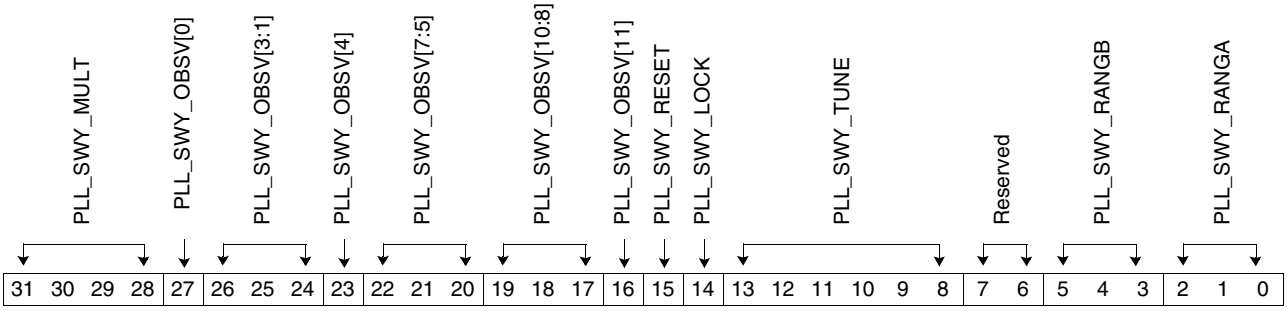
These settings correspond to a VCO setting of 660 MHz. The PLL observe bits will automatically overwrite what has been written by the microprocessor.

Reset Output Status x‘0800 C000’ (Power-On Reset)

Address in Word Mode x‘94’

Address in Byte Mode x‘94’ to x‘97’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:28	7:4	PLL_SWY_MULT	Programmable switch Y PLL multiplier. 0010 Normal operation. The reference clock is 55 to 62.5 MHz for a switch byte clock of 110 to 125 MHz.
27	3	PLL_SWY_OBSV[0]	Switch Y PLL observe reset. Read only.
26:24	2:0	PLL_SWY_OBSV[3:1]	Switch Y PLL observe. Multiplier bits 3:1. Read only.
23	7	PLL_SWY_OBSV[4]	Switch Y PLL observe. Multiplier bit 0. Read only.
22:20	6:4	PLL_SWY_OBSV[7:5]	Switch Y PLL observe. Buffered version of range B, bits 2:0. Read only.
19:17	3:1	PLL_SWY_OBSV[10:8]	Switch Y PLL observe. Buffered version of range A, bits 2:0. Read only.
16	0	PLL_SWY_OBSV[11]	Switch Y PLL observe reset (delayed by one clock cycle). Read only.
15	7	PLL_SWY_RESET	1 Resets switch Y PLL. Equivalent to bypass mode. 0 Normal operation after PLL programming.
14	6	PLL_SWY_LOCK	1 Locks switch Y PLL. 0 Unlocks switch Y PLL.
13:8	5:0	PLL_SWY_TUNE	Programmable switch Y PLL tune. 010011 Normal operation. The product of forward and feedback dividers is between (6/4)<M<6.
7:6	7:6	Reserved	Reserved.
5:3	5:3	PLL_SWY_RANGB	Programmable switch Y PLL range B. 101 Normal operation. PLLOUTB frequency is 133 to 267 MHz.
2:0	2:0	PLL_SWY_RANGA	Programmable switch Y PLL range A. 010 Normal operation. PLLOUTA frequency is 66 to 134 MHz.

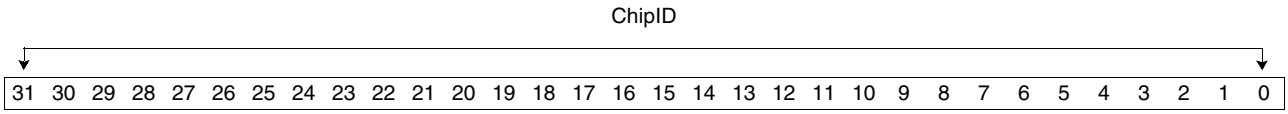
4.2.33 Chip_ID Register

Reset Output Status (not applicable, wired information)

Address in Word Mode x‘98’

Address in Byte Mode x‘98’ to x‘9B’

Access Type Read



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:0	7:0 15:8 23:16 31:24	ChipID	UDASL pass 1: x‘3442 3600’ UDASL pass 2: x‘3442 3601’

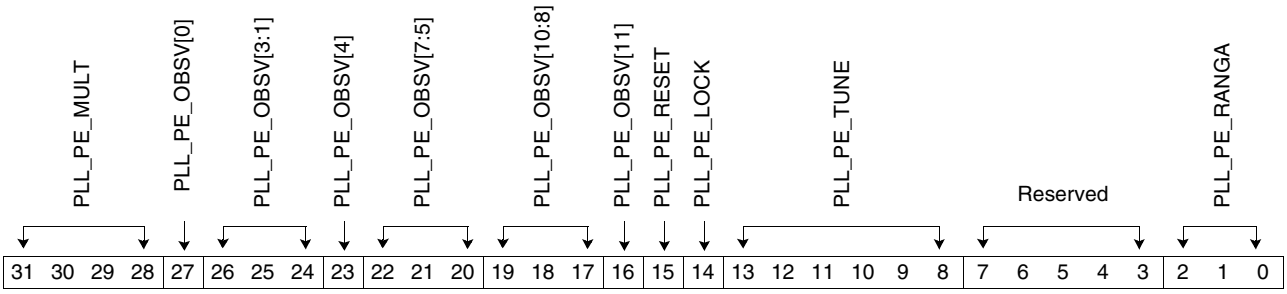
4.2.34 Protocol Engine PLL Setting Register (PE_PLL Register)

Reset Output Status x‘0800 C000’ (Power-On Reset)

Address in Word Mode x‘9C’

Address in Byte Mode x‘9C’ to x‘9F’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:28	7:4	PLL_PE_MULT	Programmable PE PLL multiplier. 0001 Frequency multiplication is one.
27	3	PLL_PE_OBSV[0]	PE X PLL observe reset. Read only.
26:24	2:0	PLL_PE_OBSV[3:1]	PE X PLL observe. Multiplier bits 3:1. Read only.
23	7	PLL_PE_OBSV[4]	PE PLL observe. Multiplier bit 0. Read only.
22:20	6:4	PLL_PE_OBSV[7:5]	PE PLL observe. Buffered version of range B, bits 2:0. Read only.
19:17	3:1	PLL_PE_OBSV[10:8]	PE PLL observe. Buffered version of range A, bits 2:0. Read only.
16	0	PLL_PE_OBSV[11]	Switch PE PLL observe reset (delayed by one clock cycle). Read only.
15	7	PLL_PE_RESET	1 Resets PE PLL. Equivalent to bypass mode. 0 Normal operation after PLL programming.
14	6	PLL_PE_LOCK	1 Locks PE PLL. 0 Unlocks PE PLL.
13:8	5:0	PLL_PE_TUNE	Programmable switch PE PLL tune. 010010 Normal operation. The product of forward and feedback dividers is between (6/4)<M<6.
7:3	7:3	Reserved	Reserved.
2:0	2:0	PLL_PE_RANGA	Programmable PE PLL range A. 010 Normal operation. PLLOUTA frequency is 66 to 134 MHz.

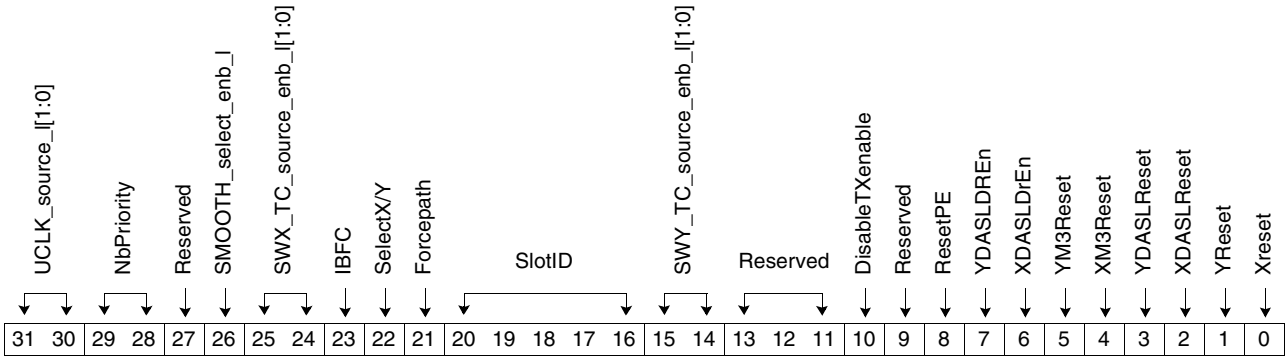
4.2.35 Common_Control Register

Reset Output Status x‘0500 413F’ (Power-On Reset)

Address in Word Mode x‘A0’

Address in Byte Mode x‘A0’ to x‘A3’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:30	7:6	UCLK_source_l[1:0]	Selects the ingress clock source. 00 Microprocessor. 01 PE clock used to time the PE interface. 10 External smoothing PLL. 11 Microprocessor clock.
29:28	5:4	NbPriority	Controls the cycling process of output queue grant and shared memory grant information from the switch. 00 Enable only priority 0. 01 Enable priority 0 and 1. 10 Enable priority 0, 1, and 2. 11 Enable priority 0, 1, 2, and 3 (all four priorities in use).
27	3	Reserved	Reserved.
26	2	SMOOTH_select_enb_l	Selects smooth PLL out and enables the driver. 0 The selected switch clock used by the converter is not the one used to drive an external smoothing PLL. In this case, a clock coming from the PE itself (or an external oscillator) is used to drive the PE interface rather than the From_Smooth_PLL_out. 1 The To_Smooth_PLL_In interface line is used to drive the PE interface to support a smooth switching from one clock plane to the other in case of switch plane switch-over. In that case, the switch and the protocol engine are clock synchronous.
25:24	1:0	SWX_TC_source_enb_l[1:0]	Selects the switch X clock. 11 Normal setting: selects switch fabric X clock for switch X interface. 10 Selects external TEST_CLK oscillator for switch X interface. 01 Selects external MP_CLK oscillator for switch X interface. 00 Forces the switch X interface clock to a fixed value of ‘1’ to test clock missing detection.

Bit(s)		Field Name	Description
Word Mode	Byte Mode		
23	7	IBFC	Enables in-band flow control (out-of-band flow control is default) and enables the sending of egress idle packets. 1 OQG and shared memory grant (SMG) information is carried in the packet header of each egress packet. On ingress, the in-band TxPause is extracted from the packet qualifier and provided to the egress FIFO flow control mechanism to control the PRS28.4G SND_GRANT interface line. 0 Out-of-band flow control (also used for switch loopback).
22	6	SelectX/Y	Selects the plane in service in case Forcepath, bit 21, is enabled. 0 X in service. 1 Y in service.
21	5	Forcepath	1 Forces the plane selected into service through bit 22 of this register. 0 Normal operation. In-service lines select the plane in service.
20:16	4:0	SlotID	Senses in which backplane slot the converter is plugged. It is directly mapped to Slot_IDn[4:0]. 0 Indicates the sense line is asserted. 1 Indicates the sense line is deasserted.
15:14	7:6	SWY_TC_source_enb_l[1:0]	Selects the switch Y clock. 11 Normal setting: selects switch fabric Y clock for switch Y interface. 10 Selects external TEST_CLK oscillator for switch Y interface. 01 Selects external MP_CLK oscillator for switch Y interface. 00 Forces the switch Y interface clock to a fixed value of '1' to test clock missing detection.
13:11	5:3	Reserved	Reserved.
10	2	DisableTXenable	1 Validates TxData on Egress PE interface (normal UTOPIA-3 mode). 0 Forces TxEnable signal to deassert ('1'). Used in switch loopback mode.
9	1	Reserved	Reserved.
8	0	ResetPE	1 Resets PE interface and all registers, except this one. Does not reset microprocessor front end or PLL register. 0 Normal operation.
7	7	YDASLDREn	1 Normal operation. 0 Disables Y path DASL driver. Same result as interface line DASL_DRV_ENB.
6	6	XDASLDrEn	1 Normal operation. 0 Disables X path DASL driver. Same result as interface line DASL_DRV_ENB.
5	5	YM3Reset	1 Resets M3 reset SDC path Y. 0 Normal operation.
4	4	XM3Reset	1 Resets M3 reset SDC path X. 0 Normal operation.
3	3	YDASLReset	1 Resets DASL path Y. 0 Normal operation.
2	2	XDASLReset	1 Resets DASL path X. 0 Normal operation.

Bit(s)		Field Name	Description
Word Mode	Byte Mode		
1	1	YReset	1 Resets path Y. 0 Normal operation.
0	0	Xreset	1 Resets path X. 0 Normal operation.

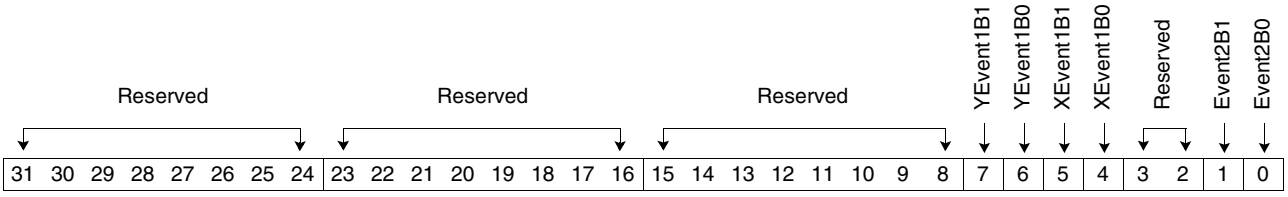
4.2.36 Interrupt_Register_Indirection Register

Reset Output Status x‘0000 0000’ (Power-On Reset)

Address in Word Mode x‘A4’

Address in Byte Mode x‘A4’ to x‘A7’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	Reserved	Reserved.
23:16	7:0	Reserved	Reserved.
15:8	7:0	Reserved	Reserved.
7	7	YEvent1B1	Event 1 on plane Y byte 1.
6	6	YEvent1B0	Event 1 on plane Y byte 0.
5	5	XEvent1B1	Event 1 on plane X byte 1.
4	4	XEvent1B0	Event 1 on plane X byte 0.
3:2	3:2	Reserved	Reserved.
1	1	Event2B1	Event 2 byte 1.
0	0	Event2B0	Event 2 byte 0.
Note: The PLL Clock Missing bits are not implemented.			

Note: The bits in this register are shadows of what is occurring in other triggering registers. To clear a bit in this register, its source must be cleared. For example, if a bit is set in the Interrupt_Enable_X register, Interrupt_Enable_Y register, or Event_2_Interrupt_Enable_X_and_Y register, the corresponding bit in this register will be set. When the bits in those registers are cleared, the corresponding bit in this register is cleared.

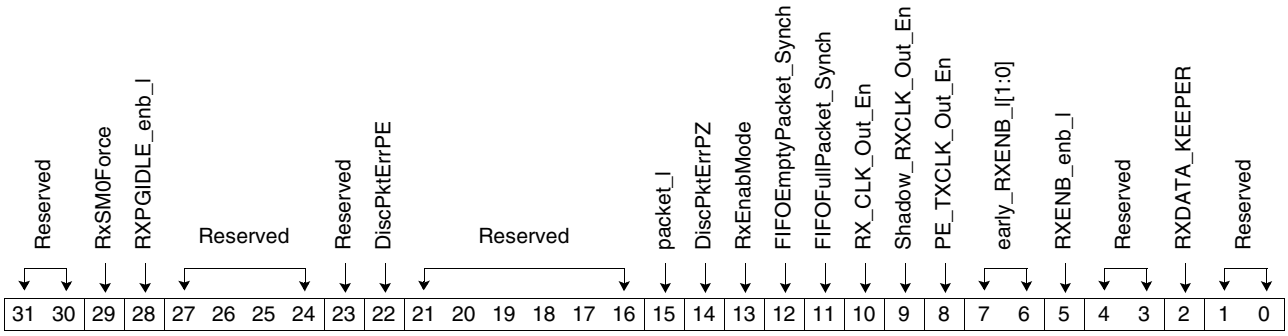
4.2.37 Ingress PE Setting Register (Ingress_PE_Interface [IPI] - Receive)

Reset Output Status x‘2001 8000’ (Power-On Reset, PE Reset)

Address in Word Mode x‘C0’

Address in Byte Mode x‘C0’ to x‘C3’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:30	7:6	Reserved	Reserved.
29	5	RxSM0Force	Forces shared memory ‘00’ degrant ‘0’ (highest priority) for FIFO full. 1 In-band flow control. 0 Out-of-band flow control.
28	4	RXPGIDLE_enb_l	1 Idle packets are received and discarded. 0 Idle packets are received and not discarded.
27:24	3:0	Reserved	Reserved.
23	7	Reserved	Reserved.
22	6	DiscPktErrPE	0 Does not discard packets with PE bus parity in error. 1 Discards packets with bad parity on PE interface.
21:16	5:0	Reserved	Reserved.
15	7	packet_l	1 Operates in packet mode on PE interface. 0 Does not support word mode.
14	6	DiscPktErrPZ	1 Discards packets with bad switch header parity. 0 Does not discard packets with bad switch header parity.
13	5	RxEnabMode	High $\overline{\text{RXENB}}$ signal is sampled at the end of the packet transmission (UTOPIA-3 compliant). Low $\overline{\text{RXENB}}$ signal is free running.
12	4	FIFOEmptyPacket_Synch	1 IBM reserved. 0 Normal FIFO operation.
11	3	FIFOFullPacket_Synch	1 IBM reserved. 0 Normal FIFO operation.
10	2	RX_CLK_Out_En	1 Enables PE RCV clock out. 0 Disables PE RCV clock out.

Bit(s)		Field Name	Description
Word Mode	Byte Mode		
9	1	Shadow_RXCLK_Out_En	1 Enables shadow receive clock out driver. 0 Disables shadow receive clock out driver.
8	0	PE_TXCLK_Out_En	1 Enables the PE TX transmit clock out driver. 0 Disables PE TX clock out driver.
7:6	7:6	early_RXENB_l[1:0]	RXDATA vs. $\overline{\text{RXENB}}$ calibration up to four URXCLK clock cycles. 00 0 URXCLK cycle delay (normal operation). 01 1 URXCLK cycle delay (IBM reserved). 10 2 URXCLK cycle delay (IBM reserved). 11 3 URXCLK cycle delay (IBM reserved).
5	5	RXENB_enb_l	Receives enable interface line assertion for FIFO full. 1 Enables $\overline{\text{RXENB}}$ to control flow for ingress FIFO full. 0 Receive enable interface line is not used for ingress link-level flow control (signal is forced deasserted to '1').
4:3	4:3	Reserved	Reserved.
2	2	RXDATA_KEEPER	Ingress PE data delay for correct resampling. Bit Selected clock. 0 ShadowRxClockOut - switch loopback. 1 ShadowRXClockIn - normal operation.
1:0	1:0	Reserved	Reserved.

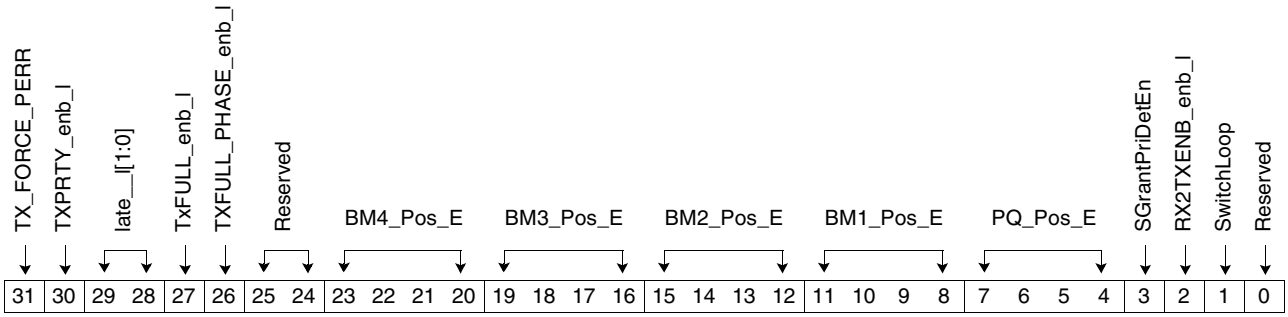
4.2.38 Egress PE Setting Register (Egress_PE_Interface [EPI] - Transmit)

Reset Output Status x‘3843 2100’ (Power-On Reset, PE Reset)

Address in Word Mode x‘C4’

Address in Byte Mode x‘C4’ to x‘C7’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31	7	TX_FORCE_PERR	1 Forces parity error on egress bus. 0 Disables parity error insertion on the egress UTOPIA-3 interface.
30	6	TXPRTY_enb_l	Egress PE interface parity enable. 1 Enables assertion of the parity bit. 0 Disables assertion of the parity bit.
29:28	5:4	late_TXFULL_l[1:0]	$\overline{\text{TXFULL}}$ vs. $\overline{\text{TXENB}}$ calibration up to four UTXCLK clock cycles. 00 1 UTXCLK cycle delay (IBM reserved). 01 2 UTXCLK cycle delay (IBM reserved). 10 3 UTXCLK cycle delay (IBM reserved). 11 4 UTXCLK cycle delay (operates as described in the UTOPIA-3 document) (normal operation).
27	3	TxFULL_enb_l	1 Enables the converter to use $\overline{\text{TXFULL}}$ interface line. 0 Disables any action of $\overline{\text{TXFULL}}$ on the converter operation.
26	2	TXFULL_PHASE_enb_l	Selects the active level of $\overline{\text{TXFULL}}$. 1 Operates with $\overline{\text{TXFULL}}$ condition asserted as active high. 0 Operates with the standard UTOPIA-3 $\overline{\text{TXFULL}}$ phase (active low).
25:24	1:0	Reserved	Reserved.
23:20	7:4	BM4_Pos_E	Bit map-4 byte position in packet. 0100 Puts OQG4 as first byte in second word of packet (OQG in sequence). 0111 Puts OQG4 as fourth byte in second word of packet (all OQG in second word).

Bit(s)		Field Name	Description
Word Mode	Byte Mode		
19:16	3:0	BM3_Pos_E	Bit map-3 byte position in packet. 0011 Puts OQG3 as fourth byte in first word of packet (OQG in sequence). 0110 Puts OQG3 as third byte in the second word of packet (all OQG in second word).
15:12	7:4	BM2_Pos_E	Bit map-2 byte position in packet. 0010 Puts OQG2 as third byte in first word of packet (OQG in sequence). 0101 Puts OQG2 as second byte in second word of packet (all OQG in second word).
11:8	3:0	BM1_Pos_E	Bit map-1 byte position in packet. 0001 Puts OQG1 as second byte in first word of packet (OQG in sequence). 0100 Puts OQG1 as first byte in second word of packet (all OQG in second word).
7:4	7:4	PQ_Pos_E	Packet qualifier byte position in packet. 0000 Puts PQ as first byte in first word of packet.
3	3	SGrantPriDetEn	1 Supports IBM Packet Routing Switch send grant per priority enable. (Set to '0' in out-of-band flow control). 0 IBFC: operates with single send grant priority to the PRS28.4G.
2	2	RX2TXENB_enb_l	1 Routes internal $\overline{\text{RXENB}}$ to the internal $\overline{\text{TXFULL}}$ to flow control the egress path during switch loop. 0 Asserts internal $\overline{\text{RXENB}}$ to egress path during switch loop (no data can go through).
1	1	SwitchLoop	1 Sends TXDATA[31:0] on ingress PE interface while in switch loop X or Y. 0 Normal operation. Data continues to exit converter.
0	0	Reserved	Reserved.

Note: In general, the packet qualifier is located in the first word of the first byte, and the bitmap is located after the packet qualifier. However, *with operation using out-of-band flow control*, the packet qualifier may be located in the second word, following the bitmap. The Egress_PE_Interface and PE_Common registers require special encoding for this configuration. In the Egress_PE_Interface register:

- Set bits 23:20 to '0011'
- Set bits 19:16 to '0010'
- Set bits 15:12 to '0001'
- Set bits 11:8 to '0000'
- Set bits 7:4 to '0100'

For the corresponding PE_Common register encoding, see the register description.

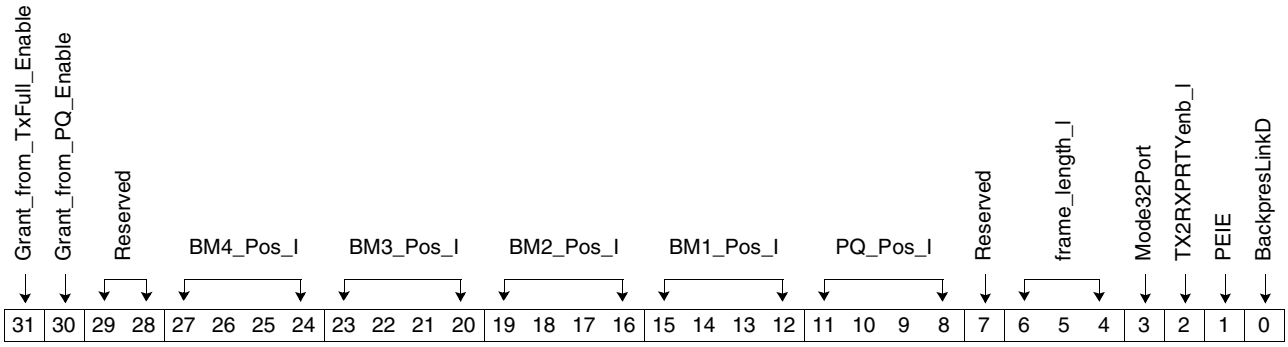
4.2.39 Common PE Setting Register (PE_Common)

Reset Output Status x‘0132 1008’ (Power-On Reset)

Address in Word Mode x‘C8’

Address in Byte Mode x‘C8’ to x‘CB’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31	7	Grant_from_TxFull_Enable	1 IBM reserved. 0 Normal operation.
30	6	Grant_from_PQ_Enable	1 Extracts TxPause flow control information from the incoming packet qualifier to control either the send grant per priority to the switch or the flow of packets from the converter. 0 Out-of-band flow control.
29:28	5:4	Reserved	Reserved.
27:24	3:0	BM4_Pos_I	Bit map-4 byte position in packet. 0001 Gets BM4 from second byte of first word (during BM1 swap, BM4 is moved there from first byte of second word [Bit_Map in sequence]). 0111 Gets BM4 from fourth byte in second word of packet (all Bit_Map in second word).
23:20	7:4	BM3_Pos_I	Bit map-3 byte position in packet. 0011 Gets BM3 from fourth byte of first word (Bit_Map in sequence). 0110 Gets BM3 from third byte in second word of packet (all Bit_Map in second word).
19:16	3:0	BM2_Pos_I	Bit map-2 byte position in packet. 0010 Gets BM2 from third byte of first word (Bit_Map in sequence). 0101 Gets BM2 from second byte in the second word of packet (all Bit_Map in second word).
15:12	7:4	BM1_Pos_I	Bit map-1 byte position in packet. 0001 Gets BM1 from second byte of first word (Bit_Map in sequence). 0100 Gets BM1 from first byte in second word of packet (all Bit_Map in second word).
11:8	3:0	PQ_Pos_I	Packet qualifier byte position in packet. 0000 Gets packet qualifier from first byte of first word.

Bit(s)		Field Name	Description
Word Mode	Byte Mode		
7	7	Reserved	Reserved.
6:4	6:4	frame_length_l	Sets the length of the LU. 000 16-byte LU (64-byte packet). 001 17-byte LU (68-byte packet). 010 18-byte LU (72-byte packet). 011 19-byte LU (76-byte packet). 100 20-byte LU (80-byte packet).
3	3	Mode32Port	1 Selects 32-bit bit map header mode. 0 Selects 16-bit bit map header mode.
2	2	TX2RXPRTYenb_l	1 Checks PE data parity in switch loopback mode. 0 Does not check PE data parity in switch loopback mode.
1	1	PEIE	1 Normal operation. 0 Disables PE interface. Default mode is inactive. Inhibits output driver (equivalent to high impedance).
0	0	BackpresLinkD	1 Operates in out-of-band flow control. 0 Disables back-pressure serial link (set to high impedance).

Note: In general, the packet qualifier is located in the first word of the first byte, and the bitmap is located after the packet qualifier. However, *with operation using out-of-band flow control*, the packet qualifier may be located in the second word, following the bitmap. The Egress_PE_Interface and PE_Common registers require special encoding for this configuration. In the PE_Common register:

- Set bits 27:24 to ‘0011’
- Set bits 23:20 to ‘0010’
- Set bits 19:16 to ‘0001’
- Set bits 15:12 to ‘0000’
- Set bits 11:8 to ‘0100’

For the corresponding Egress_PE_Interface register encoding, see the register description.

4.2.40 Ingress Parity Error Count Register (PARITY_Error_count)

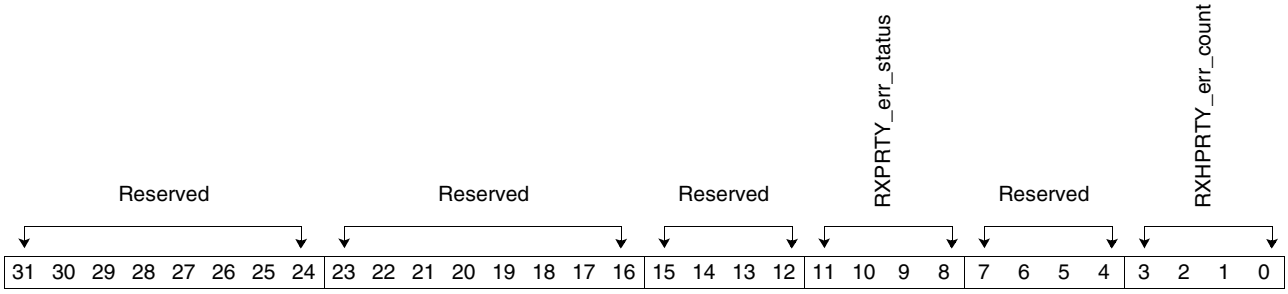
The microprocessor has the highest priority when writing into this register.

Reset Output Status x‘0000 0000’ (Power-On Reset, PE Reset)

Address in Word Mode x‘CC’

Address in Byte Mode x‘CC’ to x‘CF’

Access Type Read/Write



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31:24	7:0	Reserved	Reserved.
23:16	7:0	Reserved	Reserved.
15:12	7:4	Reserved	Reserved.
11:8	3:0	RXPRTY_err_status	Ingress PE bus parity error count.
7:4	7:4	Reserved	Reserved.
3:0	3:0	RXHPRTY_err_count	PRS28.4G header parity error count.

5. Data-Aligned Synchronous Link (DASL)

5.1 General Description

The Data-Aligned Synchronous Link (DASL) interface is intended for high-speed, point-to-point, interdevice communication. The interface macro performs multibit serialization and deserialization to reduce the I/O pin count. It is a synchronous device, removing the need for asynchronous interfaces that introduce additional interface latency. DASLs are intended to operate over a backplane without any additional components. The DASL macro is designed for high levels of integration and uses reduced voltage differential transceivers to reduce power consumption.

The DASL macro is connected to the converter logic through the interface lines shown in Figure 5-1 and described in Table 5-1.

Figure 5-1. Data-Aligned Synchronous Interface Lines

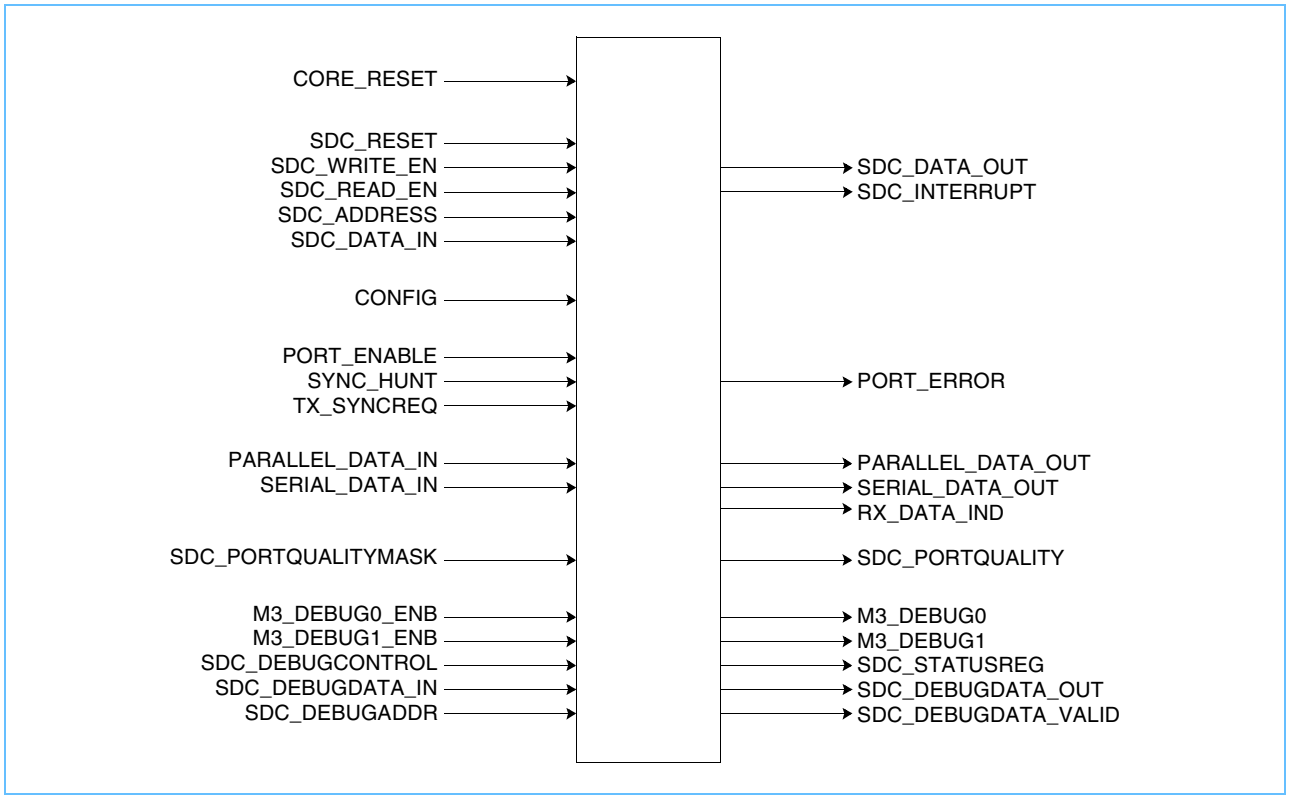


Table 5-1. Internal DASL Signal Interface Descriptions (Page 1 of 3)

Function	Signal Name	Direction	Description
Clocking Reset	CORE_RESET (DASL reset)	In	Core logic discrete reset (active reset signal).
	SDC_RESET (SDC reset)	In	Shared DASL controller processor reset. Active reset signal used in conjunction with picocode download.
SDC Internal Resource Interface	SDC_WRITE_EN	In	SDC Write Enable triggers a write operation during picocode download.
	SDC_READ_EN	In	SDC Read Enable triggers a picocode read operation.
	SDC_ADDRESS[0:10]	In	SDC address bus.
	SDC_DATA_IN[0:15]	In	SDC write data bus.
	SDC_DATA_OUT[0:15]	Out	SDC read data bus.
	SDC_INTERRUPT	Out	SDC interrupt.
Application Control Interface	CONFIG[0:15]	In	Configuration Register 0:4 Number of Physical DASL Ports - 1 (n-1). MSB = Bit 4. 5:7 Number of Physical Subports -1 (m-1). MSB = Bit 7. Only two values are supported: 110 For a 16-bit port 111 For a 32-bit port 8:12 Unique Hardware Version Number (obtain from provider of the source picocode). MSB = Bit 12. 13 External Speed Expansion Mode. This bit should be tied high if external speed expansion is enabled. **This is a reserved function and should not be enabled. This bit must be held low.** 14 Internal Speed Expansion Mode. This bit should be tied high if internal speed expansion is enabled. **This is a reserved function and should not be enabled. This bit must be held low**. 15 DASL Synchronization Mode. Same value as the signal DASLSYNCMODE.
Application Port Interface	PORT_ENABLE	In	DASL Port Enable.
	SYNC_HUNT	In	DASL Synchronization Request. A low to high transition will force the synchronization sequence of the receive DASL port.
	PARALLEL_DATA_IN[0:31]	In	Parallel Data In. Data to be transmitted.
	TX_SYNCREQ	In	Transmit Link Synchronization Request Input. When active, the DASL TXPORT enters an idle state and will begin the synchronization sequence after the falling edge.
	RX_DATA_IND	Out	Receive Data Indication. When active, indicates that the DATA_OUT bus now holds valid data.
	PARALLEL_DATA_OUT[0:31]	Out	Parallel Data Out. Data received from the DASL.
	PORT_ERROR	Out	Port Error. When active, indicates that an error has been detected by the shared DASL controller.

Table 5-1. Internal DASL Signal Interface Descriptions (Page 2 of 3)

Function	Signal Name	Direction	Description
Application Port Interface (Continued)	SDC_PORTQUALITYMASK	In	SDC Port Quality Mask. When active, indicates that the SDC port quality bit should be reset.
	SDC_PORTQUALIT	Out	SDC Port Quality. When active, indicates that the shared DASL controller has detected a minimum eye error on a port. This error indicates that one or more of the DASLs that make up the port is not operating within specification.
Application DASL Off-Chip Interface	SERIAL_DATA_IN[0:7]	In	Serial Data Input. Serialized data stream received at the serial link speed.
	SERIAL_DATA_OUT[0:7]	Out	Serial Data Out. Serialized data stream generated at the serial link speed.
Diagnostic and Debug	M3_DEBUG0_ENB	In	Processor Debug 0 Bus Enable. When active, indicates that debug information is available on the M3_DEBUG0 bus. When not active, the M3_DEBUG0 bus will be all zeros.
	M3_DEBUG0[0:15]	Out	Debug 0 Bus 0:1 Reserved. All bits are set to zero. 2:4 ALU Status Bits. MSB = Bit 2. 5:15 Program Counter. MSB = Bit 5.
	M3_DEBUG1_ENB	In	Processor Debug 1 Bus Enable. When active, indicates that debug information is available on the M3_DEBUG1 bus. When not active, the M3_DEBUG1 bus will be all zeros.
	M3_DEBUG1[0:15]	Out	Debug 1 Bus (Instruction Decoder) 0 PX_AUTO_INCREMENT[14:15]. From IDCD_CC unit. MSB = Bit 14. 1 ACCESS_PX 2 PY_AUTO_INCREMENT 3 ACCESS_PY 4:5 ALU_A_SELECT. MSB = Bit 4. 6:7 ALU_B_SELECT. MSB = Bit 6. 8:9 DATA_WIDTH. MSB = Bit 8. 10 IMMEDIATE_DATA_FROM_ INSTRUCTION 11 MUX1_CNTL 12 MUXQ_CNTL 13 MUXR_CNTL 14:15 From IDCD_CC unit. MSB = Bit 14.

Table 5-1. Internal DASL Signal Interface Descriptions (Page 3 of 3)

Function	Signal Name	Direction	Description
Diagnostic and Debug (Continued)	SDC_DEBUGCONTROL[0:31]	In	SDC Debug Control Input 0 Debug Register Enable 1 Port Processing Disable 2 Temperature Compensation Disable 3 DASL Adjustment Disable 4:7 Encoded Debug Select 8:11 Port Select. See “Debug Control Input Definition.” 12:15 DASL Select. See “Debug Control Input Definition.” 16:23 Reserved. All bits are set to zero. 24:31 Status Count Input. Used in conjunction with the Status Count Output field (XSDC_D_st0) of the SDC Status register (SDC_ Status_Reg) to create a watchdog mechanism. The DASL controller will increment this field by one and place the result in the Status Count Output field of the SDC Status register.
	SDC_DEBUGDATA_IN[0:31]	In	Contains the SDC debug write data. The data is validated by an active Debug Register Enable with a write command.
	SDC_DEBUGADDR[0:15]	In	Contains the SDC debug address for read and write commands. The address is validated by an active Debug Register Enable with a read/write command. See “SDC Debug Interface Address Map.”
	SDC_STATUSREG[0:31]	Out	SDC Status Register 0:7 DASL Control Code Version. 8:15 DASL Control Code Revision. 16:17 Reserved. All bits are set to zero. 18 Parity Error. A parity error was detected on a local store or instruction RAM read. Active high. 19 Port Quality Error. A logical “or” of the SDC_PORTQUALITY output. When active, indicates that the shared DASL controller has detected a minimum eye error on a port. This error indicates that one or more of the DASLs that make up the port is not operating within specification. 20:23 Current Port Identification. Displays the number of the port currently being processed by the shared DASL controller. 24:31 Status Count Output. Written by the shared DASL controller to be one greater than the value present in the Status Count Input field of the SDC debug control input bus. Serves as a watchdog mechanism to allow the application to monitor the shared DASL controller.
	SDC_DEBUGDATA_OUT[0:31]	Out	Contains the SDC debug read data, which is validated by an active SDC Debug Operation Complete. On write commands, this bus will contain the SDC debug write data.
	SDC_DEBUGDATA_VALID	Out	SDC Debug Operation Complete is active high for one OSC_125_DIV4 clock cycle to validate the data on the SDC_DEBUGDATA_OUT bus.

5.2 Resets

5.2.1 SDC_RESET (M3 Reset)

The DASL processor reset must be active during picocode download. Activate SDC_RESET during DASL reset (CORE_RESET).

5.2.2 CORE_RESET (DASL Reset)

The CORE_RESET signal resets the DASL. To insure proper reset, maintain the CORE_RESET signal for at least 500 ns.

Both SDC_RESET and CORE_RESET signals are synchronous resets and, therefore, require a clock to be performed.

5.3 Picocode Download

The instruction memory for the shared DASL controller is accessible through the SDC Internal Resource Interface (SDCIRI). The processor is given a separate reset so that it can be disabled until the instruction memory is loaded. The SDC_RESET signal must be held active until the instruction memory is completely loaded. Once the picocode is completely loaded, release the SDC_RESET to start the processor.

5.3.1 Picocode Write

A picocode write operation is performed using the M3 picocode access registers (DASL_M3_Picocode_X and DASL_M3_Picocode_Y). Data Instruction, Instruction Memory Address, and Write Enable bits must be written in the SDC access register. The hardware handles the transfer in the instruction memory. Contiguous operations can be performed until the picocode is completely downloaded.

5.3.2 Picocode Read

A picocode read operation is performed using the M3 picocode access registers (DASL_M3_Picocode_X and DASL_M3_Picocode_Y). Instruction Memory Address and Read Enable bits must be written in the SDC access register. The hardware handles the read operation.

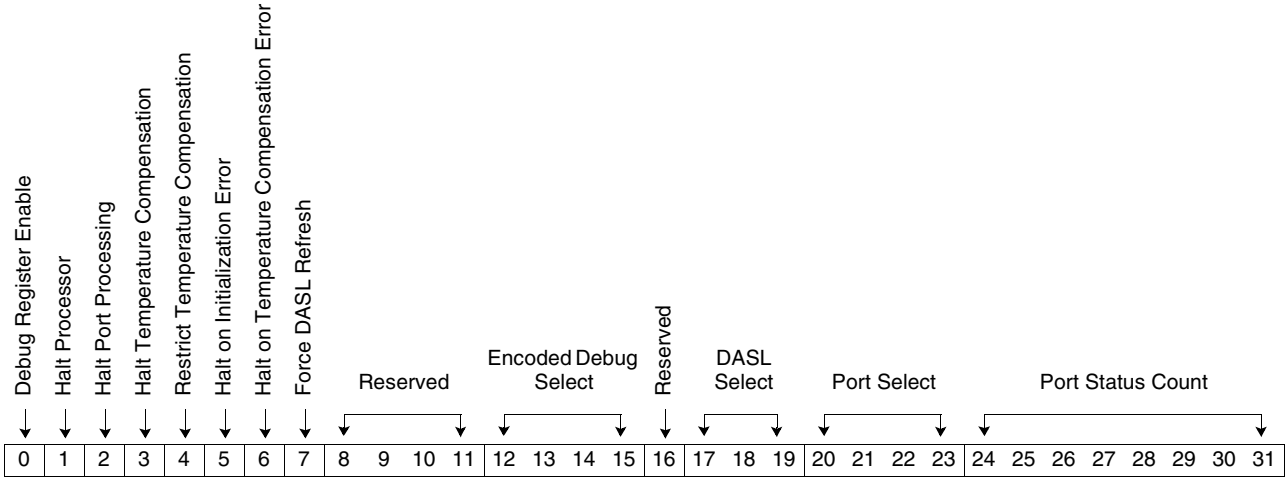
The SDC access register shall be polled until the Read Completed bit is detected to be on (active high). When this bit is on, the data contained in the SDC access register is valid and corresponds to the selected instruction memory address.

5.4 SDC_INTERRUPT Signal

A high level on SDC_INTERRUPT (M3 interruption in the Event_1_X and Event_1_Y registers) denotes an interrupt or a parity error condition. If a parity error is detected on the instruction memory or the local data store, an interrupt will be generated and remain active until the shared DASL controller is reset.

5.5 SDC Debug Interface

The SDC debug interface gives the application read-and-write access to any of the resources available to the processor. Access includes local store, sample memory, and any hardware-assist registers addressable by the processor (access to instruction memory is provided through SDCIRI). The interface includes a 32-bit debug control input, a 32-bit debug data output, a 32-bit debug data input, a 16-bit debug address input, and a 1-bit debug data valid output. The application requests a service offered by the processor via the debug control input. The results are returned by the processor on the debug data output. Debug control input field definitions are shown below:

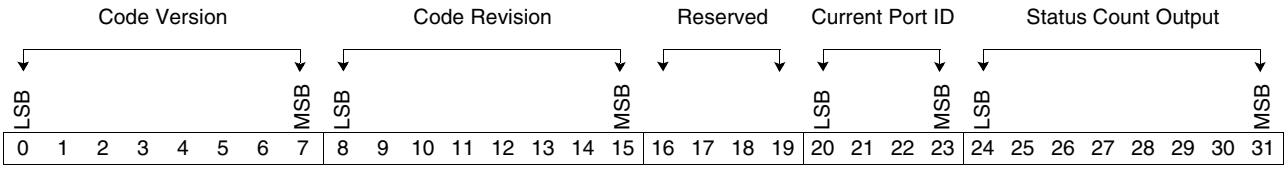


Bit(s)		Field Name	Description
Word Mode	Byte Mode		
0	0	Debug Register Enable	When on high, this signal enables debug mode. When on low, the rest of the bits in the Debug Control Input will be ignored, with the exception of the Port Status Count field.
1	1	Halt Processor	When set, the M3 picoprocessor stops all processing.
2	2	Halt Port Processing	When set, the M3 picoprocessor stops all processing, but continues to update the status and respond to debug requests.
3	3	Halt Temperature Compensation	When set, the M3 picoprocessor does not perform any port processing functions beyond initialization.
4	4	Restrict Temperature Compensation	When set, the M3 picoprocessor performs all port processing functions, but the multiplexer setting is not adjusted beyond initialization.
5	5	Halt on Initialization Error	When set, the M3 picoprocessor stops all processing after the next initialization error.
6	6	Halt on Temperature Compensation Error	When set, the M3 picoprocessor stops all processing after the next data mode.
7	7	Force DASL Refresh	When set, the M3 picoprocessor writes the current DASL receiver settings to all ports that have completed initialization, but does not perform data mode compensation.
8:11	0:3	Reserved	Reserved.

Bit(s)		Field Name	Description
Word Mode	Byte Mode		
12:15	4:7	Encoded Debug Select	The value of this field indicates which service the picocode should perform. Valid values: 0000 No operation. 0001 Request a read to the address given by the Debug Address. 0010 Request a write to the address given by the Debug Address. 0100 Dump local store memory. 0101 Load sample memory. 0110 Dump sample memory. 1000 Request a delay line sample from the DASL receiver specified by the Port Select and DASL Select fields. 1001 Update the DASL Data Structure with the Debug Data Input for the DASL receiver specified by the Port Select and DASL Select fields. Others Reserved.
16	0	Reserved	Reserved. Should be low.
17:19	1:3	DASL Select	An encoded value that selects the DASL receiver for a given action. If the supplied DASL value is out of range, the request will be processed for DASL 0.
20:23	4:7	Port Select	An encoded value that selects the port for a given action. A request that utilizes the Port Select field is processed at the next service time for the selected port. If the supplied port value is out of range, the request will be processed for Port 0.
24:31	0:7	Port Status Count	This 8-bit field will be read by the picoprocessor, incremented, and written back out of the SDC_Status_Reg_X register output.

5.6 Status Register

The status register contains various information about the processor status. The output of this register is connected to the SDC_Status_Reg_X register output. The status register definitions are shown below.



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
0:7	0:7	C_V	Code Version. Identifies the code version.
8:15	0:7	C_R	Code Revision. Identifies the revision code version.
16:19	0:3	Reserved	Reserved.
20:23	4:7	CP_ID	Current Port ID. Identifies the DASL port undergoing picocode processing.
24:31	0:7	ST_CO	Status Count Output. Reports the output from the Port Status Count register incremented by the picoprocessor.

5.7 DASL Initialization and Operation

Once the device has been fully configured, but before actual data traffic can take place between the converter and a switch, the DASL interfaces must be initialized to provide bit phase alignment and packet alignment at the data receivers in both directions. DASL initialization requires communication between two devices: a converter and a switch core port.

The port synchronization is under the overall control of the system Control Processor, which coordinates the operation between the switch core and the adapters. Synchronization between the switch control and the port adapter can also be performed directly through the interface lines, fabric port available (FPA), and adapter port available (APA).

The registers of interest at both ends of the link are:

6. Port Enable register
- No Signal register
- Sync Status and Sync Hunt registers
- Sync Packet Transmit register
- Signal Detect Interrupt in Status register

The Sync Status register reports the status of the input receiver, and the Sync Hunt register forces the input ports to start the synchronization sequence.

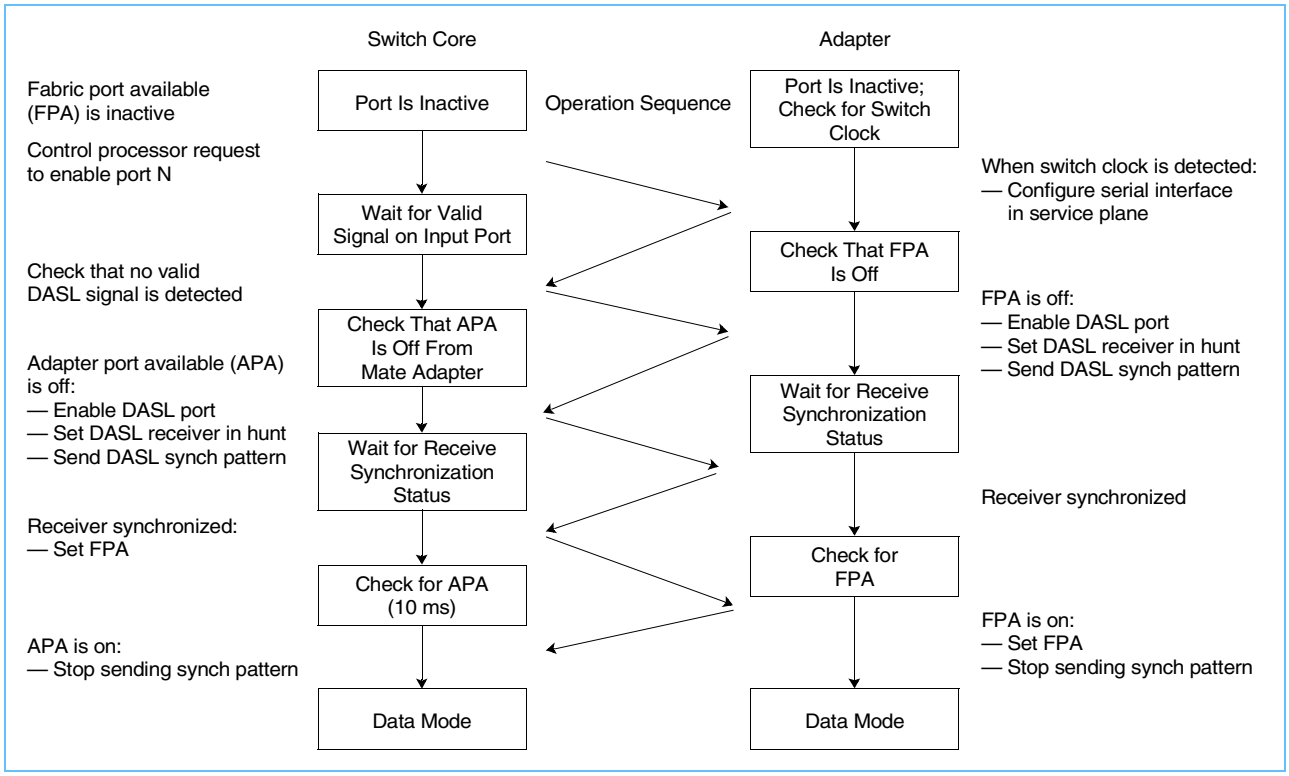
The Sync Packet Transmit register specifies that synchronization packets must be transmitted in order to synchronize the remote device input port. When not transmitting synchronization packets, the output ports transmit normal traffic packets (that is, data packets or idle packets).

The following steps must be taken to synchronize input ports, either after reset and initialization of the device or when the control processor decides to resynchronize a link due to data errors on the incoming links. Even if the same steps are taken on both the switch port and the converter device, they do not need to be synchronous. The global sequence of operation (below) must be followed:

1. Disable the switch and converter ports.
2. Enable the switch and converter ports by writing ‘1’ into the Port Enable register.
3. Disable DASL transmission by disabling Transmit Synch Enable.
4. Check for valid connectivity of the receiver to a differential transmitter through the No Signal register. This ensures the integrity of the serial links.
5. Enable Transmit Sync packets.
6. Enable DASL transmission by writing ‘1’ in Transmit Synch Enable.
7. Write ‘1’ into the Sync Hunt register for the enabled ports to start synchronization.
8. Poll the Sync Status register to verify completion of synchronization after a Sync Time-Out period. If the port fails to synchronize, its Sync Status bits will be ‘0’.
9. When synchronization has been achieved, the local processor at each end reports to the control processor that it is ready for data transfer.
10. Clear any Cyclic Redundancy Check (CRC) error indication that might have been set up during the synchronization period.
11. Upon receipt of both reports, the control processor indicates to both ends of the full duplex link (switch port and converter) to stop transmitting Sync packets. Normal packet transfer (idle or data) on the input ports can then be initiated.

12. As the link is now in data mode, both the switch control and the adapter controller have to poll the CRC error registers and the No Signal register to check that the receiver is synchronized for error-free operation. This operational sequence is mapped in Figure 5-2.

Figure 5-2. Switch Fabric DASL Port Synchronization Sequence

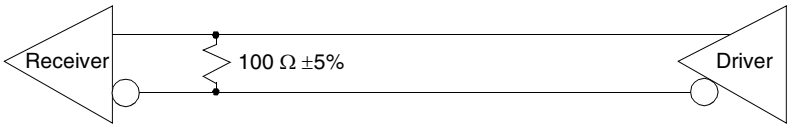


5.8 Line Termination

5.8.1 DASL and SYS_CLK

The DASL data inputs (DASL_X_TX, DASL_Y_TX) and the clock reference (SWITCH_X_CLK and SWITCH_Y_CLK) use differential HSTL Electronics Industries Association/JEDEC (EIA/JESD8-6) standard-compliant I/O books. Figure 5-3 gives the recommended termination for the receiver lines.

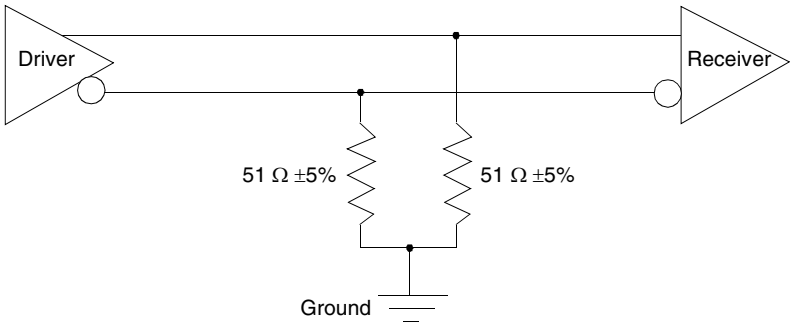
Figure 5-3. DASL Termination



The termination network must be placed within 2.5 cm of the receiver device.

Note: For a switch clock X/Y differential pair, both termination resistors must be directly connected to ground (GND), without the use of the 100-pF capacitor.

Figure 5-4. Clock Termination



6. Phase-Locked Loop (PLL)

6.1 PLL Configuration

During device power-on reset (POR), the PLL is held in reset until software releases the PLL _RESET bit in the PLL register. Before starting the PLL (by releasing the PLL_RESET bit), the PLL_RANGE, PLL_MULT, and PLL_TUNE bits must be written in the PLL register(s). Once the PLL is started, software polls the PLL register for PLL_LOCK bit detection. When the PLL_LOCK bit is detected high, the logic clocked by the PLL is operational.

6.2 PLL_RESET

A PLL_RESET[15] field is provided in the Switch_X_PLL, Switch_Y_PLL, and PE_PLL registers.

The reset function puts the PLL in bypass mode so that the output clock is identical to the input reference clock. PLL_RESET should be held active (high) during power on until all of the following conditions are met:

- All PLL inputs are stable and at their final values.
- The reference clock is stable.
- PLL V_{DDA} and V_{DD} are at their final values.

A reset is also required if the PLL inputs change after power on.

6.3 PLL_RANGE and PLL_MULT

PLL_RANGE[5:0] and PLL_MULT[31:28] fields are provided in the Switch_X_PLL, Switch_Y_PLL, and PE_PLL registers. Use these programmable inputs to choose the output frequency of the PLL. The logic state of these inputs must be stable before the PLL can begin to lock.

6.4 PLL_Tune

A PLL_TUNE[13:8] field is provided in the Switch_X_PLL, Switch_Y_PLL, and PE_PLL registers. These programmable inputs are used to optimize the PLL stability and jitter. The logic state of these inputs must be stable before the PLL can begin to lock.

6.5 PLL_LOCK

A PLL_LOCK[14] field is provided in the Switch_X_PLL, Switch_Y_PLL, and PE_PLL registers. This signal indicates when the feedback clock is in phase with the reference clock. While PLL_RESET is high, PLL_LOCK will be low. Following reset, PLL_LOCK will stay low until lock is achieved.

The PLL_LOCK signal will go high less than 300 µs after one of the following occurs:

- The reference clock is stabilized at a constant frequency
- The PLL_RANGE and PLL_MULT inputs are at their final states
- The V_{DDA} input is at the rail

PLL_LOCK will return to a low state, if the PLL loses lock with the reference clock.

6.6 PLL Settings

Table 6-1 gives the recommended values for the PRS28.4G PLL settings.

Table 6-1. PRS28.4G PLL Settings

Settings (PLL Registers)	IBM Packet Routing Switch PRS28.4G	Switch Operating at 125-MHz Byte Clock
Reference Clock	55 MHz	62.5 MHz
PLL_RANGA[2:0]	010	010
PLL_RANGB[5:3]	101	101
PLL_MULT[31:28]	0010	0010
PLL_TUNE[13:8]	010011	010011
VCO Frequency	660 MHz	750 MHz

Note: If the PE PLL is used with a 55-MHz reference clock, the same settings are used except for the reserved PLL_RANGEB bits.

Table 6-2 presents some common PLL frequency settings along with the PLL configuration register settings to enable the desired operation. Other frequency settings are possible, but the following examples are the most common PE PLL settings.

Table 6-2. PE PLL Programming Examples

Input Frequency	Output Frequency	Range	Multiplier	VCO	Tune
50	100	001	0010	700[1]	010011
		010		600	010011
		011		500	010011
100	100	001	0001	700[1]	010011
		010		600	010010
		011		500	010010
55	110	001	0010	770[1]	010011
		010		660	010011
		011		550	010011
		100		440	010011
110	110	001	0001	770[1]	010011
		010		660	010010
		011		550	010010
		100		440	010001
62.5	125	010	0010	750[1]	010011
		011		625	010011
		100		500	010011
125	125	010	0001	750[1]	010010
		011		625	010010
		100		500	010001

1. This is the recommended setting because it is the highest VCO frequency that corresponds to the minimum clock jitter.

7. JTAG Description

The IBM Packet Routing Switch Serial Interface Converter complies with the IEEE Standard Test Access Port and Boundary-Scan Architecture for testing and debugging components assembled at the board level. (See “IEEE Standard Test Access Port and Boundary-Scan Architecture,” doc. IEEE Std. 1149.1-1990, and the IBM ASIC Products Application Note “IEEE 1149.1 Boundary-Scan in IBM ASICs,” 11/97, version 4.)

Joint Test Action Group (JTAG) test architecture consists of a Test Access Port (TAP) and associated controller, an Instruction register, and three Test Data registers. The three Test Data registers are the Bypass register, the IDcode register, and the Boundary Scan register.

The TAP is a general-purpose port that provides access to the implemented test support functions defined by the JTAG Standard. It consists of five ports: test clock input (TCK), test mode select input (TMS), test data input (TDI), test reset input (TRST), and test data output (TDO). The TAP controller is a synchronous finite-state machine that responds to changes at the TMS and TCK signals and controls the sequence of operations of the internal test logic. It generates the clock and control signals required to shift data down the Instruction register and Test Data registers. These registers constitute separate shift register-based paths that are connected, in parallel, between TDI and TDO.

The JTAG Instruction register is a three-bit shift register that the user programs to specify the desired JTAG instruction. Table 7-1 specifies the seven supported JTAG instructions and the binary operation code for each.

Table 7-1. Supported JTAG Instructions

Instruction Name	Instruction Operation Code (binary)
Extest	000
Intest	001
Sample	010
IDcode	011
Hi-Z	100
Clamp	110
Bypass	111

The Bypass register is a one-bit shift register and is scannable during the Bypass instruction. It provides a minimum length serial path to move test data between TDI and TDO. Use the Bypass register to speed access to JTAG registers in other components on a board-level test data path.

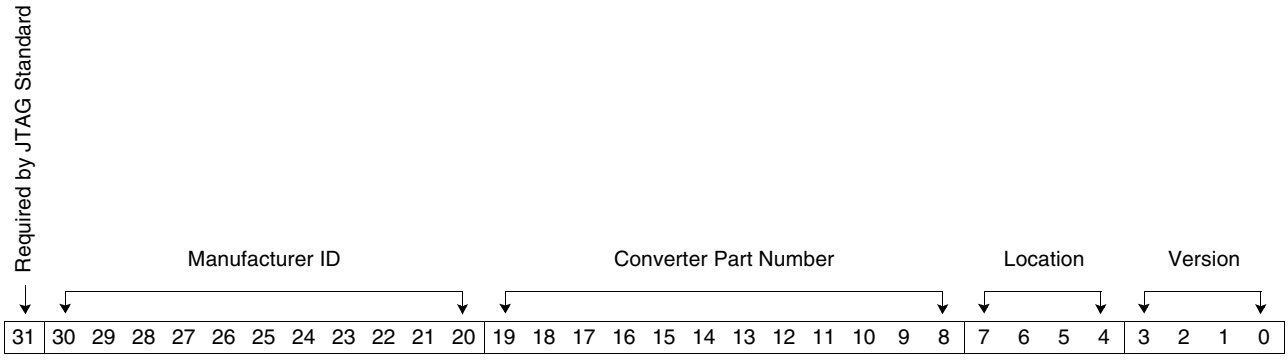
The Boundary Scan register is a shift register that allows sampling and/or forcing of signals flowing into and out of the system logic through the system ports.

During JTAG operation, certain input pins must be at specific values, as indicated in Table 7-2. All signals but the Receiver Inhibit (RI) signal are already internally tied up or tied down and do not need any user-forced action. The RI signal must be forced to ‘1’ externally.

Table 7-2. JTAG Compliance Pattern

Signal Name	Required Setting
CE0_IO	0
CE0_Scan	0
CE0_TEST	0
CE1_A	1
CE1_B	1
TEST_B2	1
CE1_C1	1
CE1_C2	1
TEST_C3	1
LT	1
DI1	1
DI2	1
RI	1

The IDcode register is a 32-bit set/reset latch (SRL), x‘3442 3600’. Binary values are shown below.



Bit(s)		Field Name	Description
Word Mode	Byte Mode		
31	N/A	Required by JTAG Standard	Defaults to ‘0’ for JTAG indication.
30:20		Manufacturer ID	Defaults to ‘0110 1000 100’ for IBM.
19:8		Converter Part Number	Defaults to ‘0010 0011 0110’ for the converter ID.
7:4		Location	Defaults to ‘0000’ for Burlington, Vermont, USA.
3:0		Version	Defaults to ‘0000’ for the version used.

8. I/O Signal Definitions

8.1 Signal Descriptions

All functional signals are 3.3-V low-voltage transistor-transistor logic (LVTTL)-compatible for drivers and receivers, except the following:

- Protocol engine interface
- Protocol engine clocks provided by the converter
- Back-pressure serial link
- Level-sensitive scan design (LSSD) and JTAG test signals

These signals are based on the tri-state driver/receiver (BP2550 type) that interfaces 2.5-V internal functions with 3.3 V-tolerant 2.5-V CMOS drivers and receivers off of device bidirectional data buses. The driver is 50-Ohm source-terminated.

The switch fabric clocks are balanced at high-speed transceiver logic (HSTL) levels.

Table 8-1. Test Signals (Page 1 of 2) Overbars Indicate Signals that are Active Low

Signal Name	Type	Level	Description	Notes
$\overline{DI1}$		LVCMOS	Non-test driver inhibit for all device boundary outputs. 0 Boundary outputs are disabled and in tri-state. 1 Inactive: all boundary outputs are controlled by normal functions. An internal pull-up resistor forces the inactive state. Boundary outputs are device outputs or common I/Os that serve as primary outputs of the internal boundary logic. Fed directly by boundary latches or special boundary logic books that make up the boundary logic.	
$\overline{DI2}$	Input	LVCMOS	The test driver inhibit for all device nonboundary outputs. 0 Nonboundary outputs are disabled and in tri-state. An internal pull-up resistor forces the inactive state. 1 Inactive: all nonboundary outputs are controlled by normal functions. Nonboundary outputs are device outputs or common I/Os that bring test function and LSSD data directly to and from the internal boundary logic.	
$\overline{RI}$	Input	LVCMOS	Gates all boundary receivers during internal test to prevent unknown states from entering the internal logic and to reduce switching activities. The RI pad must be tied up externally for system mode. When active, all boundary receivers are placed in a known state independent of the receiver input.	
CE1_A	Input	LVCMOS	External source of the internal set/reset latch (SRL) scan A clock used during an LSSD test to enable the tester to independently source the internal SRL clocks from the primary inputs.	1

1. An internal pull-up resistor forces the inactive state.
2. An internal pull-down resistor forces the inactive state.
3. The signal must be kept low during normal PLL operation.

Table 8-1. Test Signals (Page 2 of 2) Overbars Indicate Signals that are Active Low

Signal Name	Type	Level	Description	Notes
CE1_B	Input	LVCMOS	External source of the internal SRL scan B clock used during an LSSD test to enable the tester to independently source the internal SRL clocks from the primary inputs.	1
TEST_B2	Input	LVTTL	External source of the internal SRL scan B clock used during an LSSD test to enable the tester to independently source the internal SRL clocks from the primary inputs.	1
CE1_C1	Input	LVCMOS	External source of the internal SRL scan C clock used during an LSSD test to enable the tester to independently source the internal SRL clocks from the primary inputs (used for logic).	1
CE1_C2	Input	LVCMOS	External source of the internal SRL scan C clock used during an LSSD test to enable the tester to independently source the internal SRL clocks from the primary inputs (used for RAM).	1
CE0_IO	Input	LVCMOS	Used to force the JTAG EXTEST operation for IBM test methodology purposes.	2
CE0_Scan	Input	LVCMOS	Gates both the A and B LSSD test clocks.	2
CE0_TEST	Input	LVCMOS	Forces ‘0’ in system mode and ‘1’ in LSSD test mode.	2
TEST_C3	Input	LVTTL	External source of the internal growable RAM array (GRA) scan C clock used during an LSSD test to enable the tester to independently source the internal GRA clocks from the primary inputs.	1
PE_TESTIN	Input	LVCMOS	Programs the PLL to perform parametric testing at the wafer and module level.	3
SWITCH_X_TESTIN	Input	LVCMOS	Programs the DASL PLL for fabric X to perform parametric testing at the wafer and module levels.	3
SWITCH_Y_TESTIN	Input	LVCMOS	Programs the DASL PLL for fabric Y to perform parametric testing at the wafer and module levels.	3
PE_TESTOUT	Output	LVCMOS	Monitors TESTOUT output during PLL test to verify the PLL output frequency.	
SWITCH_X_TESTOUT	Output	LVCMOS	Monitors TESTOUT output during PLL test to verify the PLL output frequency.	
SWITCH_Y_TESTOUT	Output	LVCMOS	Monitors TESTOUT output during PLL test to verify the PLL output frequency.	
ABIST_CLK	Input	LVCMOS	Connected to the array built-in self test (ABIST) controller STCLK input and used only during test operation. Keep this signal inactive (tied to ground) during system mode to reduce power consumption in the BIST logic.	
ABIST_DIAGOUT	Output	LVTTL	Each SRAM DIAGOUT output is multiplexed to this ABIST_DIAGOUT PO to observe the pass/fail flag of individual arrays during the ABIST diagnostic mode. See bit 2 of the Test_Status_X_Y register for the X or Y result on that pin.	

1. An internal pull-up resistor forces the inactive state.
2. An internal pull-down resistor forces the inactive state.
3. The signal must be kept low during normal PLL operation.

Table 8-2. JTAG Interface External Signals

Signal Name	Type	Level	Description	Notes
TCK	Input	3.3-V LVTTL Receiver Tri-State Common Input/Output (CIO)	Test clock input.	1, 2
TMS	Input	3.3-V LVTTL Receiver Tri-State CIO	Test mode select input.	1, 2
TDI	Input	3.3-V LVTTL Receiver Tri-State CIO	Test data input.	1, 2
TDO	Output	3.3-V LVTTL 50-Ω Tri-State CIO	Test data output.	1, 2
TRST	Input	3.3-V LVTTL Receiver Tri-State CIO	Test reset input must be asserted during power-on reset to reset the JTAG control logic. TRST should be tied to ground (for example, through a 1K resistor) for normal operation.	1, 2

1. An internal pull-up resistor forces the inactive state.
2. See IEEE 1149.1 specification for details.

Table 8-3. Processor Interface Signals

Signal Name	Type	Level	Description
$\overline{\text{MP\_SEL}}$	Input	LVTTL	Converter select for processor access.
$\overline{\text{MP\_WR}}$	Input	LVTTL	Write/Read indicator on processor bus.
MP_PRDY	Output	LVTTL	Ready signal for transfer complete indication.
$\overline{\text{MP\_INT}}$	Output	LVTTL	Interrupt to processor.
MP_ADDR_7…MP_ADDR_0	Inputs	LVTTL	Processor bus address.
MP_ADD_PRTY	Inputs	LVTTL	Processor bus parity (optional and can be set through an interface pin).
MP_DATA_7…MP_DATA_0	Input/ Output	LVTTL	Processor data bus.
MP_DATA_PRTY	Input/ Output	LVTTL	Processor data bus parity (optional and can be set through an interface pin).
MP_PRTY_ENB	Input	LVTTL	Enables generation and checking of the microprocessor data and address parity.
MP_BURST_MODE	Input	LVTTL	Enables the operation in either single-byte mode access or in byte burst mode compatible with the Intel i960®processor. When tied to ground, the device operates in byte mode access; when tied to 3.3 V, it operates in word mode access.

Table 8-4. Converter Signals

Signal Name	Type	Level	Description
DASL_X_TX_0…DASL_X_TX_7 DASL_X_TX_0…DASL_X_TX_7	Input	HSTL	Differential (400 to 500 Mbps) signals for input port from switch X.
DASL_X_RX_0…DASL_X_RX_7 DASL_X_RX_0…DASL_X_RX_7	Output	HSTL	Differential (400 to 500 Mbps) signals for output port to switch X.
DASL_Y_TX_0…DASL_Y_TX_7 DASL_Y_TX_0…DASL_Y_TX_7	Input	HSTL	Differential (400 to 500 Mbps) signals for input port from switch Y.
DASL_Y_RX_0…DASL_Y_RX_7 DASL_Y_RX_0…DASL_Y_RX_7	Output	HSTL	Differential (400 to 500 Mbps) signals for output port to switch Y.
SEND_GNT_X	Ouput	LVTTL	0 The switch on switch board X is not allowed to send data to the converter. 1 The switch is allowed to send data to the converter. In reset mode, this signal is forced to Hi-Z.
SEND_GNT_Y	Output	LVTTL	0 The switch on switch board Y is not allowed to send data to the converter. 1 The switch is allowed to send data to the converter. In reset mode, this signal is forced to Hi-Z.
MEM_GNT_X_3…MEM_GNT_X_0	Input	LVTTL	Indicates that the shared memory is not full for a given priority. 0 The switch on switch board X cannot accept anymore data from the converter. 1 The switch can accept more data from the converter.
MEM_GNT_Y_3…MEM_GNT_Y_0	Input	LVTTL	Indicates that the shared memory is not full for a given priority. 0 The switch on switch board Y cannot accept anymore data from the converter. 1 The switch can accept more data from the converter.
$\overline{\text{DASL\_DRV\_ENB}}$	Input	LVTTL	Sets DASL drivers in Hi-Z until the board housing the converter is fully inserted. Ensures that both ends of the adapter board to which the converter is soldered are fully inserted. An internal pull-up resistor forces the inactive state. See Figure 8-1.

Note: The electrical level supported by the converter lines is called high-speed transceiver logic (HSTL). It is specified in the Joint Electron Device Engineering Council (JEDEC) JESD8-6 standard.

Figure 8-1. Fully Inserted Line Card Detection

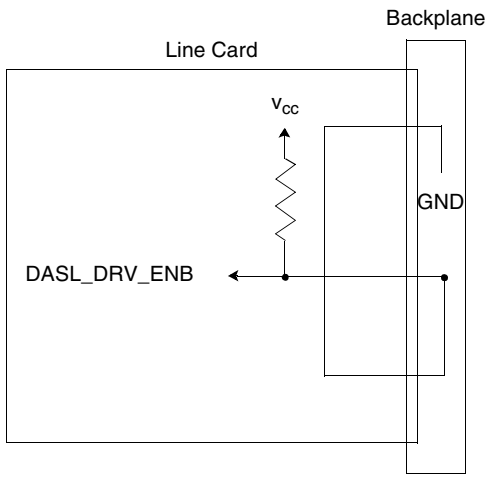


Table 8-5. PE Interface Receive Signals For a functional description, see the PE interface description (ingress and egress).

Signal Name	Type	Level	Description
RXDATA_31…RXDATA_0	Input	LVCMOS	Input data bus from the PE to the converter.
RXPRTY	Input	LVCMOS	Provides optional odd parity checking on the input data bus from the PE to the converter.
RXSOP	Input	LVCMOS	Start of packet from the PE to the converter.
RXPAV	Input	LVCMOS	Indicates that at least one packet is available in the PE.
$\overline{\text{RXENB}}$	Output	LVCMOS	Asserted by the converter during packet cycles when the PE is allowed to send data.

Table 8-6. PE Interface Transmit Signals

Signal Name	Type	Level	Description
TXDATA_31…TXDATA_0	Output	LVCMOS	Output data bus from the converter to the PE. Signals are Hi-Z when the converter is not selected.
TXPRTY	Output	LVCMOS	Provides an optional odd parity bit on the output data bus from the converter to the PE. Signals are Hi-Z when the interface is not selected.
TXSOP	Output	LVCMOS	Asserted by the converter to the PE to indicate the position of the start of packet. Signal is Hi-Z when the interface is not selected.
$\overline{\text{TXFULL}}$	Input	LVCMOS	The PE has no space available for any additional packets.
$\overline{\text{TXENB}}$	Output	LVCMOS	Asserted by the converter during packet cycles when the PE is allowed to receive data.

Table 8-7. External Clocking/PLL Signals

Signal Name	Type	Level	Description
$\overline{\text{SWITCH\_X\_CLK}}$ SWITCH_X_CLK	Input	HSTL (balanced)	Switch core X system clock differential pair used for the internal clock generation in the switch X interface side (clock frequency is 55 to 62.5 MHz).
$\overline{\text{SWITCH\_Y\_CLK}}$ SWITCH_Y_CLK	Input	HSTL (balanced)	Switch core Y system clock differential pair used for the internal clock generation in the switch Y interface side (clock frequency is 55 to 62.5 MHz).
MP_CLK	Inputs	LVTTL	Processor bus clock input: 25 to 66 MHz. This clock also drives the PE interface when no other clock has been selected by setting bits 31:30 of the Common_Control register to ‘00’ or ‘11’ (default settings).
PE_CLK	Input	LVCMOS	Clock used to drive all converter PE side actions. Clock source can drive the PE interface by setting bits 31:30 of the Common_Control register to ‘01’.
FROM_SMOOTH_PLL_OUT	Input	LVTTL	Clock derived from the in-service clock and smoothed by an external PLL in case of clock switch-over. Used to drive all converter PE side actions. Clock source can drive the PE interface by setting bits 31:30 of the Common_Control register to ‘10’.
TO_SMOOTH_PLL_IN	Output	LVTTL	Raw clock derived from the in-service clock source of either switch fabric derived from either the switch X or the switch Y clock source, depending on the status of the switch X or Y in-service lines from the switch core. Can be forced to be either a switch X or a switch Y clock according to the plane that has been forced in bits 22:21 of the Interrupt_Register_Indirection register. Enabling bit 26 of that register enables this signal. It is derived from the switch clock through a multiplexer and is between 52.5 and 62.5 MHz.
PE_TXCLK_out	Ouput	LVCMOS	Clock delivered by the converter that allows the transfer/synchronization of the TXDATA[31:0] and their associated controls from the converter to the PE. Clock source is determined by bits 31:30 of the Common_Control register. Enabling this clock’s driver depends on bit 8 of the Ingress_PE_Interface register.
PE_RXCLK_out	Output	LVCMOS	Clock delivered by the converter in case PE_CLK is not available on the PE layer. Allows the transfer/synchronization of the RXDATA[31:0] and their associated controls from the PE to the DASL device. Clock source is determined by bits 31:30 of the Common_Control register. Enabling this clock’s driver depends on bit 10 of the Ingress_PE_Interface register.
Shadow_RXclock_Out	Output	LVCMOS	Clock delivered by the converter to allow a matched sampling with the receive data coming from the PE. It can be connected to either an on-board delay line or the attached PE to provide (along with Shadow_RXclock_In) a clock phase incurring the same delay as the data. Enabling this clock’s driver depends on bit 10 of the Ingress_PE_Interface register. This clock is at the rate of the PE interface (that is, from 50 to 125 MHz).
Shadow_RXclock_In	Input	LVCMOS	Clock derived from the Shadow_RXclock_Out after having passed through either an on-board delay line or the PE. It can be used to sample the ingress receive data.
SWITCH_X_VDDA	Input	PLL Analog V_{DD}	Required to get a dedicated filtered voltage to switch X of the PLL.
SWITCH_Y_VDDA	Input	PLL Analog V_{DD}	Required to get a dedicated filtered voltage to switch Y of the PLL.
PE_VDDA	Input	PLL Analog V_{DD}	Required to get a dedicated filtered voltage to the PLL PE. Must be connected to 2.5 V.

To provide isolation from the noisy internal digital V_{DD} signal, V_{DDA} is brought to a package pin. If little noise is expected at the board level, then V_{DDA} can be connected directly to the digital V_{DD} plane. In most circumstances, it is prudent to place a filter circuit on V_{DDA} as shown in Figure 8-2. All wire lengths should be kept as short as possible to minimize coupling from other signals.

Figure 8-2. V_{DDA} Filtering

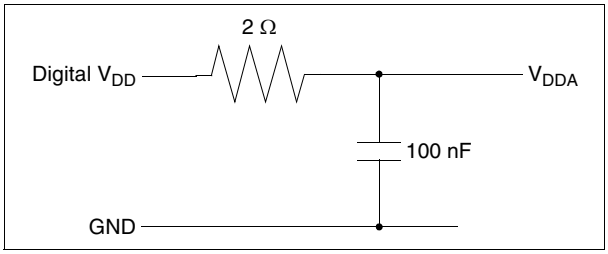


Table 8-8. Back-Pressure Serial Link Signals

Signal Name	Type	Level	Description
START_GCXFR	Output	LVCMOS	Starts the transfer of the switch grant information asserted by the converter to the PE to indicate the position of the start of the overall priority cycle in a superframe. The superframe is made up of as many frames as there are priorities in use. This signal is Hi-Z when the interface is not selected.
ODD_OQG	Output	LVCMOS	Contains the information per priority related to switch output queues 0-7 and 16-23. This signal is Hi-Z when the interface is not selected.
EVEN_OQG	Output	LVCMOS	Contains the information per priority related to switch output queues 8-15 and 24-31. This signal is Hi-Z when the interface is not selected.
SHARED_GNT	Output	LVCMOS	In a frame, indicates the relevant priority on the odd/even output queue grant (OQG) serial link and carries the global shared memory grant. The last bit of each frame carries the odd parity bit computed on all data bits in the frame. This signal is Hi-Z when the interface is not selected.

Table 8-9. Miscellaneous External Signals

Signal Name	Type	Level	Description	Notes
$\overline{\text{POR}}$	Input	LVTTL	Creates a hardware reset of the converter (flushes LSSD).	1
$\overline{\text{Slot\_IDN\_4}}$…$\overline{\text{Slot\_IDN\_0}}$	Input	LVTTL	Hardware slot ID. These bits are directly mapped to SlotID, bits 20:16, of the Common_Control register.	1
$\overline{\text{APAN\_X}}$	Output	LVTTL	Adapter Port Available (APA) signal sent to the switch board X. This bit is directly mapped, with inversion, from XAPA, bit 19, of the Control_X_PATH register.	
$\overline{\text{APAN\_Y}}$	Output	LVTTL	APA signal sent to the switch board Y. This bit is directly mapped from YAPA, bit 19, of the Control_Y_PATH register.	
$\overline{\text{FPAN\_X}}$	Input	LVTTL	Fabric Port Available (FPA). This bit is directly mapped to XFPAE, bit 2, of the Event_2_X_and_Y register.	1
$\overline{\text{FPAN\_Y}}$	Input	LVTTL	FPA. This bit is directly mapped to YFPAE, bit 6, of the Event_2_X_and_Y register.	1
$\overline{\text{SWITCH\_X\_INSERVICE}}$	Input	LVTTL	Fabric X in service selects which plane and clock are currently in use. This bit is directly mapped, with inversion, to XInServE, bit 0, of the Event_2_X_and_Y register.	1
$\overline{\text{SWITCH\_Y\_INSERVICE}}$	Input	LVTTL	Fabric Y in service selects which plane and clock are currently in use. This bit is directly mapped, with inversion, to YInServE, bit 4, of the Event_2_X_and_Y register.	1
$\overline{\text{SWITCH\_X\_PRESENT}}$	Input	LVTTL	Fabric X detects when a switch board is inserted into the backplane and that a switch clock should be present. This bit is directly mapped to XPresent, bit 3, of the Event_2_X_and_Y register.	1
$\overline{\text{SWITCH\_Y\_PRESENT}}$	Input	LVTTL	Fabric Y detects when a switch board is inserted into the backplane and that a switch clock should be present. This bit is directly mapped to YPresent, bit 7, of the Event_2_X_and_Y register.	1

1. An internal pull-up resistor forces the inactive state.

Figure 8-3. Switch Present Detection

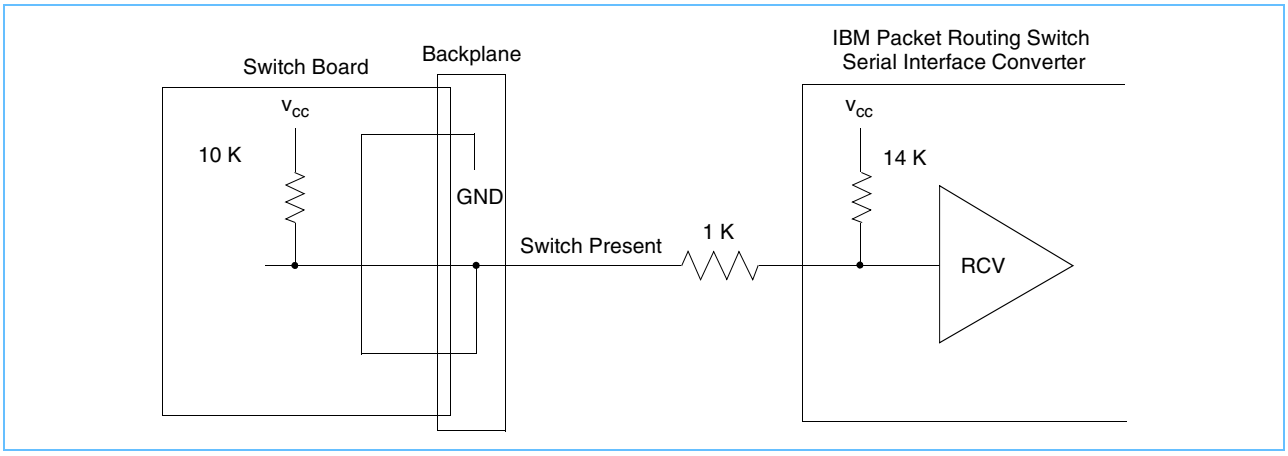


Table 8-10. Spare Signals Used to Carry Additional DC Voltages

Signal Name	Type	Level	Description
DDV1	Input	V_{DD1}	Voltage I/O connected to V_{DD1}/2.5 V.
DDV2	Input	V_{DD1}	Voltage I/O connected to V_{DD2}/2.5 V.
DNG1	Input	GND	Voltage I/O connected to GND.
DNG2	Input	GND	Voltage I/O connected to GND.

Table 8-11. External Debugging Signals

Signal Name	Type	Level	Description
AC_TEST_in	Input	LVCMOS	Test I/O used to determine the DASL macro propagation delay.
AC_TEST_out	Output	LVCMOS	Test I/O used to determine the DASL macro propagation delay (based on 12 DASL delay lines).
PE_PLLLOCK	Output	LVCMOS	Test I/O used to determine the lock state of the PE PLL.
SWITCH_X_PLLLOCK	Output	LVCMOS	Test I/O used to determine the lock state of the switch X PLL.
SWITCH_Y_PLLLOCK	Output	LVCMOS	Test I/O used to determine the lock state of the switch Y PLL.
TEST_CLK	Output	LVCMOS	External oscillator clock input: 50 to 62.5 MHz.
DBG_BusSELECT_0[15:0] and DBG_BusSELECT_1[15:0]	Output	LVCMOS	Two 16-bit buses provide direct I/O access (logic analyzer) to the debug bus specified by DEBUG_select in the Test_Status_X_Y register.

Table 8-12. DBG_SELECT Bus Definition (Page 1 of 5)

Test_Status_X_Y Register		Description
Bits 7:3	Bits 15:11	
00000	00000	Debug bus not used; DBG_DATA bus is tri-stated.
00001	00001	Data movement monitoring. Bits Description 15 Switch _Y_FREQOUT bit 1_padout (clockgen island) 14 Switch_X_FREQOUT bit 0_padout (clockgen island) 13-8 Reserved 7 Egress packet clock EDI Y (sop_o_TEBUF) 6 Egress packet clock EDI X (sop_o_TEBUF) 5 Ingress packet clock ISEQ Y (pkt_clk_O_TIBUF) 4 Ingress packet clock ISEQ X (pkt_clk_O_TIBUF) 3 YUMTX: Data packet transmitted indicator at ingress Y switch interface 2 YUMRX: Data packet received indicator at ingress Y switch interface 1 XUMTX: Data packet transmitted indicator at ingress X switch interface 0 XUMRX: Data packet received indicator at ingress X switch interface
00010	00010	M3_debug 0 (16 bits) X Bits Description 15 M3 oscillator (OSC_125 → OSC_DIV4 with C_Clock) 14 Reserved 13-11 ALU status bits (M3_DEBUG0[2:4]) 10-0 Program counter (M3_DEBUG0[5:15])
00011	00011	M3_debug 0 (16 bits) Y Bits Description 15 M3 oscillator (OSC_125 → OSC_DIV4 with C_Clock) 14 Reserved 13-11 ALU status bits (M3_DEBUG0[2:4]) 0-10 Program counter (M3_DEBUG0[5:15])
00100	00100	IDI to DASL X Bits Description 15 C_Clock 125 14 Packet clock ISEQ (Pkt_clk_0_TIBUF) 13-8 Reserved 0-7 Parallel_Data_in master LU (DASL_DATA_IN_DEBUG)
00101	00101	IDI to DASL Y Bits Description 15 C_Clock 125 14 Packet clock ISEQ (SOP_O_TEBUF) 13-8 Reserved 0-7 Parallel_Data_in master LU (DASL_DATA_IN_DEBUG)
00110	00110	DASL to EDI X Bits Description 15 C_Clock 125 14 Packet clock ISEQ (Synchro_i_fdasl) 13-8 Reserved 0-7 Parallel_Data_Out master LU (DASL_DATA_OUT_DEBUG)

Table 8-12. DBG_SELECT Bus Definition (Page 2 of 5)

Test_Status_X_Y Register		Description
Bits 7:3	Bits 15:11	
00111	00111	DASL to EDI Y Bits Description 15 C_Clock 125 14 Packet clock ISEQ (SOP_0_TEBUF) 13-8 Reserved 0-7 Parallel_Data_Out master LU (DASL_DATA_OUT_DEBUG)
01000	01000	Output queue grant priority 0 X Bits Description 15-0 GRANTP0_O[15:0]
01001	01001	Output queue grant priority 1 X Bits Description 15-0 GRANTP1_O[15:0]
01010	01010	Output queue grant priority 2 X Bits Description 15-0 GRANTP2_O[15:0]
01011	01011	Output queue grant priority 3 X Bits Description 15-0 GRANTP3_O[15:0]
01100	01100	Output queue grant priority 0 Y Bits Description 15-0 GRANTP0_O[15:0]
01101	01101	Output Queue Grant priority 1 Y Bits Description 15-0 GRANTP_1O[15:0]
01110	01110	Output queue grant priority 2 Y Bits Description 15-0 GRANTP2_O[15:0]
01111	01111	Output queue grant priority 3 Y Bits Description 15-0 GRANTP3_O[15:0]
10000	10000	Receive framing in Bits Description 15 URXCLK 14 Start_RXxfr 13 RxPRTY_error 12 Rxdata_valid 11-8 Reserved 7-0 RXDATA_L_Out[31:24] (8 bits of master LU)
10001	10001	Receive framing out Bits Description 15 URXCLK 14 SOP_to_RXfifo 13 VALID_to_RXfifo 12-8 Reserved 7-0 RXframed_data_L[31:24] (8 bits of master LU)

Table 8-12. DBG_SELECT Bus Definition (Page 3 of 5)

Test_Status_X_Y Register		Description
Bits 7:3	Bits 15:11	
10010	10010	Receive FIFO in Bits Description 15 URXCLK 14 SOP_to_RXfifo 13 VALID_to_RXfifo 12-8 Reserved 7-0 RXframed_data_L[31:24] (8 bits of master LU)
10011	10011	RXFIFO out X Bits Description 15 DASLCLK_X 14 fifo_empty 13 fifo_almost_empty 12 fifo_full 11 fifo_almost_full 10 ACK_to_RXdasl 9 SOP_from_RXdasl 8 REQ_from_RXdasl 7-0 RXfifoed_data_L[31:24] (8 bits of master LU)
10100	10100	RXFIFO out Y Bits Description 15 DASLCLK_Y 14 fifo_empty 13 fifo_almost_empty 12 fifo_full 11 fifo_almost_full 10 ACK_to_RXdasl 9 SOP_from_RXdasl 8 REQ_from_RXdasl 7-0 RXfifoed_data_L[31:24] (8 bits of master LU)
10101	10101	TXFIFO path X Bits Description 15 DASLCLK_X 14 SOP_from_TXdasl 13 fifo_empty 12 fifo_almost_empty 11 fifo_full 10 fifo_almost_full 9 VALID_from_TXdasl 8 Reserved 7-0 DATA_from_Filter[31:24] (8 bits of master LU)

Table 8-12. DBG_SELECT Bus Definition (Page 4 of 5)

Test_Status_X_Y Register		Description
Bits 7:3	Bits 15:11	
10110	10110	TXFIFO path Y Bits Description 15 DASLCLK_Y 14 SOP_from_TXdasl 13 fifo_empty 12 fifo_almost_empty 11 fifo_full 10 fifo_almost_full 9 VALID_from_TXdasl 8 Reserved 7-0 DATA_from_Filter[31:24] (8 bits of master LU)
10111	10111	TxFraming in (from FIFO X) Bits Description 15 UTXCLK 14 SOP_to_TXfifo_x 13 Hold_toTXfifo_x 12 FAF_from_TXfifo_x 11 VALID_from_TXfifo_x 10 REQ_to_TXfifo_x 9-8 Reserved 7-0 DATA_from_TXfifo_x[31:24] (8 bits of master LU)
11000	11000	TxFraming in (from FIFO Y) Bits Description 15 UTXCLK 14 SOP_to_TXfifo_y 13 Hold_toTXfifo_y 12 FAF_from_TXfifo_y 11 VALID_from_TXfifo_y 10 REQ_to_TXfifo_y 9-8 Reserved 7-0 DATA_from_TXfifo_y[31:24] (8 bits of master LU)

Table 8-12. DBG_SELECT Bus Definition (Page 5 of 5)

Test_Status_X_Y Register		Description
Bits 7:3	Bits 15:11	
11001	11001	TxFraming towards PE interface Bits Description 15 UTXCLK 14 Reserved 13 HOLD_from_SNDGRNT_GEN 12 PENDING_from_TXframing 11-8 Reserved 7-0 DATA_from_TXframing[31:24] (8 bits of master LU)
11010	11010	UTOPIA-3-like ingress interface Bits Description 15 URXCLK 14 RXSOP 13 RXPAV 12 $\overline{\text{RXENB}}$ 11-8 Reserved 7-0 RXDATA[31:24] (8 bits of master LU)
11011	11011	UTOPIA-3-like egress interface Bits Description 15 UTXCLK 14 TXSOP 13 $\overline{\text{TXFULL}}$ 12 $\overline{\text{TXENB}}$ 11-8 Reserved 7-0 TX DATA[31:24] (8 bits of master LU)

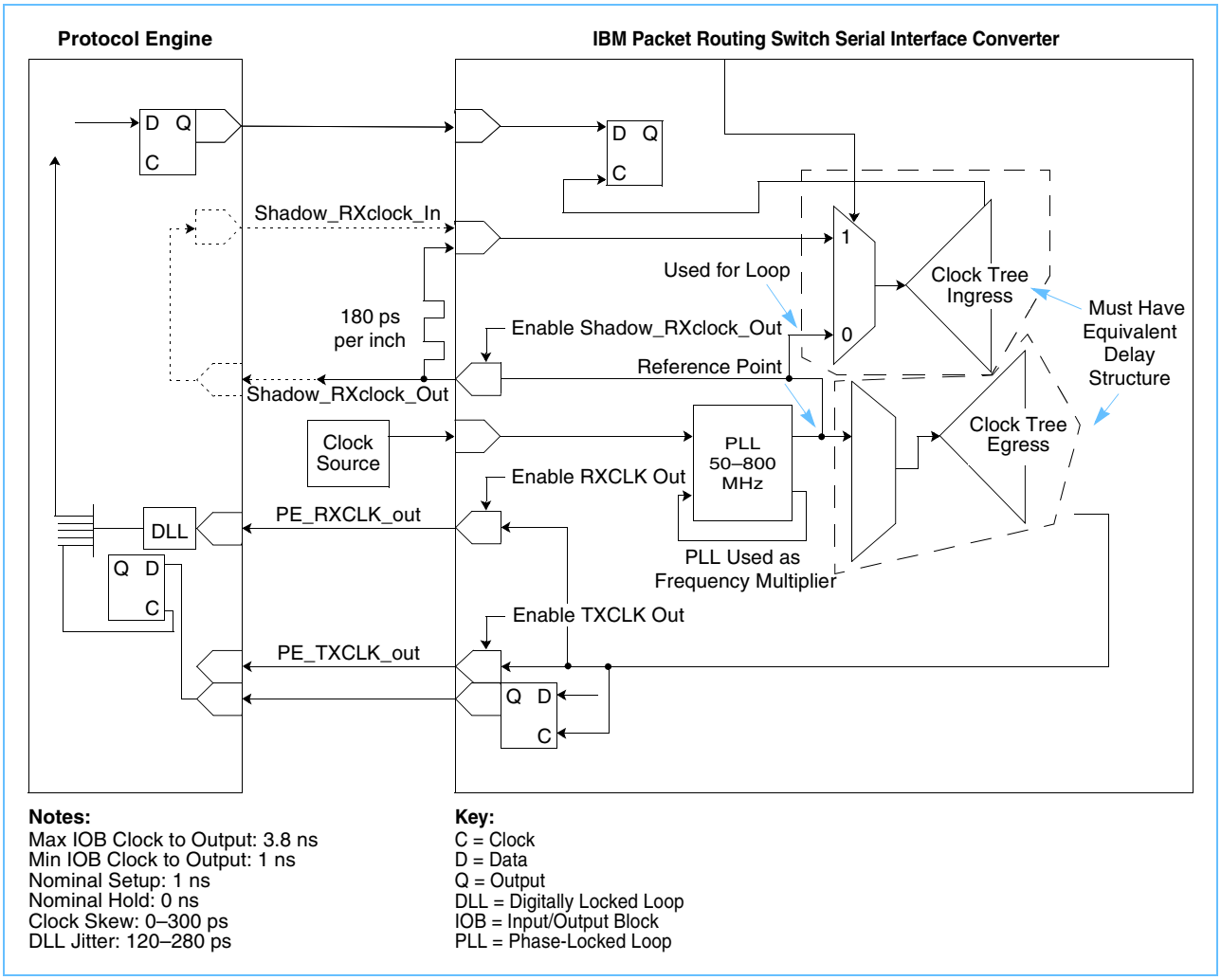
8.2 I/O Timing

8.2.1 AC Parameter Characteristics

The converter's external interfaces (UTOPIA-3-like, processor, and DASL) specify that all inputs and outputs are latch bound; thus, only setup times and hold times for inputs and clock-to-output times for outputs are needed.

Figure 8-4 illustrates the flexibility in implementing the UTOPIA-3-like interface timing.

Figure 8-4. Options for Ingress UTOPIA-3-Like Interface Clocking



8.2.2 Protocol Engine (UTOPIA-3-Like) Interface AC Ratings, Transmit

Figure 8-5. AC Parameter Transmit Timing

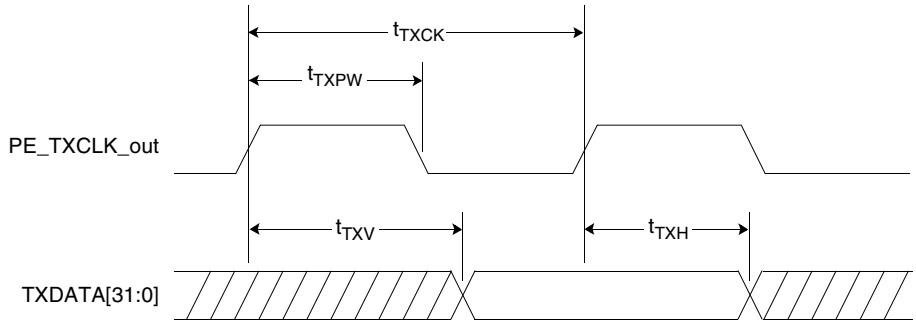


Table 8-13. Protocol Engine (UTOPIA-3-Like) Interface AC Ratings, Transmit

Symbol	Time Parameter	Rating		Unit
		Minimum	Maximum	
f_{TX}	Transmit Clock Frequency		125	MHz
t_{TXCK}	Transmit Clock Period	8		ns
t_{TXPW}	Transmit Clock Pulse Width (high or low)	3.3		ns
t_{TXV}	Transmit Clock Rising Edge to Output Valid		5.4	ns
t_{TXH}	Transmit Clock Rising Edge to Output Hold	3.5		ns
Note: Load is 15 pF. The reference clock is PE_TXCLK_out.				

8.2.3 Protocol Engine (UTOPIA-3-Like) Interface AC Ratings, Receive

Figure 8-6. AC Parameter Receive Timing

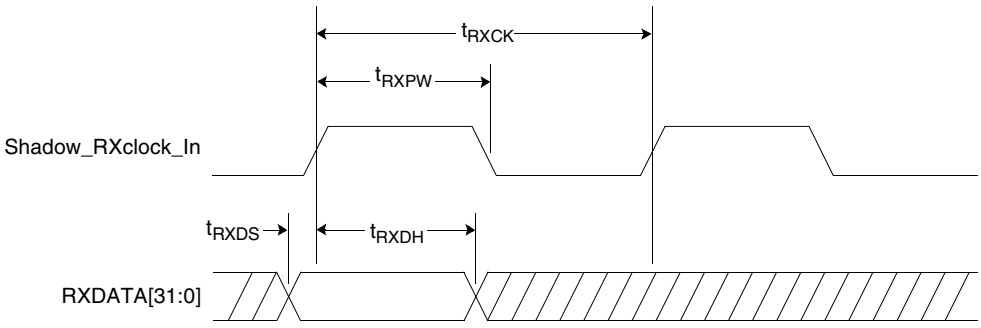


Table 8-14. Protocol Engine (UTOPIA-3-Like) Interface AC Ratings, Receive

Symbol	Time Parameter	Rating		Unit
		Minimum	Maximum	
f_{RX}	Receive Clock Frequency		125	MHz
t_{RXCK}	Receive Clock Period	8		ns
t_{RXPW}	Receive Clock Pulse Width (high or low)	3.3		ns
t_{RXDS}	Receive Data Input Setup	0.5		ns
t_{RXDH}	Receive Data Input Hold	3.5		ns
Note: The reference clock is Shadow_RXclock_In.				

8.2.4 Microprocessor Interface AC Ratings

Figure 8-7. AC Parameter Microprocessor Timing

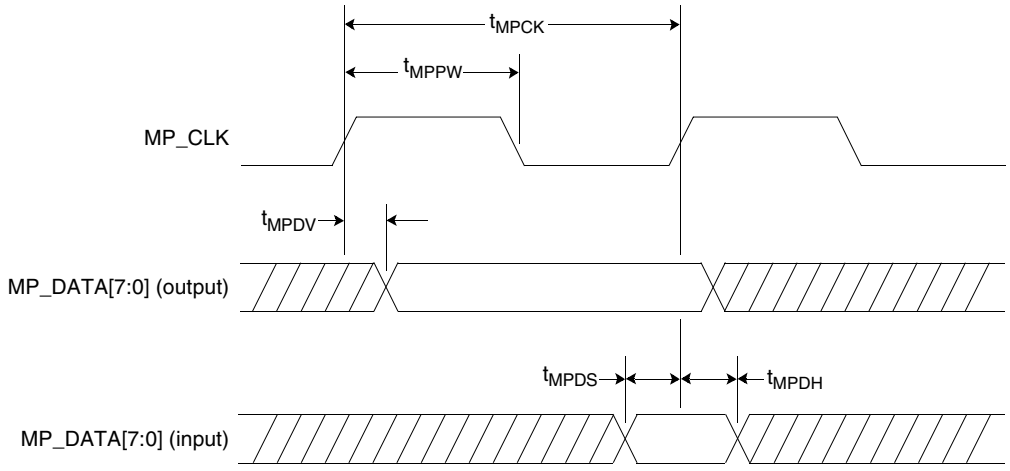


Table 8-15. Microprocessor Interface AC Ratings

Symbol	Time Parameter	Rating		Unit
		Minimum	Maximum	
f_{MP}	Microprocessor Clock Frequency		67	MHz
t_{MPCK}	Microprocessor Clock Period	15		ns
t_{MPPW}	Microprocessor Clock Pulse Width (high or low)	7		ns
t_{MPDV}	Microprocessor Clock Rising Edge to Output Data Valid	3.1	4.2	ns
t_{MPDS}	Microprocessor Data/Address Input Setup	2		ns
t_{MPDH}	Microprocessor Data/Address Input Hold	0		ns
Note: Load is 25 pF. The reference clock is MP_CLK.				

9. Electrical Specifications

Table 9-1. Absolute Maximum Ratings

Symbol	Parameter	Rating			Unit
		Minimum	Typical	Maximum	
V_{DD}	Supply Voltage	-0.5	2.5	2.7	V
V_{IN}	Input Voltage	-0.5		$V_{DD+0.6}$	V
V_{OUT}	Output Voltage	-0.5		$V_{DD+0.6}$	V
	Thermal Impedance Junction to Ambient Package (air flow = 0)		14.7		°C/W
	Thermal Impedance Junction to Ambient Package (air flow = 100 feet per minute)		13.3		°C/W
	Thermal Impedance Junction to Ambient Package (air flow = 200 feet per minute)		11.9		°C/W
	Thermal Impedance Junction to Case Package		1.9		°C/W
T_S	Storage Temperature	-65		150	°C
T_A	Operating Junction Temperature Range	0		125	°C
	Electrostatic Discharge	-3.000	6,000	3,000	V

Note: Permanent device damage may occur if the above absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in Section 1.2 , Description, on page 11. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9.1 Power Sequencing

To prevent latchup (and destruction) of the device, the power supplies must be sequenced up and down so that any supply is greater than or equal to the voltage of another supply of lesser value, both during “turn on” and “turn off” (including a quick t_{off} - t_{on} sequence).

For example, the 3.3 V supply must be greater than or equal to the 2.5 V supply which must be greater than or equal to the 1.5 V supply during power up and power down. Actually, up to 400 mV of negative voltage can be tolerated during the sequence between any two supplies. There is no time delay requirement, only a negative voltage restriction. Ideally, all supplies would rise together until they reach their operating level and all would fall together until they reach zero.

Placing a 400-mV (max.) diode between 3.3 V (cathode) and 2.5 V (anode), and another between 2.5 V (cathode) and 1.5 (anode), will ensure that the 400-mV diodes internal to the device do not get forward biased more than 400 mV, and will keep the device out of latchup conditions.

Also, the 3.3 V supply should not exceed the 2.5 V supply by more than 2.7 V during power up or down, and 1.3 V in constant use.

9.2 Recommended Operating Conditions

Table 9-2. LVCMOS-Compatible I/Os

Symbol	Parameter	Rating			Unit
		Minimum	Typical	Maximum	
V_{DD}	Supply Voltage	2.3	2.5	2.7	V
V_{IH}	Input Up Level	1.1	1.4	1.8	V
V_{IL}	Input Down Level	0.8	1.0	1.3	V
V_{OH}	High-Level Output Voltage (V_{DD} = Min, I_{OH} = -4 mA)	2.0	2.2		V
V_{OL}	Low-Level Output Voltage (V_{DD} = Min, I_{OL} = 6 mA)	Ground	0.2	0.4	V
I_{High}	2.5-V CMOS Driver, Minimum DC at Rated Voltage (V_{DD} = 2.3 V, Temperature = 100°C), V_{Low} = 2.0 V		7		mA
I_{Low}	2.5-V CMOS Driver, Minimum DC at Rated Voltage (V_{DD} = 2.3 V, Temperature = 100°C), V_{Low} = 0.4 V		9		mA
I_{IL}	Receiver Maximum Input Leakage, Low-Level Input Current at Least Positive Down Level (LPDL)	No pull up or pull down With pull down With pull up		0 0 -250	µA
I_{IH}	Receiver Maximum Input Leakage, High-Level Input Current at Most Positive Up Level (MPUL)	No pull up or pull down With pull down With pull up		0 400 0	µA
C_I	Input Capacitance, V_{DD} = Nom			5	pF

Table 9-3. LVTTL-Compatible I/Os

Symbol	Parameter	Rating			Unit
		Minimum	Typical	Maximum	
V_{DD4}	Supply Voltage	3	3.3	3.6	V
V_{IH}	Input Up Level	1.9	3.6	5.3	V
V_{IL}	Input Down Level	0	0.5	1	V
V_{OH}	High-Level Output Voltage (V_{DD} = Min, I_{OH} = -4 mA)	2.5	3.9	5.3	V
V_{OL}	Low-Level Output Voltage (V_{DD} = Min, I_{OL} = 6 mA)	Ground	0.25	0.4	V
I_{High}	3.3-V LVTTL Driver, Minimum DC at Rated Voltage (V_{DD} = 3 V, Temperature = 100°C), V_{Low} = 2.0 V		12		mA
I_{Low}	3.3-V LVTTL Driver, Minimum DC at Rated Voltage (V_{DD} = 3 V, Temperature = 100°C), V_{Low} = 0.4 V		8		mA
I_{IL}	Receiver Maximum Input Leakage, Low-Level Input Current at LPDL	No pull up or pull down With pull down With pull up		0 0 -250	µA
I_{IH}	Receiver Maximum Input Leakage, High-Level Input Current at MPUL	No pull up or pull down with pull-down with pull-up		0 400 0	µA
C_I	Input Capacitance, V_{DD} = Nom			5	pF

Table 9-4. Recommended Operating Conditions for All I/Os

Reference Signal	Parameter	Rating			Unit
		Min	Typ	Max	
DASL Driver	Rising Transition Rate of the Output	1.8	2.09	2.28	V/ns
DASL Driver	Falling Transition Rate of the Output	1.54	1.92	2.08	V/ns
DASL Receiver	Maximum Input Pin Cap		2.5		pF

Table 9-5. Power Dissipation

Supply	Power			Current		
	Nominal	Maximum	Unit	Nominal	Maximum	Unit
Total 3.3 V	0.04	0.05	W	12	14	mA
Total 2.5 V	2.05	2.39	W	820	880	mA
Total 1.5 V	0.34	0.4	W	226	261	mA
Total Device	2.43	2.84	W			

10. Pin Assignments

Figure 10-1. Pinout (25 × 25 mm CBGA Package Bottom View)
For a listing of pin assignments, see Table 10-2, Signal Pins Sorted by Grid Location.

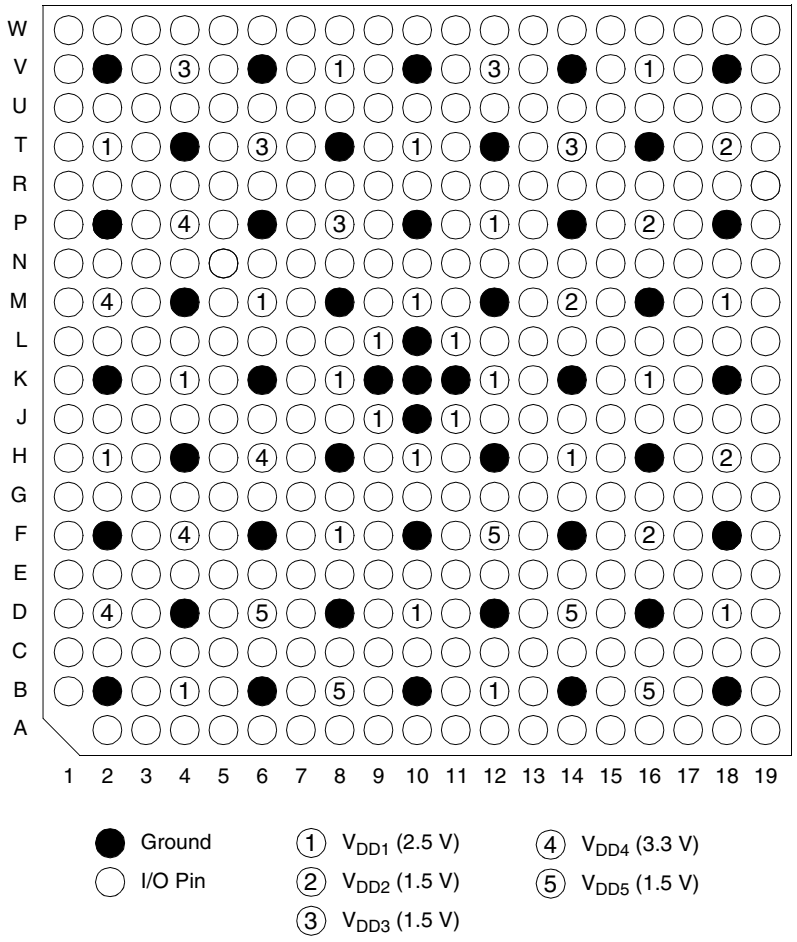


Table 10-1. Signal Pins Sorted by Signal Name (Page 1 of 4)

Signal Name	Grid Location	Signal Name	Grid Location
ABIST_CLK	E15	DASL_X_TX3	U12
ABIST_DIAGOUT	J5	$\overline{\text{DASL\_X\_TX3}}$	R12
AC_TEST_in	U6	DASL_X_TX4	W11
AC_TEST_out	V5	$\overline{\text{DASL\_X\_TX4}}$	V11
APAN_X	P1	DASL_X_TX5	N11
APAN_Y	W1	$\overline{\text{DASL\_X\_TX5}}$	R11
CE0_IO	W5	DASL_X_TX6	W10
CE0_Scan	W7	$\overline{\text{DASL\_X\_TX6}}$	U10
CE0_TEST	U5	DASL_X_TX7	R10
CE1_A	J13	$\overline{\text{DASL\_X\_TX7}}$	N10
CE1_B	R15	DASL_Y_RX0	A16
CE1_C1	L15	$\overline{\text{DASL\_Y\_RX0}}$	B15
CE1_C2	J15	DASL_Y_RX1	C17
$\overline{\text{DASL\_DRV\_ENB}}$	G6	$\overline{\text{DASL\_Y\_RX1}}$	A17
DASL_X_RX0	L17	DASL_Y_RX2	B17
$\overline{\text{DASL\_X\_RX0}}$	L19	$\overline{\text{DASL\_Y\_RX2}}$	A18
DASL_X_RX1	M17	DASL_Y_RX3	A19
$\overline{\text{DASL\_X\_RX1}}$	M19	$\overline{\text{DASL\_Y\_RX3}}$	B19
DASL_X_RX2	P17	DASL_Y_RX4	D17
$\overline{\text{DASL\_X\_RX2}}$	P19	$\overline{\text{DASL\_Y\_RX4}}$	D19
DASL_X_RX3	T19	DASL_Y_RX5	H19
$\overline{\text{DASL\_X\_RX3}}$	R18	$\overline{\text{DASL\_Y\_RX5}}$	H17
DASL_X_RX4	W19	DASL_Y_RX6	J19
$\overline{\text{DASL\_X\_RX4}}$	V19	$\overline{\text{DASL\_Y\_RX6}}$	J17
DASL_X_RX5	W18	DASL_Y_RX7	K19
$\overline{\text{DASL\_X\_RX5}}$	V17	$\overline{\text{DASL\_Y\_RX7}}$	K17
DASL_X_RX6	W17	DASL_Y_TX0	A8
$\overline{\text{DASL\_X\_RX6}}$	U17	$\overline{\text{DASL\_Y\_TX0}}$	C8
DASL_X_RX7	V15	DASL_Y_TX1	A9
$\overline{\text{DASL\_X\_RX7}}$	W16	$\overline{\text{DASL\_Y\_TX1}}$	B9
DASL_X_TX0	W15	DASL_Y_TX2	E10
$\overline{\text{DASL\_X\_TX0}}$	U15	$\overline{\text{DASL\_Y\_TX2}}$	G10
DASL_X_TX1	W13	DASL_Y_TX3	C10
$\overline{\text{DASL\_X\_TX1}}$	U13	$\overline{\text{DASL\_Y\_TX3}}$	A10
DASL_X_TX2	R13	DASL_Y_TX4	E11
$\overline{\text{DASL\_X\_TX2}}$	N12	$\overline{\text{DASL\_Y\_TX4}}$	G11

Table 10-1. Signal Pins Sorted by Signal Name (Page 2 of 4)

Signal Name	Grid Location	Signal Name	Grid Location
DASL_Y_TX5	B11	DBG_BusSELECT_1_9	L14
$\overline{\text{DASL\_Y\_TX5}}$	A11	DDV_1	P13
DASL_Y_TX6	C13	DDV_2	C16
$\overline{\text{DASL\_Y\_TX6}}$	A13	DI1	A5
DASL_Y_TX7	C15	DI2	A3
$\overline{\text{DASL\_Y\_TX7}}$	A15	DNG_1	K15
DBG_BusSELECT_0_0	E16	DNG_2	M9
DBG_BusSELECT_0_10	G14	EVEN_OQG	G8
DBG_BusSELECT_0_11	F19	FPAN_X	M3
DBG_BusSELECT_0_12	J16	FPAN_Y	N6
DBG_BusSELECT_0_13	G15	FROM_SMOOTH_PLL_OUT	R4
DBG_BusSELECT_0_14	J12	MEM_GNT_X_0	M1
DBG_BusSELECT_0_15	H15	MEM_GNT_X_1	M5
DBG_BusSELECT_0_1	C18	MEM_GNT_X_2	N4
DBG_BusSELECT_0_2	E18	MEM_GNT_X_3	L8
DBG_BusSELECT_0_3	F17	MEM_GNT_Y_0	J6
DBG_BusSELECT_0_4	G16	MEM_GNT_Y_1	E4
DBG_BusSELECT_0_5	J14	MEM_GNT_Y_2	C2
DBG_BusSELECT_0_6	F15	MEM_GNT_Y_3	D3
DBG_BusSELECT_0_7	G18	MP_ADD_PRTY	N7
DBG_BusSELECT_0_8	D15	MP_ADDR_0	E2
DBG_BusSELECT_0_9	H13	MP_ADDR_1	J8
DBG_BusSELECT_1_0	M15	MP_ADDR_2	G2
DBG_BusSELECT_1_10	N15	MP_ADDR_3	H5
DBG_BusSELECT_1_11	P15	MP_ADDR_4	K5
DBG_BusSELECT_1_12	R16	MP_ADDR_5	K7
DBG_BusSELECT_1_13	U18	MP_ADDR_6	L3
DBG_BusSELECT_1_14	T17	MP_ADDR_7	R2
DBG_BusSELECT_1_15	U16	MP_BURST_MODE	M7
DBG_BusSELECT_1_1	L12	MP_CLK	U1
DBG_BusSELECT_1_2	K13	MP_DATA_0	H7
DBG_BusSELECT_1_3	R14	MP_DATA_1	F5
DBG_BusSELECT_1_4	N18	MP_DATA_2	F1
DBG_BusSELECT_1_5	N14	MP_DATA_3	H1
DBG_BusSELECT_1_6	M13	MP_DATA_4	G5
DBG_BusSELECT_1_7	L16	MP_DATA_5	K3
DBG_BusSELECT_1_8	N16	MP_DATA_6	L2

Table 10-1. Signal Pins Sorted by Signal Name (Page 3 of 4)

Signal Name	Grid Location	Signal Name	Grid Location
MP_DATA_7	L1	RXDATA_28	P9
MP_DATA_PRTY	G4	RXDATA_29	W4
$\overline{\text{MP\_INT}}$	L4	RXDATA_2	T13
MP_PRDY	H3	RXDATA_30	N8
MP_PRTY_ENB	N2	RXDATA_31	P7
$\overline{\text{MP\_SEL}}$	N1	RXDATA_3	U7
$\overline{\text{MP\_WR}}$	N3	RXDATA_4	W14
ODD_OQG	E7	RXDATA_5	P11
PE_CLK	G1	RXDATA_6	N13
PE_PLLLOCK	E1	RXDATA_7	W12
PE_RXCLK_out	E3	RXDATA_8	R9
PE_TESTIN	C3	RXDATA_9	N9
PE_TESTOUT	C1	$\overline{\text{RXENB}}$	T5
PE_TXCLK_out	R5	RXPAV	U4
PE_VDDA	K1	RXPRTY	V3
$\overline{\text{POR}}$	T1	RXSOP	W2
RI	C5	SEND_GNT_X	N5
RXDATA_0	T15	SEND_GNT_Y	U2
RXDATA_10	U11	Shadow_RXclock_In	F3
RXDATA_11	V13	Shadow_RXclock_Out	D1
RXDATA_12	T11	SHARED_GNT	C11
RXDATA_13	M11	Slot_IDN_0	G7
RXDATA_14	U3	Slot_IDN_1	J2
RXDATA_15	W3	Slot_IDN_2	J1
RXDATA_16	R8	Slot_IDN_3	J3
RXDATA_17	V9	Slot_IDN_4	J4
RXDATA_18	W9	START_GCXFR	D7
RXDATA_19	U9	SWITCH_X_CLK	N17
RXDATA_1	U14	$\overline{\text{SWITCH\_X\_CLK}}$	N19
RXDATA_20	V7	$\overline{\text{SWITCH\_X\_INSERVICE}}$	T3
RXDATA_21	T7	SWITCH_X_PLLLOCK	R19
RXDATA_22	U8	$\overline{\text{SWITCH\_X\_PRESENT}}$	B1
RXDATA_23	W8	SWITCH_X_TESTIN	R17
RXDATA_24	T9	SWITCH_X_TESTOUT	U19
RXDATA_25	W6	SWITCH_X_VDDA	L18
RXDATA_26	R6	SWITCH_Y_CLK	G19
RXDATA_27	R7	$\overline{\text{SWITCH\_Y\_CLK}}$	G17

Table 10-1. Signal Pins Sorted by Signal Name (Page 4 of 4)

Signal Name	Grid Location	Signal Name	Grid Location
$\overline{\text{SWITCH\_Y\_INSERVICE}}$	V1	TXDATA_1	C7
SWITCH_Y_PLLLOCK	E19	TXDATA_20	G12
$\overline{\text{SWITCH\_Y\_PRESENT}}$	P5	TXDATA_21	E14
SWITCH_Y_TESTIN	C19	TXDATA_22	F13
SWITCH_Y_TESTOUT	E17	TXDATA_23	H11
SWITCH_Y_VDDA	J18	TXDATA_24	D11
TCK	L5	TXDATA_25	B13
TDI	J7	TXDATA_26	G13
TDO	L6	TXDATA_27	A12
TEST_B2	R1	TXDATA_28	F11
TEST_C3	R3	TXDATA_29	A14
TEST_CLK	L13	TXDATA_2	A2
TMS	G3	TXDATA_30	D13
TO_SMOOTH_PLL_IN	P3	TXDATA_31	C14
TRST	L7	TXDATA_3	B3
TXDATA_0	E5	TXDATA_4	C4
TXDATA_10	B5	TXDATA_5	D5
TXDATA_11	C6	TXDATA_6	G9
TXDATA_12	E6	TXDATA_7	E9
TXDATA_13	A6	TXDATA_8	F7
TXDATA_14	D9	TXDATA_9	A4
TXDATA_15	H9	$\overline{\text{TXENB}}$	E12
TXDATA_16	A7	$\overline{\text{TXFULL}}$	E8
TXDATA_17	B7	TXPRTY	F9
TXDATA_18	C9	TXSOP	C12
TXDATA_19	E13		

Table 10-2. Signal Pins Sorted by Grid Location (Page 1 of 4)

Grid Location	Signal Name	Grid Location	Signal Name
A2	TXDATA_2	C9	TXDATA_18
A3	DI2	C10	DASL_Y_TX3
A4	TXDATA_9	C11	SHARED_GNT
A5	DI1	C12	TXSOP
A6	TXDATA_13	C13	DASL_Y_TX6
A7	TXDATA_16	C14	TXDATA_31
A8	DASL_Y_TX0	C15	DASL_Y_TX7
A9	DASL_Y_TX1	C16	DDV_2
A10	$\overline{\text{DASL\_Y\_TX3}}$	C17	DASL_Y_RX1
A11	$\overline{\text{DASL\_Y\_TX5}}$	C18	DBG_BusSELECT_0_1
A12	TXDATA_27	C19	SWITCH_Y_TESTIN
A13	$\overline{\text{DASL\_Y\_TX6}}$	D1	Shadow_RXclock_Out
A14	TXDATA_29	D3	MEM_GNT_Y_3
A15	$\overline{\text{DASL\_Y\_TX7}}$	D5	TXDATA_5
A16	DASL_Y_RX0	D7	START_GCXFR
A17	$\overline{\text{DASL\_Y\_RX1}}$	D9	TXDATA_14
A18	$\overline{\text{DASL\_Y\_RX2}}$	D11	TXDATA_24
A19	DASL_Y_RX3	D13	TXDATA_30
B1	$\overline{\text{SWITCH\_X\_PRESENT}}$	D15	DBG_BusSELECT_0_8
B3	TXDATA_3	D17	DASL_Y_RX4
B5	TXDATA_10	D19	$\overline{\text{DASL\_Y\_RX4}}$
B7	TXDATA_17	E1	PE_PLLLOCK
B9	$\overline{\text{DASL\_Y\_TX1}}$	E2	MP_ADDR_0
B11	DASL_Y_TX5	E3	PE_RXCLK_out
B13	TXDATA_25	E4	MEM_GNT_Y_1
B15	$\overline{\text{DASL\_Y\_RX0}}$	E5	TXDATA_0
B17	DASL_Y_RX2	E6	TXDATA_12
B19	$\overline{\text{DASL\_Y\_RX3}}$	E7	ODD_OQG
C1	PE_TESTOUT	E8	$\overline{\text{TXFULL}}$
C2	MEM_GNT_Y_2	E9	TXDATA_7
C3	PE_TESTIN	E10	DASL_Y_TX2
C4	TXDATA_4	E11	DASL_Y_TX4
C5	RI	E12	$\overline{\text{TXENB}}$
C6	TXDATA_11	E13	TXDATA_19
C7	TXDATA_1	E14	TXDATA_21
C8	$\overline{\text{DASL\_Y\_TX0}}$	E15	ABIST_CLK

Table 10-2. Signal Pins Sorted by Grid Location (Page 2 of 4)

Grid Location	Signal Name	Grid Location	Signal Name
E16	DBG_BusSELECT_0_0	H9	TXDATA_15
E17	SWITCH_Y_TESTOUT	H11	TXDATA_23
E18	DBG_BusSELECT_0_2	H13	DBG_BusSELECT_0_9
E19	SWITCH_Y_PLLLOCK	H15	DBG_BusSELECT_0_15
F1	MP_DATA_2	H17	$\overline{\text{DASL\_Y\_RX5}}$
F3	Shadow_RXclock_In	H19	DASL_Y_RX5
F5	MP_DATA_1	J1	Slot_IDN_2
F7	TXDATA_8	J2	Slot_IDN_1
F9	TXPRTY	J3	Slot_IDN_3
F11	TXDATA_28	J4	Slot_IDN_4
F13	TXDATA_22	J5	ABIST_DIAGOUT
F15	DBG_BusSELECT_0_6	J6	MEM_GNT_Y_0
F17	DBG_BusSELECT_0_3	J7	TDI
F19	DBG_BusSELECT_0_11	J8	MP_ADDR_1
G1	PE_CLK	J12	DBG_BusSELECT_0_14
G2	MP_ADDR_2	J13	CE1_A
G3	TMS	J14	DBG_BusSELECT_0_5
G4	MP_DATA_PRTY	J15	CE1_C2
G5	MP_DATA_4	J16	DBG_BusSELECT_0_12
G6	$\overline{\text{DASL\_DRV\_ENB}}$	J17	$\overline{\text{DASL\_Y\_RX6}}$
G7	Slot_IDN_0	J18	SWITCH_Y_VDDA
G8	EVEN_OQG	J19	DASL_Y_RX6
G9	TXDATA_6	K1	PE_VDDA
G10	$\overline{\text{DASL\_Y\_TX2}}$	K3	MP_DATA_5
G11	$\overline{\text{DASL\_Y\_TX4}}$	K5	MP_ADDR_4
G12	TXDATA_20	K7	MP_ADDR_5
G13	TXDATA_26	K13	DBG_BusSELECT_1_2
G14	DBG_BusSELECT_0_10	K15	DNG_1
G15	DBG_BusSELECT_0_13	K17	$\overline{\text{DASL\_Y\_RX7}}$
G16	DBG_BusSELECT_0_4	K19	DASL_Y_RX7
G17	$\overline{\text{SWITCH\_Y\_CLK}}$	L1	MP_DATA_7
G18	DBG_BusSELECT_0_7	L2	MP_DATA_6
G19	SWITCH_Y_CLK	L3	MP_ADDR_6
H1	MP_DATA_3	L4	$\overline{\text{MP\_INT}}$
H3	MP_PRDY	L5	TCK
H5	MP_ADDR_3	L6	TDO
H7	MP_DATA_0	L7	TRST

Table 10-2. Signal Pins Sorted by Grid Location (Page 3 of 4)

Grid Location	Signal Name	Grid Location	Signal Name
L8	MEM_GNT_X_3	N19	$\overline{\text{SWITCH\_X\_CLK}}$
L12	DBG_BusSELECT_1_1	P1	APAN_X
L13	TEST_CLK	P3	TO_SMOOTH_PLL_IN
L14	DBG_BusSELECT_1_9	P5	$\overline{\text{SWITCH\_Y\_PRESENT}}$
L15	CE1_C1	P7	RXDATA_31
L16	DBG_BusSELECT_1_7	P9	RXDATA_28
L17	DASL_X_RX0	P11	RXDATA_5
L18	SWITCH_X_VDDA	P13	DDV_1
L19	$\overline{\text{DASL\_X\_RX0}}$	P15	DBG_BusSELECT_1_11
M1	MEM_GNT_X_0	P17	DASL_X_RX2
M3	FPAN_X	P19	$\overline{\text{DASL\_X\_RX2}}$
M5	MEM_GNT_X_1	R1	TEST_B2
M7	MP_BURST_MODE	R2	MP_ADDR_7
M9	DNG_2	R3	TEST_C3
M11	RXDATA_13	R4	FROM_SMOOTH_PLL_OUT
M13	DBG_BusSELECT_1_6	R5	PE_TXCLK_out
M15	DBG_BusSELECT_1_0	R6	RXDATA_26
M17	DASL_X_RX1	R7	RXDATA_27
M19	$\overline{\text{DASL\_X\_RX1}}$	R8	RXDATA_16
N1	$\overline{\text{MP\_SEL}}$	R9	RXDATA_8
N2	MP_PRTY_ENB	R10	DASL_X_TX7
N3	$\overline{\text{MP\_WR}}$	R11	$\overline{\text{DASL\_X\_TX5}}$
N4	MEM_GNT_X_2	R12	$\overline{\text{DASL\_X\_TX3}}$
N5	SEND_GNT_X	R13	DASL_X_TX2
N6	FPAN_Y	R14	DBG_BusSELECT_1_3
N7	MP_ADD_PRTY	R15	CE1_B
N8	RXDATA_30	R16	DBG_BusSELECT_1_12
N9	RXDATA_9	R17	SWITCH_X_TESTIN
N10	$\overline{\text{DASL\_X\_TX7}}$	R18	$\overline{\text{DASL\_X\_RX3}}$
N11	DASL_X_TX5	R19	SWITCH_X_PLLLOCK
N12	$\overline{\text{DASL\_X\_TX2}}$	T1	$\overline{\text{POR}}$
N13	RXDATA_6	T3	$\overline{\text{SWITCH\_X\_INSERVICE}}$
N14	DBG_BusSELECT_1_5	T5	$\overline{\text{RXENB}}$
N15	DBG_BusSELECT_1_10	T7	RXDATA_21
N16	DBG_BusSELECT_1_8	T9	RXDATA_24
N17	SWITCH_X_CLK	T11	RXDATA_12
N18	DBG_BusSELECT_1_4	T13	RXDATA_2

Table 10-2. Signal Pins Sorted by Grid Location (Page 4 of 4)

Grid Location	Signal Name	Grid Location	Signal Name
T15	RXDATA_0	V9	RXDATA_17
T17	DBG_BusSELECT_1_14	V11	$\overline{\text{DASL\_X\_TX4}}$
T19	DASL_X_RX3	V13	RXDATA_11
U1	MP_CLK	V15	DASL_X_RX7
U2	SEND_GNT_Y	V17	$\overline{\text{DASL\_X\_RX5}}$
U3	RXDATA_14	V19	$\overline{\text{DASL\_X\_RX4}}$
U4	RXPAV	W1	APAN_Y
U5	CE0_TEST	W2	RXSOP
U6	AC_TEST_in	W3	RXDATA_15
U7	RXDATA_3	W4	RXDATA_29
U8	RXDATA_22	W5	CE0_IO
U9	RXDATA_19	W6	RXDATA_25
U10	$\overline{\text{DASL\_X\_TX6}}$	W7	CE0_Scan
U11	RXDATA_10	W8	RXDATA_23
U12	DASL_X_TX3	W9	RXDATA_18
U13	$\overline{\text{DASL\_X\_TX1}}$	W10	DASL_X_TX6
U14	RXDATA_1	W11	DASL_X_TX4
U15	$\overline{\text{DASL\_X\_TX0}}$	W12	RXDATA_7
U16	DBG_BusSELECT_1_15	W13	DASL_X_TX1
U17	$\overline{\text{DASL\_X\_RX6}}$	W14	RXDATA_4
U18	DBG_BusSELECT_1_13	W15	DASL_X_TX0
U19	SWITCH_X_TESTOUT	W16	$\overline{\text{DASL\_X\_RX7}}$
V1	$\overline{\text{SWITCH\_Y\_INSERVICE}}$	W17	DASL_X_RX6
V3	RXPRTY	W18	DASL_X_RX5
V5	AC_TEST_out	W19	DASL_X_RX4
V7	RXDATA_20		

10.1 Power Signals

Table 10-3. Ground Signal Pin Locations

Sequence Number	Grid Location	Sequence Number	Grid Location	Sequence Number	Grid Location
1	B2	16	H8	31	M16
2	B6	17	H12	32	P2
3	B10	18	H16	33	P6
4	B14	19	J10	34	P10
5	B18	20	K2	35	P14
6	D4	21	K6	36	P18
7	D8	22	K9	37	T4
8	D12	23	K10	38	T8
9	D16	24	K11	39	T12
10	F2	25	K14	40	T16
11	F6	26	K18	41	V2
12	F10	27	L10	42	V6
13	F14	28	M4	43	V10
14	F18	29	M8	44	V14
15	H4	30	M12	45	V18

Table 10-4. V_{DD1} (2.5 V) Signal Pin Locations

Sequence Number	Grid Location	Sequence Number	Grid Location	Sequence Number	Grid Location
1	B4	9	J9	17	M6
2	B12	10	J11	18	M10
3	D10	11	K4	19	M18
4	D18	12	K8	20	P12
5	F8	13	K12	21	T2
6	H2	14	K16	22	T10
7	H10	15	L9	23	V8
8	H14	16	L11	24	V16

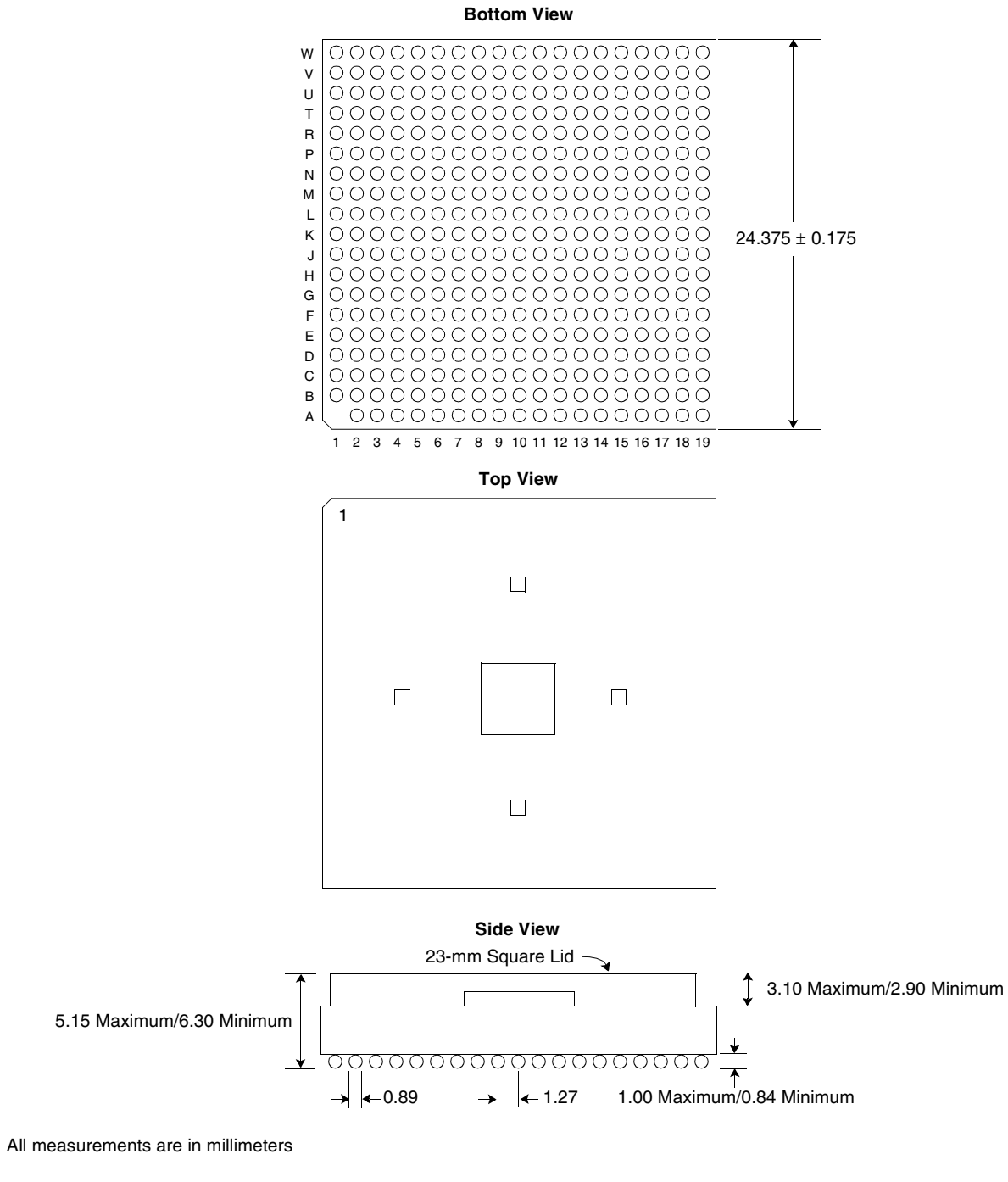
Table 10-5. V_{DD2} - V_{DD5} (1.5 V and 3.3 V) Signal Pin Locations

Pin Name	Supply	Location	Sequence Number	Grid Location
V_{DD2}	1.5 V	South	1	F16
			2	H18
			3	M14
			4	P16
			5	T18
V_{DD3}	1.5 V	East	1	P8
			2	T6
			3	T14
			4	V4
			5	V12
V_{DD4}	3.3 V	North	1	D2
			2	F4
			3	H6
			4	M2
			5	P4
V_{DD5}	1.5 V	West	1	B8
			2	B16
			3	D6
			4	D14
			5	F12

11. Packaging Information

CBGA-360 with standard aluminum lid and grease.

Figure 11-1. 25 x 25 mm 360-Lead Ceramic Ball Grid Array (CBGA)



12. Glossary

ABIST	array built-in self test
AC	alternating current
APA	adapter port available
ASIC	application-specific integrated circuit
ATM	asynchronous transfer mode
BIST	built-in self test
BM	Bit map addressing. If there is a ‘1’ in this field, then data within the same packet is for the corresponding output port of the switch.
CBGA	ceramic ball grid array
CC	clock cycle
CCR	Common_Control register
cell	A small portion of fixed-length data transported as an entity and not partitioned further. A converter cell is 64 to 80 bytes long, in steps of four bytes. Used interchangeably with packet.
CIO	common input/output
CMOS	complementary metal-oxide semiconductor
control	A control packet communicates with the switch control. The bit map of such a packet is set to all zeros. Upon detecting such a value, the switch automatically routes the packet to the switch control. In response, the switch control can also insert a control packet in the output queues of the switch.
converter	The IBM Packet Routing Switch Serial Interface Converter. The device performing a UTOPIA-3-like parallel interface to switch the DASL interface conversion.
CRC	Cyclic Redundancy Check. A code used to validate a block of data. A CRC8 is used in the IBM Packet Routing Switch Serial Interface Converter
DASL	Data-Aligned Synchronous Link. A high-speed, point-to-point, interdevice, communication interface. Performs multibit serialization to reduce the input/output pin count. Uses reduced voltage differential transceivers to reduce power consumption.
DC	direct current
DLL	digitally locked loop
EDI	Egress DASL Interface. The logical and physical interface between the converter egress FIFO and the DASL macro.
egress	Away from the switch core, corresponds to the data transmitted by the switch.

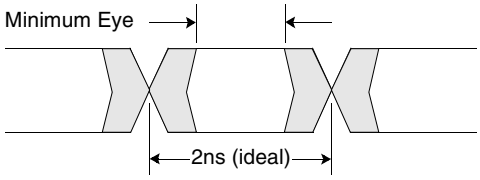
EIA	Electronics Industries Association
FCS	frame check sequence
FFDC	first failure data capture
FIFO	First-in/first-out. A read-write memory used as a buffer to smooth out the converter data flow. The output bits are in the same sequence as the input bits.
FPA	fabric port available
frame	A stream of packaged data that is a multiple of packet length divided by four (equal to LU length). For example, if there are only two priorities in use in the back-pressure link, then the frame length of the framing signal will be equivalent to two logical units of the switch or to two data packets where the length of the data packet is expressed in words (4 bytes or 32 bits).
GRA	growable RAM array
HSTL	High-speed transceiver logic. The electrical level supported by the converter lines.
I/O	input and/or output
IBFC	In-band flow control. Corresponds to the case where the switch flow control information (output queue grant and memory grant in the egress direction and send grant in the ingress direction) are carried within any contiguous packets (idle or data) flowing between the protocol engine and the converter.
IBLC	in-band link-level flow control
IDI	Ingress DASL Interface. The logical and physical interface between the converter ingress FIFO and the DASL macro.
idle packet	Idle packets are used as time-fill packets to maintain the integrity of the bus when there is no data.
IEEE	Institute of Electrical and Electronics Engineers
ingress	Towards the switch core, corresponds to the data received by the switch.
IOB	input/output block
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Action Test Group
LBIST	logic built-in self test
LOS	loss of signal
LPDL	least positive down level
LSB	least significant bit (or byte)
LSSD	level-sensitive scan design

LU Logical unit. Defines the length of an 8-bit row of data processed by a single shared memory within the switch. The converter handles LUs of 16 to 20 bytes corresponding to packet sizes of 64 to 80 bytes.

LVTTL low-voltage transistor-transistor logic

M3 See SDC.

minimum eye As part of the DASL receiver error detection function, used to detect bit synchronization errors due to excessive transient noise (that is, ESD). This class of error is characterized by eye closures, which are detected by the edge sampling circuit. An error condition exists when an edge is detected within the minimum eye region of the data sample.



MP microprocessor

MPUL most positive up level

MSB most significant bit (or byte)

OBFC Out-of-band flow control. Corresponds to the case where the switch flow control information (output queue grant and memory grant in the egress direction and send grant in the ingress direction) is carried through $\overline{\text{RXENB}}$ or $\overline{\text{TXFULL}}$.

OBLC out-of-band link-level flow control

OQG output queue grant

packet Used interchangeably with cell.

PC packet cycle

PE Protocol Engine (protocol processor, ATM layer, etc.). The device that attaches on the line side of the converter and runs the higher layer protocols.

PHY physical layer

PLL phase-locked loop

POR power-on reset

PQ Packet qualifier. A byte of information used by the switch to interpret packet priority, packet idle or data, or packet color.

RAM random access memory

reserved Reserved for future use.

RI receiver Inhibit

RR	receive ready
RX	receive
SDC/M3	Shared DASL Controller (also called the M3 picoprocessor). The processor that controls the DASL transceiver for the delay line management for temperature tracking, clock drift, and so forth.
SDCIRI	SDC Internal Resource Interface
service	A service packet is any idle packet (resulting from a flow control situation or an empty link) or any physical layer interface packet that checks the continuity of a link packet (yellow packet).
SM	shared memory
SMG	shared memory grant
SOP	start of packet
SRAM	static random access memory
SRL	set/reset latch
switch	IBM Packet Routing Switch PRS28.4G. The switch element that enables high-performance, nonblocking, fixed-length packet switching.
synch packet	Synchronization packets are service packets used to train the DASL receiver to acquire bit/byte/packet synchronization.
TAP	test access port
TDI	test data input
TDO	test data output
TX	transmit
UTOPIA	Universal Test and Operations PHY Interface for ATM
VCO	voltage-controlled oscillator
VOQ	virtual output queuing
yellow packet	A service packet used to check the continuity of the physical link between the switch and the converter.

13. Revision Log

Revision	Description of Modification
10/15/99	Initial release (00)
07/12/00	First revision (01). Added Grant Control Generation to Figure 2-1. Added numbering to headings and tables. Added Table of Contents.
03/01/01	Second revision (02). Changed product number from IBM3209K3114 to IBM3229P2035.
04/23/01	Third revision (03). Incorporated new sections on Converter Flow Control and Switch Flow Control (Section 2.3 and Section 2.4, respectively). Incorporated the following content changes: • Removed flow control paragraphs from Section 1.2, Description. • Defined “big endian architecture” in Section 1.4, Conventions and Notation. • Edited multiple references to OBFC/IBFC and OBLC/IBLC terminology in Section 2 and Section 3. • Inserted a sentence to introduce and reference Figure 2-4. • Modified the notes and key definitions in Figure 2-4. • Moved grant control paragraph from Section 2.4.1 to Section 3.7. • Edited the ninth bullet in Section 3.2, Functional Overview. • Added one sentence to end of RXENB function description in Table 3-1. • Modified caption and content of Figure 3-3. • Replaced Figure 3-4. • Modified Figures 3-5 and 3-6 to remove “Converter cannot accept new packet.” • Modified text of section 3.2.3. • Moved Figure 3-9 from Section 3.2.2.2 to follow introductory paragraph in Section 3.2.3. • Changed Figure 3-9 caption and Section 3.2.3 heading from “TXFULL Timing” to “TXFULL Timing Restriction.” • Added Section 3.2.4, Timing for TXFULL Deasserted. • Added new bullet to the ingress LU formatter functional description in Section 3.3.1. • Added two examples to the TxPause discussion in Section 3.3.2. • Replaced data packet bit meaning values in Table 3-4, Table 3-6, and Table 3-7. • Changed from “UTOPIA-3 Notation” to “IBM Notation” in Figure 3-10. • Reformatted two tables in Section 3.5 to emphasize path selection results. Added a note to the second table. • Added a note to the end of Section 3.6.1.2, Packet Formats. • Edited the note regarding yellow packets that follows the 32 × 32 switch interface idle packet format table. • Edited bullets in Section 3.6.2.1, EDI Functions. • Moved back-pressure serial link discussion from Section 3.7 to Section 2.3.1.1. • Added a note to the table in Section 3.10.1, Reset Strategy. • Modified the last paragraph of Section 3.10.2. • Added two new processor interface I/O line descriptions to the table in Section 3.11.2. • Changed signal name from MP_WR to MP_RNW in table in Section 3.11.2. • Changed MP_ADD_PRTY from [7:2] to [7:0] and removed tri-state condition for MP_PRDY in Figure 3-23 and Figure 3-24. • Modified note following Figure 3-24. • Modified Figure 4-1, Individual Register Mapping. • Inserted a sentence to introduce and reference Figure 4-2. • Edited the fifth bullet and the second enumerated item presented in Section 4.1, Error Detection, Reporting, and Interrupt Registers. • Reformatted register names consistently in Table 4-1, Register Map. • Modified specific content in the register tables in Sections 4.2.1, 4.2.3, 4.2.4, 4.2.5, 4.2.6, 4.2.8, 4.2.10, 4.2.11, 4.2.12, 4.2.13, 4.2.15, 4.2.16, 4.2.20, 4.2.21, 4.2.27, 4.2.28, 4.2.29, 4.2.31, 4.2.32, 4.2.33, 4.2.34, 4.2.35, 4.2.37, 4.2.38, 4.2.39, and 4.2.40. • Edited the paragraph following “Read and Write Operations” in Section 4.2.15. • Added “SDC_Debug_CNTL Register Purpose” and “M3 Keep Alive Feature” subsections to Section 4.2.16. • Modified Figure 4-3 and Figure 4-5 and explanatory notes. • Inserted sentences to introduce and reference Figure 4-4 and Figure 4-6. • Deleted the Latency section (Section 5 in Rev. 01). Latency is discussed in Sections 2.3 and 2.4. • Removed Appendix A and B labels from section headings and moved DASL and PLL sections forward to Section 5 and Section 6, respectively. • Inserted a sentence to introduce and reference Figure 5-1 and Table 5-1; modified Figure 5-1. • Defined the Debug Control Input fields in Section 5.5. • Created Section 5.6 heading. • Modified the SDC Status register table in Section 5.6. • Replaced Figure 5-3 and added Figure 5-4.

Revision	Description of Modification
04/23/01	• Deleted the DASL Synchronization Signals table (Table 48 in Rev. 01). • Inserted a paragraph to introduce and reference Table 6-2. • Edited the IDcode register text and modified the register table that follows Table 7-2. • Corrected the corresponding notes for the CE0_IO, CE0_Scan,and CE0_TEST signals in Table 8-1. • Modified description of TRST in Table 8-2. • Removed overbars from MP_PRDY and MP_PRTY_ENB signals in Table 8-3. • Added one sentence to the end of the descriptions of TO_SMOOTH_PLL_IN, Shadow_RXclock_Out, and PR_VDDA signals in Table 8-7. • Modified Figure 8-2 to show resistor. • Modified specific bit definitions in Table 8-12, DBG_SELECT Bus Definition. • Replaced “AC Specifications” with “AC Ratings” in Section 8.2.2 and Section 8.2.4 headings. • Modified Figure 8-4, Options for Ingress UTOPIA-3-Like Interface Clocking. • Edited third paragraph under Section 9.1, Power Sequencing. • Modified entries in Table 9-2 and Table 9-3. • Replaced DASL Driver signal rating values in Table 9-4. • Combined multiple V_{DD} signal pin location tables into one table (Table 10-5).\ • Added “minimum eye” definition to Glossary. Made minor text changes to improve consistency and readability throughout document. Inserted pinout diagram (Figure 10-1). Reformatted tables for consistent column headings and column widths. Defined acronyms at first occurrence. Changed the definition of DASL from “data-aligned serial link” to “data-aligned synchronous link.” Reformatted and updated Glossary (Section 12). Changed references to the “IBM 28.4G Packet Routing Switch” to the “IBM Packet Routing Switch PRS28.4G” or the shortened version “PRS28.4G” (Wired Products Naming Convention, August 2000). Added List of Figures and List of Tables. Added Intel trademark language to legal page.