Integrated Device Technology, Inc.

512K x 8 CMOS STATIC RAM MODULE

IDT7MP4008S

FEATURES:

- High-density 4 megabit CMOS static RAM module
- Fast access times
  - — 30ns (max.)
- Cost effective plastic surface mount RAM packages on a epoxy laminate (FR-4) substrate
- Available in 36-pin SIP (Single In-line Package)
- Low power consumption
  - — Dynamic: 2.6W (max.)
  - — Full standby: 1.9W (max.)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT7MP4008 is a 512K x 8 high-speed CMOS static RAM module constructed on an epoxy laminate surface using sixteen 32K x 8 static RAMs in plastic surface mount packages. Extremely fast speeds can be achieved with this technique due to the use of 256K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS™ technology.

The IDT7MP family of surface-mounted SIP modules is a cost-effective solution allowing for very high packing density and the IDT7MP4008 is offered in a 36-pin SIP. The IDT7MP4008 can be stacked on 300 mil centers, yielding greater than 12 megabits of RAM in less than 5 square inches of board space.

The IDT7MP4008 is available with minimum access times as fast as 30ns over the commercial temperature range with maximum power consumption of 2.6 watts. The IDT7MP4008 also offers a full standby mode of 1.9W (max.).

All inputs and outputs of the IDT7MP4008 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

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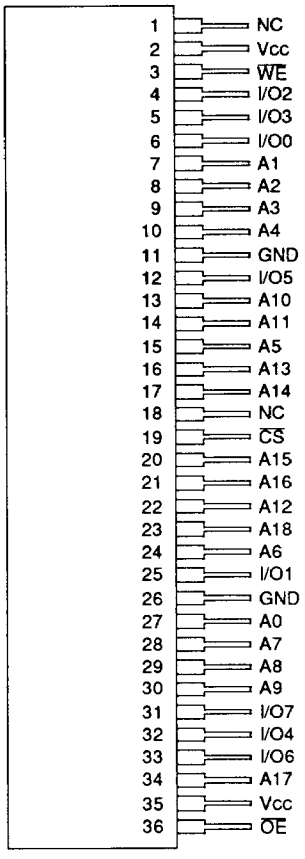
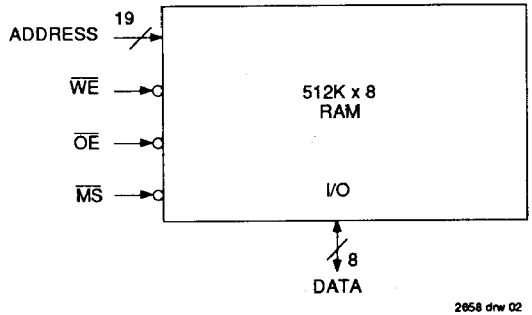
PIN CONFIGURATION[1]



SIP
BACK VIEW

2658 drw 01

FUNCTIONAL BLOCK DIAGRAM



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PIN NAMES

A_{0-18}	Addresses
I/O_{0-7}	Data Inputs/Outputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
Vcc	Power
GND	Ground

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NOTE:
1. For module dimensions, please refer to module drawing M37 in the packaging section.

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

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NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

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NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

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DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MP4008S Min.	IDT7MP4008S Max.(2)	IDT7MP4008S Max.(3)	Unit
$\|I_{LI}\|$	Input Leakage Current(1)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	80	80	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	80	80	µA
I_{CC}	Dynamic Operating Current	$\overline{CS}$ = V_{IL} V_{CC} = Max. Output Open f = f_{MAX}	—	550	500	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or (TTL Level) V_{CC} = Max., f = f_{MAX} Outputs Open	—	480	350	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ V_{HC}, V_{IN} ≥ V_{HC} or ≤ V_{LC} V_{CS} = Max., Output Open	—	285	285	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA, V_{CC} = Min.	2.4	—	—	V

2658 tbl 05

NOTES:
1. $|I_{LI}|$ for A_{15}–A_{16} and $\overline{CS}$ = 400 µA (max.).
2. t_{AA} = 30ns.
3. t_{AA} = 35, 45, 55, 70ns.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2658 tbl 06

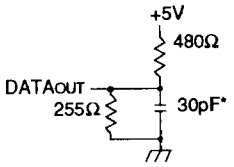

Figure 1. Output Load

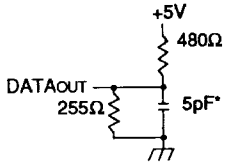

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Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP4008S30		7MP408S35		7MP4008S45		7MP4008S55		7MP4008S70		Unit
		Min.	Max.	Min.	Max	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	30	—	35	—	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	30	—	35	—	45	—	55	—	70	ns
t_{ACS}	Chip Select Access Time	—	30	—	35	—	45	—	55	—	70	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enables to Output Valid	—	13	—	15	—	20	—	25	—	30	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	0	—	0	—	0	—	ns
t_{CHZ}[1]	Chip Select to Output in High Z	—	20	—	21	—	25	—	30	—	35	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	11	—	13	—	25	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
Write Cycle												
t_{WC}	Write Cycle Time	30	—	35	—	45	—	55	—	70	—	ns
t_{CW}	Chip Select to End of Write	25	—	30	—	40	—	50	—	60	—	ns
t_{AW}	Address Valid to End of Write	25	—	30	—	40	—	50	—	60	—	ns
t_{AS}	Address Set-up Time	5	—	5	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	35	—	45	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	5	—	5	—	10	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	13	—	14	—	15	—	20	—	25	ns
t_{DW}	Data Valid to End of Write	14	—	16	—	20	—	25	—	30	—	ns
t_{DH}	Data Hold from Write Time	3	—	3	—	5	—	5	—	5	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

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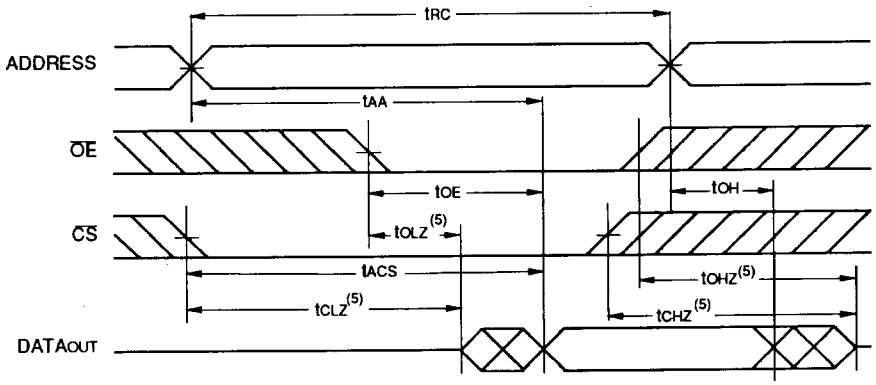
NOTE:
1. This parameter is guaranteed by design but not tested.

8

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



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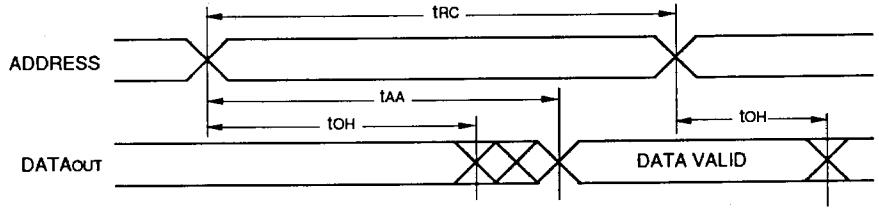
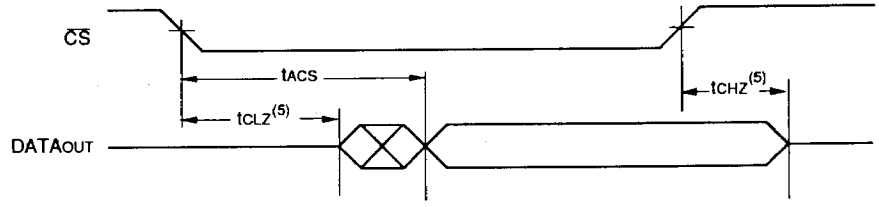
TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2658 drw 05

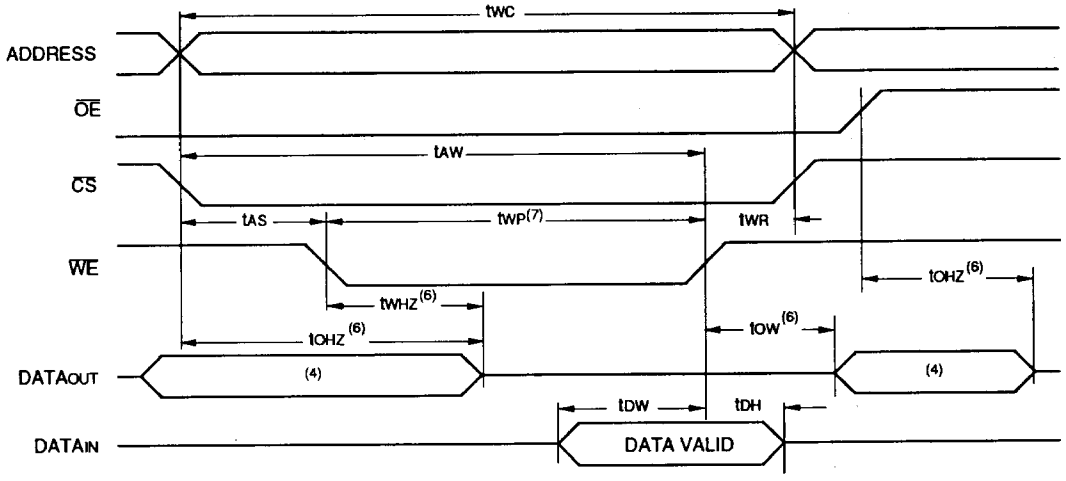
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2658 drw 06

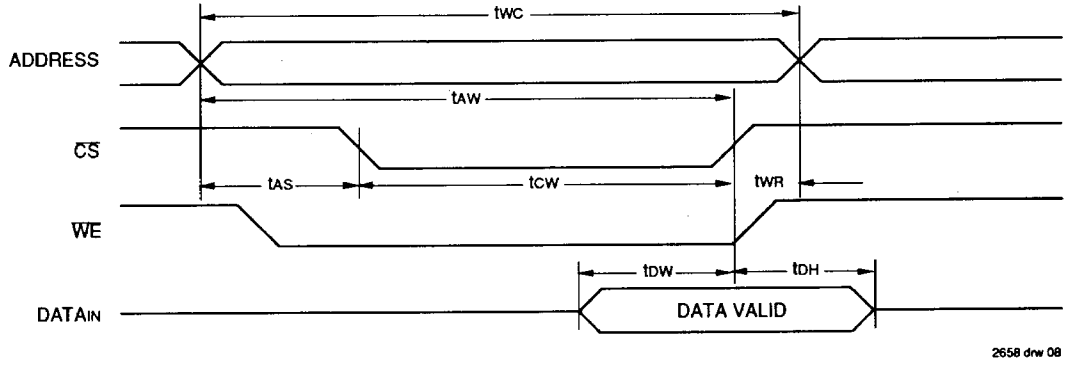
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



2658 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



2658 drw 08

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured by ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (tWP > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

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TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DATAOUT	Active
Read	L	H	H	High Z	Active
Write	L	X	L	DATAIN	Active

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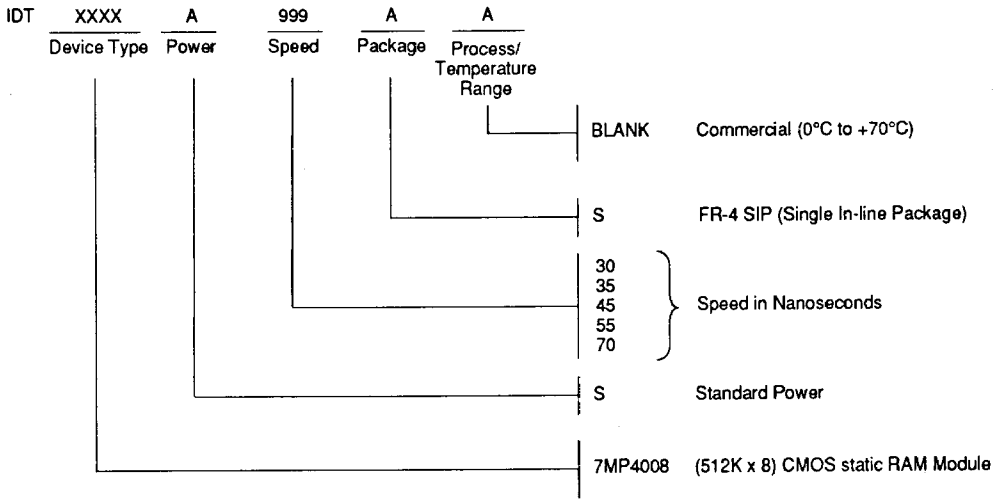
CAPACITANCE[1] (T_A = +25°C, f =1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	188	pF
$C_{IN(A)}$	Input Capacitance (Address and Control)	V_{IN} = 0V	188	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	128	pF

2658 tbl 09

NOTE:
1. This parameter is guaranteed by design but not tested.

ORDERING INFORMATION



2658 drw 09