HB66B1616A Series

16,384-Word × 16-Bit High Speed Static RAM Module

■ DESCRIPTION

The HB66B1616A is a high speed 16K × 16 Static RAM module, mounted 4 pieces of 64K bit SRAM (HM6289JP) sealed in SOJ package. An outline of the HB66B1616A is 36-pin dual in-line package. Therefore, the HB66B1616A makes high density mounting possible without surface mount technology. The HB66B1616A provides common data inputs and outputs. Its module board has decoupling capacitors to reduce noise.

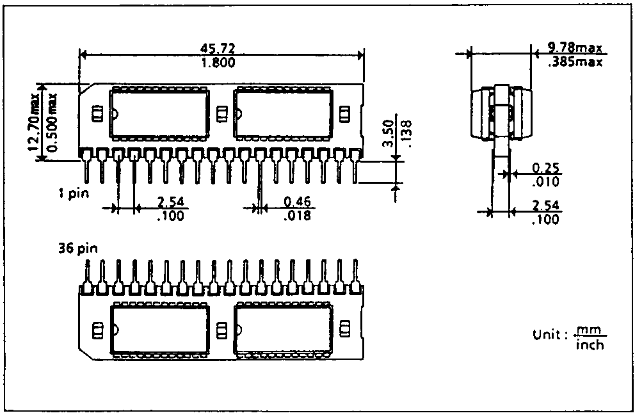
■ FEATURES

- Single 5V (± 5%) Supply
- High Speed
  - Access Time . . . . .25/35ns (max.)
- Low Power Dissipation
  - Active Mode. . . . . .1200mW typ.
  - Standby Mode. . . . . .300mW typ. (TTL level)
    0.4mW typ. (CMOS level)
- Equal Access and Cycle Time
- Completely Static RAM
  - No Clock or Timing Strobe Required
- Directly TTL Compatible: All Inputs and Outputs

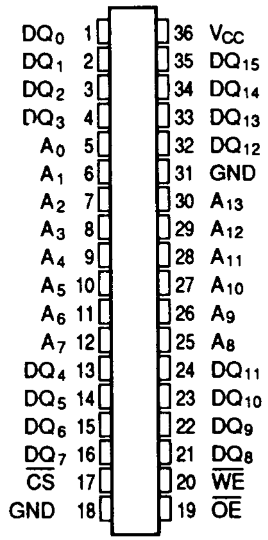
■ ORDERING INFORMATION

Part No.	Access	Package
HB66B1616A-25 HB66B1616A-35	25ns 35ns	36-pin dual in-line leaded type

■ PHYSICAL OUTLINE



■ PIN ASSIGNMENT

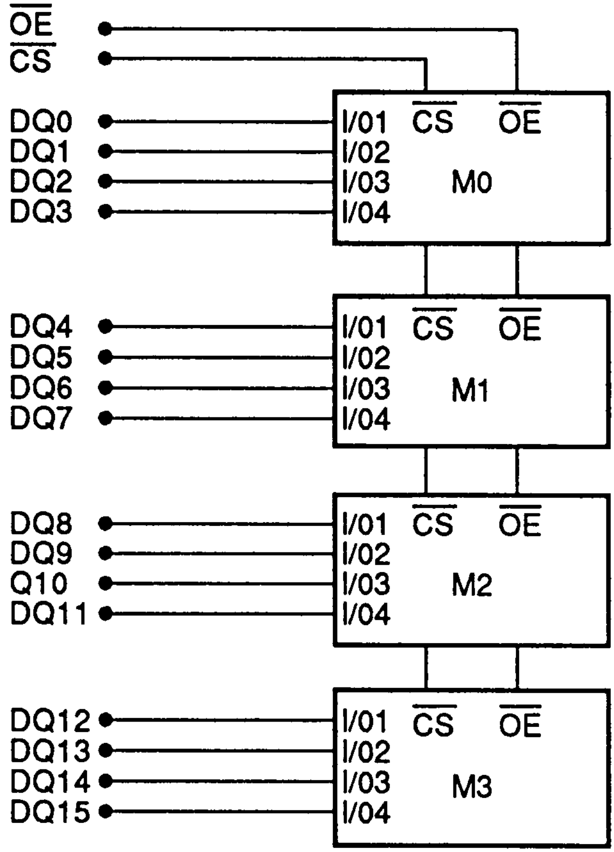


(Top View)

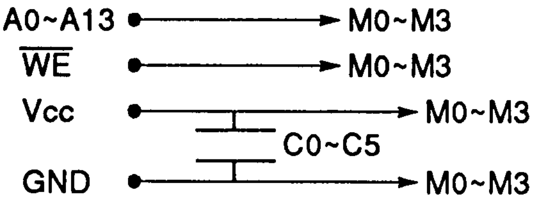
■ PIN DESCRIPTION

Pin Name	Function
$A_0 \sim A_{13}$	Address Input
$DQ_0 \sim DQ_{15}$	Data-in, Data-out
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply (+5V)
GND	Ground

■ BLOCK DIAGRAM



* M0~M3 : HM6289JP



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{in}	$-0.5^{(1)}$ to $+7.0$	V
Power Dissipation	P_T	4.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	-10 to +85	°C

NOTE: 1. V_{in} min. = -2.0V for pulse width ≤ 10ns.

■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	D_{out}	Read Cycle (1-3)
L	H	L	Write	I_{CC}	D_{in}	Write Cycle (1) (2)
L	L	L	Write	I_{CC}	D_{in}	Write Cycle (3-6)

NOTE: X means don't care.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{SS}	0.0	0.0	0.0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	$-0.5^{(1)}$	—	0.8	V

NOTE: 1. V_{IL} min. = -2.0V for pulse width ≤ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Parameter	Symbol	Test Condition	Min.	Typ.$^{(1)}$	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., $V_{in} = V_{SS}$ to V_{CC}	-10	—	10	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$, $V_{I/O} = V_{SS}$ to V_{CC}	-2	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $I_{I/O}$ = 0mA Min. Cycle	—	240	480	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$ Min. Cycle	—	60	120	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS} = \geq V_{CC} -0.2V$ $0V \leq V_{in} \leq 0.2V$ or $V_{in} \geq V_{CC} -0.2V$	—	0.08	8	mA
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V

NOTE: 1. Typical limits are at V_{CC} = 5.0V, T_a = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)$^{(1)}$

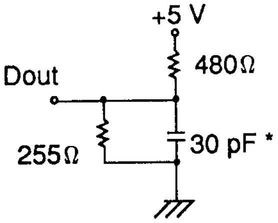
Parameter	Symbol	Test Conditions	Min.	Max.	Unit
Input Capacitance (Address, $\overline{CS}$, $\overline{OE}$, $\overline{WE}$)	C_{in}	V_{in} = 0V	—	35	pF
Input/Output Capacitance (DQ)	$C_{I/O}$	$V_{I/O}$ = 0V	—	15	pF

NOTE: 1. This parameter is sampled and not 100% tested.

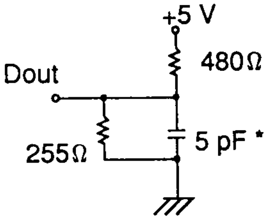
■ AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted.)

• Test Conditions

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Timing Reference Levels: 1.5V
- Input Rise and Fall Times: 5ns
- Output Load: See Figures



Output Load A



Output Load B
(for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} & t_{OW})

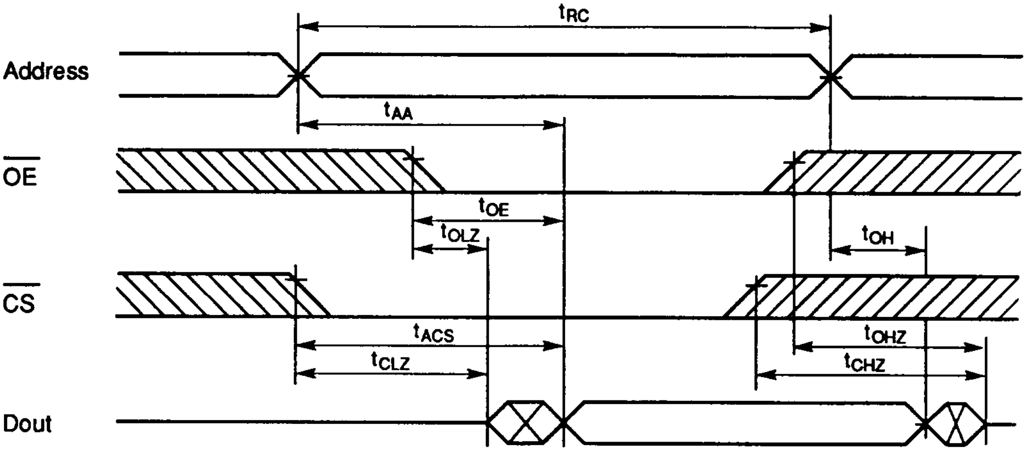
*Including scope and jig capacitance.

• Read Cycle

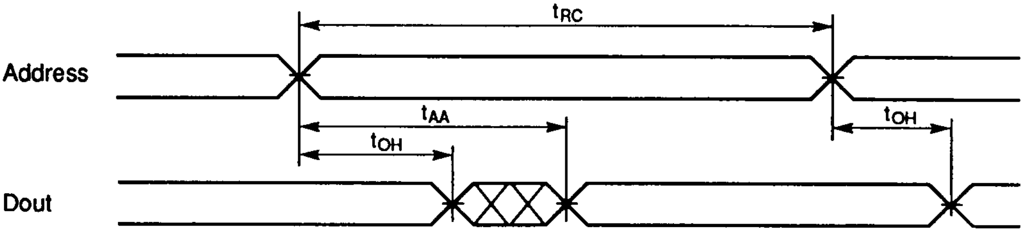
Parameter	Symbol	HB66B1616A-25		HB66B1616A-35		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	ns
Address Access Time	t_{AA}	—	25	—	35	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	ns
Chip Selection to Output in Low-Z	$t_{CLZ}^{(1)}$	5	—	5	—	ns
Output Enable to Output Valid	t_{OE}	—	12	—	15	ns
Output Enable to Output in Low-Z	$t_{OLZ}^{(1)}$	0	—	0	—	ns
Chip Deselection to Output in High-Z	$t_{CHZ}^{(1)}$	0	12	0	20	ns
Chip Disable to Output in High-Z	$t_{OHZ}^{(1)}$	0	10	0	10	ns
Output Hold from Address Change	t_{OH}	3	—	5	—	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	25	—	30	ns

NOTE: 1. Output transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

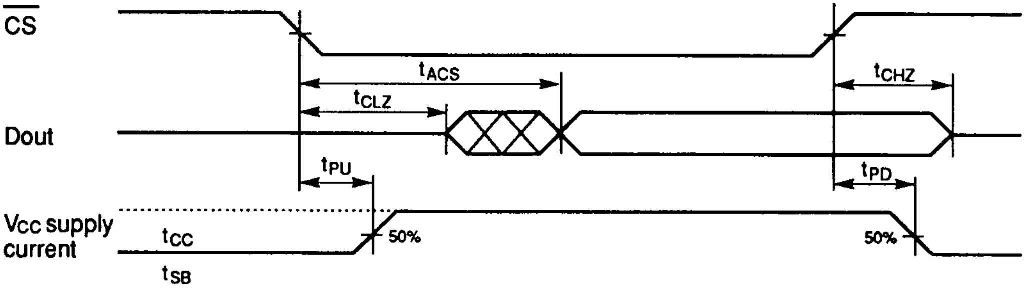
- **Read Timing Waveform (1)** (1)



- **Read Timing Waveform (2)** (1) (2) (4)



- **Read Timing Waveform (3)** (1) (3) (4)



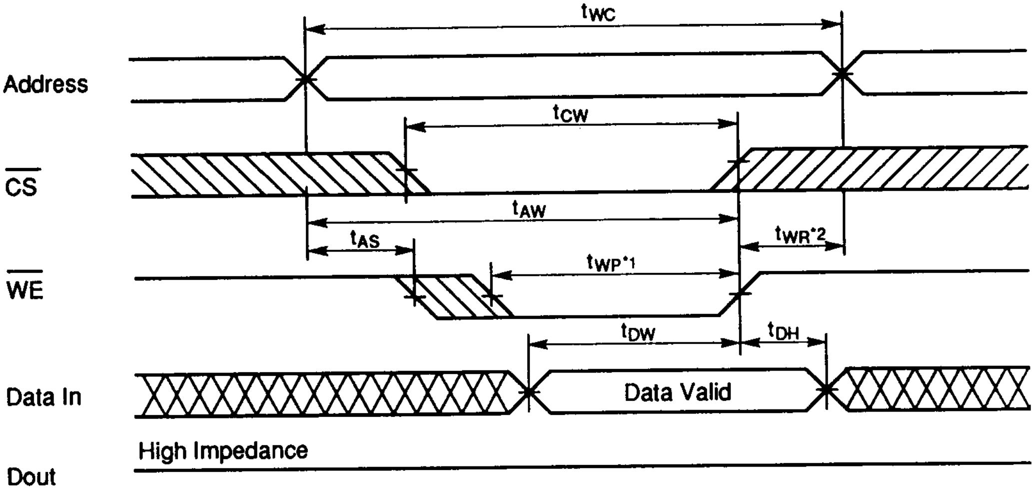
NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.

- **Write Cycle**

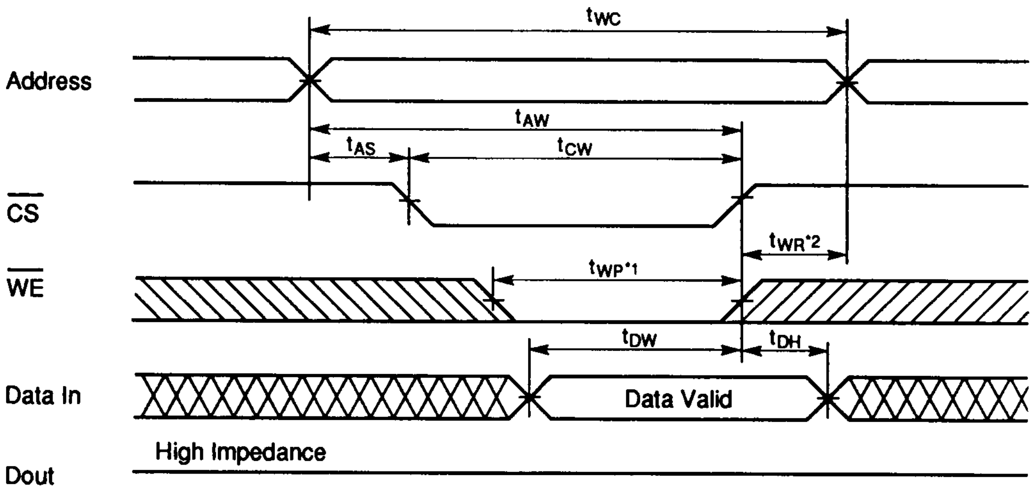
Parameter	Symbol	HB66B1616A-25		HB66B1616A-35		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	25	—	35	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	20	—	30	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Output Disable to Output in High-Z	t_{OHZ}(1)	0	10	0	10	ns
Write to Output in High-Z	t_{WHZ}(1)	0	8	0	10	ns
Data to Write Time Overlap	t_{DW}	12	—	20	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	ns
Output Active from End of Write	t_{OW}(1)	5	—	5	—	ns

NOTE: 1. Output transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

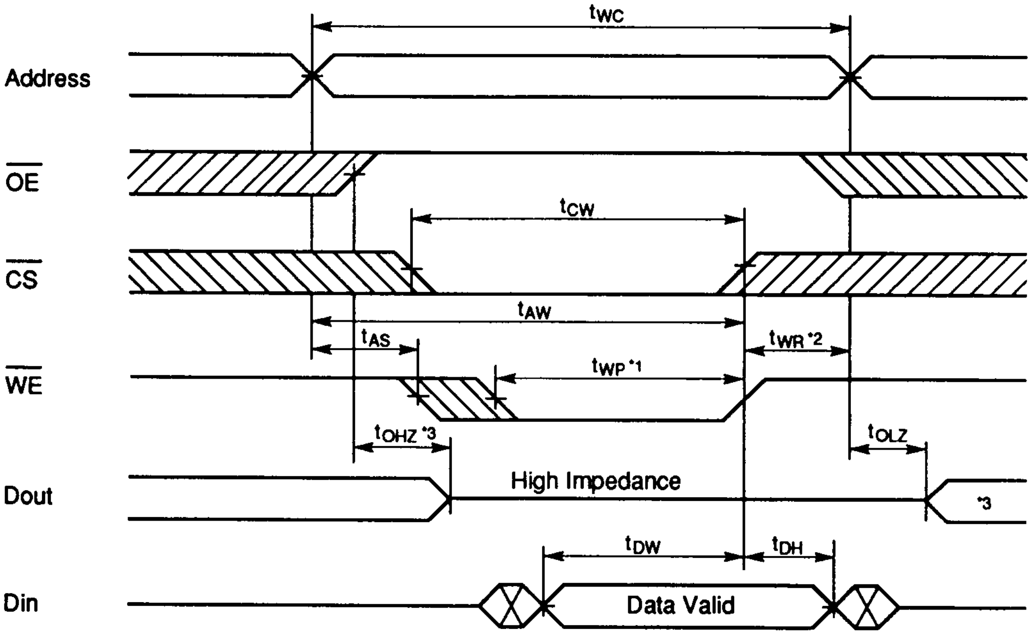
- **Write Timing Waveform (1)** ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



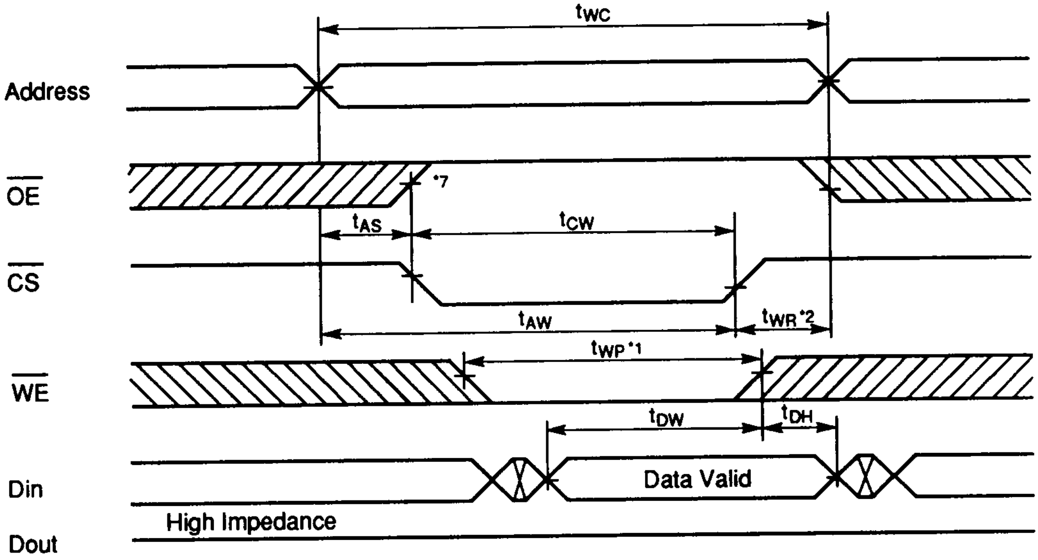
- **Write Timing Waveform (2)** ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



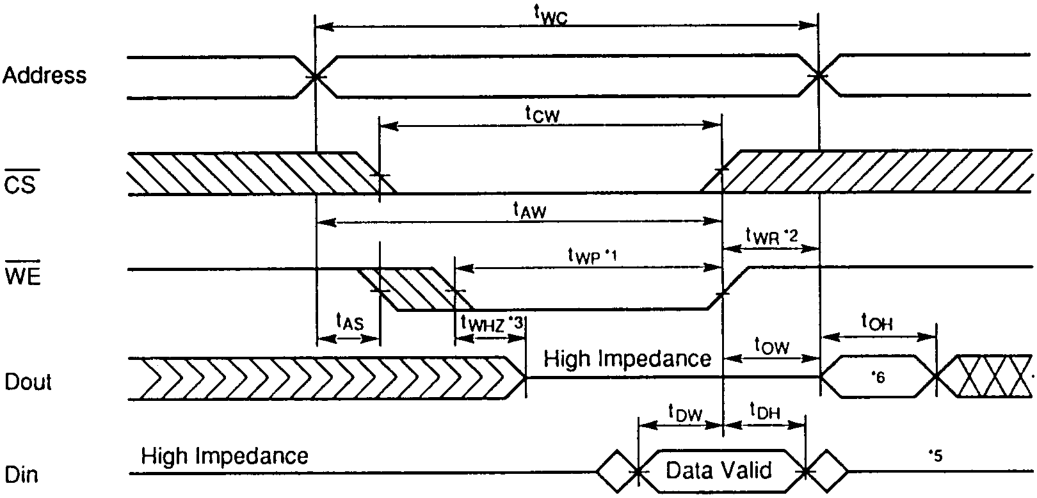
- **Write Timing Waveform (3)** ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



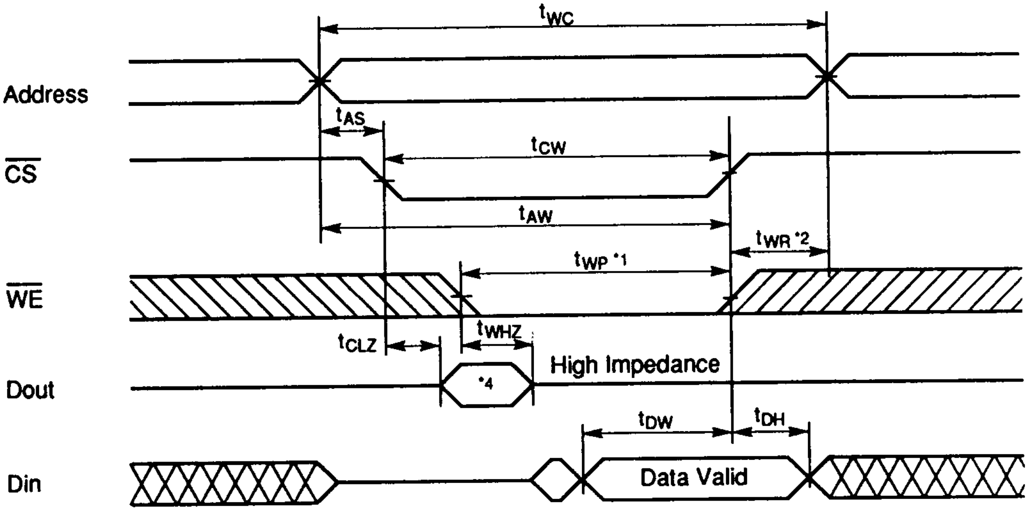
- **Write Timing Waveform (4)** ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



- **Write Timing Waveform (5)** ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



- **Write Timing Waveform (6)** ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



NOTES:

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after t_{OW}. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. D_{out} is the same phase of write data of this write cycle, if t_{WR} is long enough.
7. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, the output buffers remain in a high impedance state.