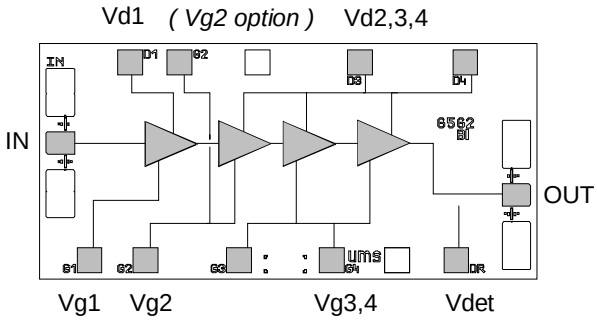
20-40GHz Medium Power Amplifier

GaAs Monolithic Microwave IC

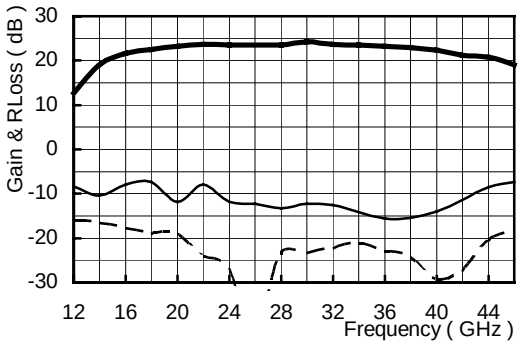
Description

The CHA3093 is a high gain broadband four-stage monolithic medium power amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.
A B.I.T. (Build In Test) monitors a DC voltage that is representative of the microwave output power.

The circuit is manufactured with a PM-HEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Typical on wafer measurements :



Input Rloss : dash line & output Rloss : solid line.

Main Features

- Broadband performances : 20-40GHz
- 20dBm output power.
- 22dB ±1.0dB gain
- Very good broadband input matching
- On chip output power level DC detector
- Low DC power consumption, 300mA @ 3.5V
- Chip size : 0.88 X 1.72 X 0.10 mm

Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	20		40	GHz
G	Small signal gain	18	20		dB
P03	Output power at 3dB gain compression	20	23		dBm
Id	Bias current		300	400	mA

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ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

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Electrical Characteristics for Broadband Operation

Tamb = +25°C, Vd1,2,3,4 = 3.5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	20		40	GHz
G	Small signal gain [in 20GHz to 35GHz](1)	20	22		dB
G	Small signal gain (1)	18	20		dB
ΔG	Small signal gain flatness (1)		±1.0		dB
Is	Reverse isolation (1)		50		dB
P1dB	Pulsed output power at 1dB compression (1)	18	20		dBm
P03	Output power at 3dB gain compression	20	23		dBm
IP3	3rd order intercept point		29		dBm
PAE	Power added efficiency at saturation		10		%
VSWRin	Input VSWR (1)			2.0:1	
VSWRout	Output VSWR (1)			3.0:1	
NF	Noise figure (2)			10.0	dB
Vdet	Detected voltage : at 25GHz@Pout=20dBm Detected voltage : at 38GHz@Pout=20dBm		0.8 0.4		V V
Id	Bias current (2)		300	400	mA

(1) These values are representative for pulsed on-wafer measurements that are made without bonding wires at the RF ports. In the case of a jig or a module CW mode operation, the typical output power may be around 2dB less.
(2) Input matching is below 2:1 down to 10GHz.
(3) Voltage across an external 10kOhm parallele resistor connected to the voltage detector pad.

Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	5.0	V
Id	Drain bias current	500	mA
Vg	Gate bias voltage	-2.0 to +0.4	V
Pin	Maximum peak input power overdrive (2)	+15	dBm
Ta	Operating temperature range	-40 to +85	°C

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Tstg	Storage temperature range	-55 to +155	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

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Typical Scattering Parameters *(On wafer Sij measurements)*

Bias Conditions : Vd1,2,3,4 = 3.5 Volt, Vg1,2,3,4 = -0.15 Volt, Id = 300 mA.

Freq. GHz	S11 dB	S11 /°	S12 dB	S12 /°	S21 dB	S21 /°	S22 dB	S22 /°
10.0	-13.3	138.0	-70.1	178.4	1.6	174.0	-5.8	-177.2
11.0	-14.0	137.0	-72.1	95.4	6.6	143.7	-7.3	178.0
12.0	-14.5	137.3	-64.2	-174.5	10.9	111.5	-8.3	174.0
13.0	-14.8	136.5	-68.9	123.0	15.1	74.6	-10.6	179.4
14.0	-15.1	133.5	-66.4	179.8	17.7	36.1	-9.9	-169.8
15.0	-15.8	132.9	-66.5	164.5	19.5	-1.4	-8.6	-172.9
16.0	-16.2	129.0	-63.8	-167.5	20.8	-38.1	-7.8	-173.7
17.0	-17.5	129.6	-61.0	161.9	21.2	-72.1	-6.9	173.7
18.0	-17.8	131.1	-61.5	150.7	21.8	-99.9	-7.3	164.6
19.0	-18.5	130.0	-57.6	132.3	21.9	-128.2	-7.5	155.8
20.0	-18.3	129.4	-63.4	122.7	23.2	-158.0	-10.8	149.5
21.0	-20.6	120.6	-57.2	116.0	22.4	172.2	-10.1	158.7
22.0	-22.9	139.6	-58.2	88.2	20.5	156.3	-7.4	141.8
23.0	-20.7	124.5	-51.6	48.4	22.0	144.4	-10.8	150.4
24.0	-25.1	133.7	-60.8	-167.2	23.2	106.2	-11.1	137.6
25.0	-26.1	129.3	-56.2	127.5	23.0	84.6	-12.2	145.2
26.0	-32.0	153.8	-55.3	96.6	22.9	62.8	-11.7	141.2
27.0	-28.8	-160.2	-60.8	92.0	22.9	41.8	-12.9	138.4
28.0	-25.1	-144.0	-57.2	103.2	23.1	19.9	-12.9	145.7
29.0	-22.7	-160.1	-55.7	90.9	22.7	-2.2	-11.7	145.2
30.0	-22.5	-154.6	-54.0	67.8	23.2	-18.7	-11.9	131.7
31.0	-20.9	-157.3	-58.2	68.9	23.3	-44.2	-13.6	127.7
32.0	-21.5	-160.9	-55.0	81.0	23.2	-64.6	-12.5	131.9
33.0	-20.2	-154.2	-52.7	58.7	23.1	-87.4	-12.9	111.7
34.0	-20.1	-160.0	-56.7	15.6	23.0	-107.2	-15.1	109.2
35.0	-19.7	-158.3	-57.8	56.8	22.9	-128.5	-16.3	102.4
36.0	-19.8	-163.5	-59.1	21.2	22.9	-147.9	-17.3	101.7
37.0	-19.6	-163.8	-60.2	60.7	22.9	-170.1	-17.6	85.3
38.0	-19.2	-162.4	-55.6	5.7	22.9	168.1	-19.1	61.2
39.0	-20.2	-173.2	-63.6	124.8	22.6	146.9	-20.9	40.0
40.0	-21.8	-176.4	-57.3	78.2	22.5	124.0	-19.4	12.3
41.0	-23.7	-173.2	-62.6	14.9	21.8	102.3	-17.7	-18.5
42.0	-26.1	-167.2	-60.1	92.4	21.7	78.6	-15.2	-39.3
43.0	-31.2	-138.4	-51.8	70.1	21.6	57.9	-12.7	-55.8
44.0	-27.3	-85.2	-54.2	56.5	21.5	34.7	-10.5	-69.3
45.0	-21.5	-92.9	-49.2	87.0	21.3	9.1	-8.3	-86.4
46.0	-26.2	-35.3	-46.5	-6.7	20.3	-16.3	-7.9	-101.5
47.0	-17.0	-27.4	-43.9	-55.8	20.1	-40.2	-7.8	-106.3
48.0	-11.6	-54.0	-39.1	-165.6	19.7	-67.5	-6.1	-111.4
49.0	-8.4	-55.8	-54.2	-160.8	18.9	-97.3	-4.9	-119.1
50.0	-5.7	-69.7	-44.5	-145.5	17.5	-129.8	-4.0	-126.7

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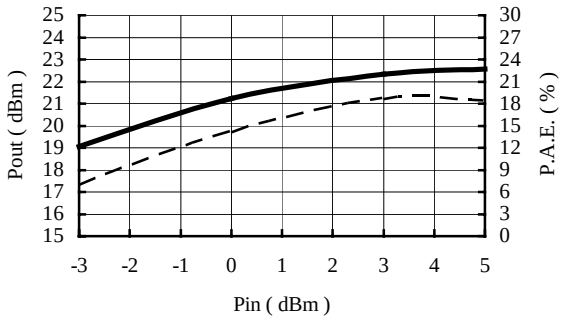
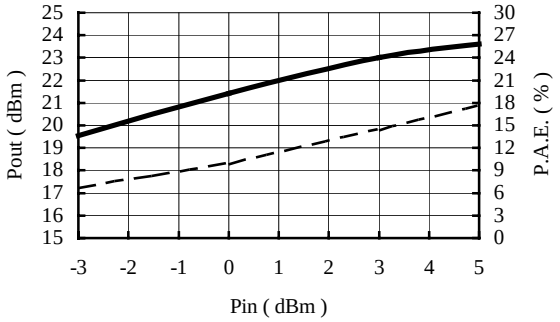
Typical On wafer Power Measurements

Bias Conditions : Vd1,2,3,4 = 3.5 Volt, Vg1,2,3,4 = -0.15 Volt, Id = 300 mA.

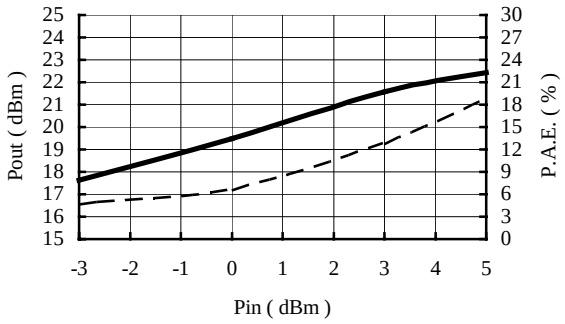
On wafer Pin / Pout at 20 GHz



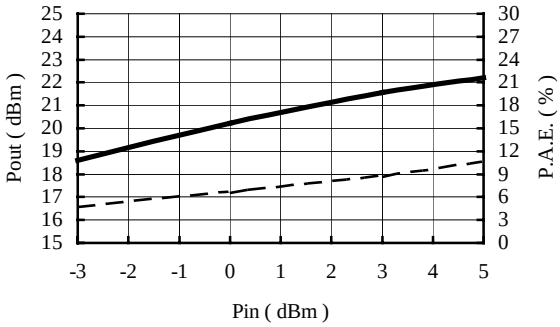
On wafer Pin / Pout at 28 GHz



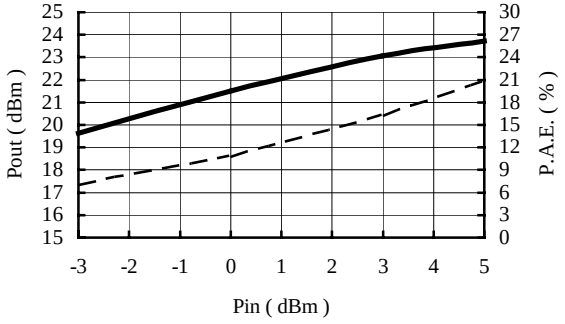
On wafer Pin / Pout at 22 GHz



On wafer Pin / Pout at 38 GHz



On wafer Pin / Pout at 26 GHz



Notes :

1- Test conditions :
Vd1,2,3,4 = 3.5 Volt, Vg1,2,3,4 = -0.15 Volt.

2- Power measurements are typical (solid lines). P.A.E. is representative of on wafer measurements on a typical circuit (Dotted lines).

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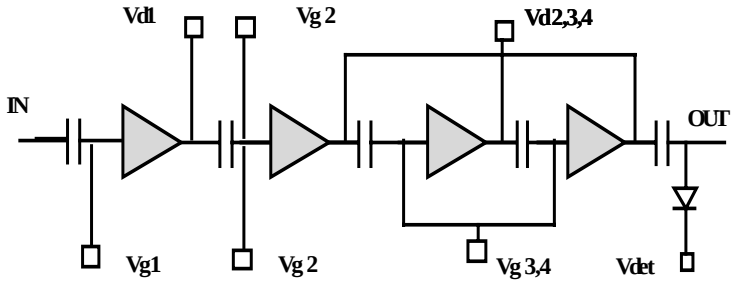
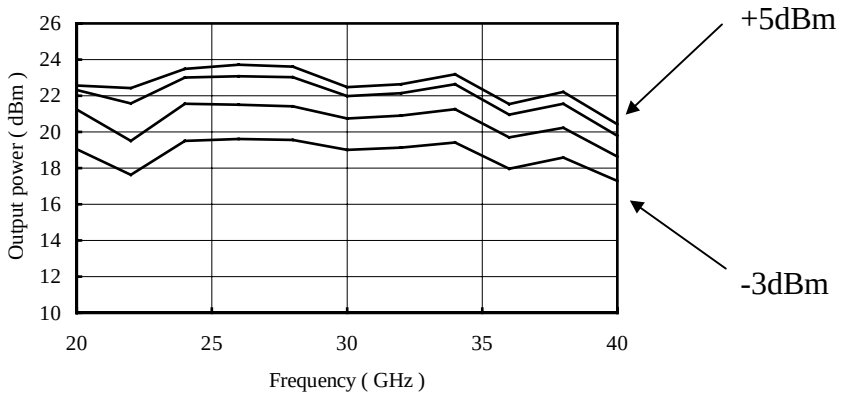
Typical Bias Tuning

The circuit schematic is given below :

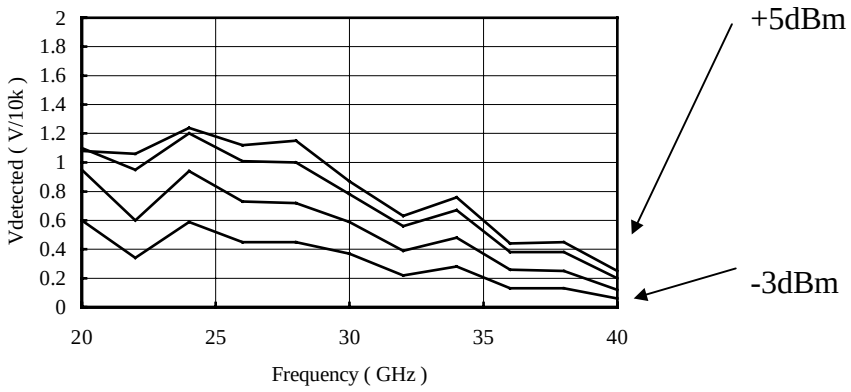


For medium power operation, the four drain biases are connected altogether. In a same way, all the gate biases are connected together at the same power supply, tuned to drive a small signal operating current of 300mA. A separate access to the gate voltages of the two first stages (Vg1,2) is provided in order to be able to tune the first stages for the application, as a lower noise amplifier or a multiplier.
An additional pad is provided for monitoring the output power, using the Build In Test. This access, when connected to an external resistor of 10 kOhm (typical value) provides a DC voltage which follows the output power level.

On wafer power measurements for fixed input power of -3dBm, 0 dBm +3dBm & +5 dBm.



On wafer detected voltage for fixed input power of -3dBm, 0 dBm +3dBm & +5 dBm.



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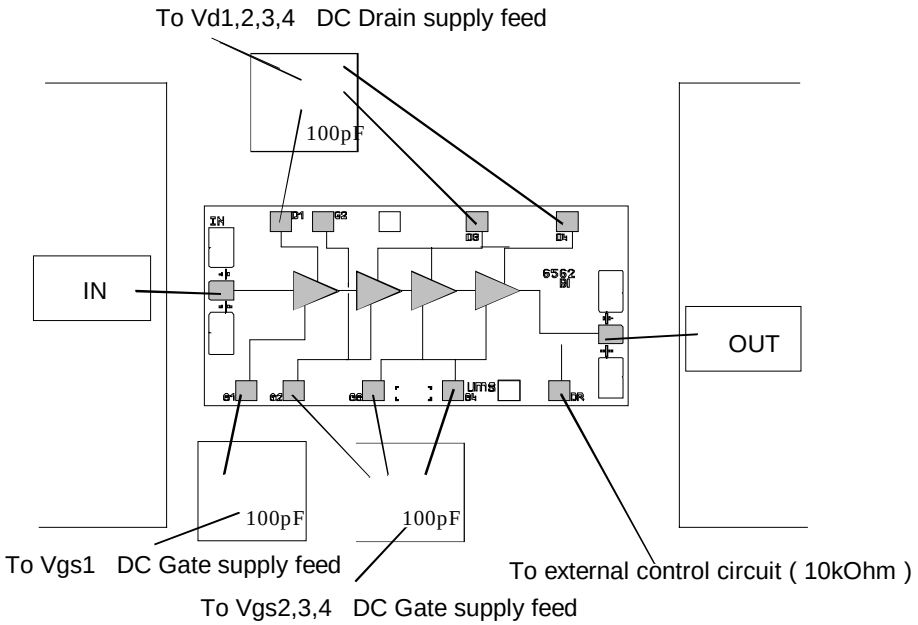
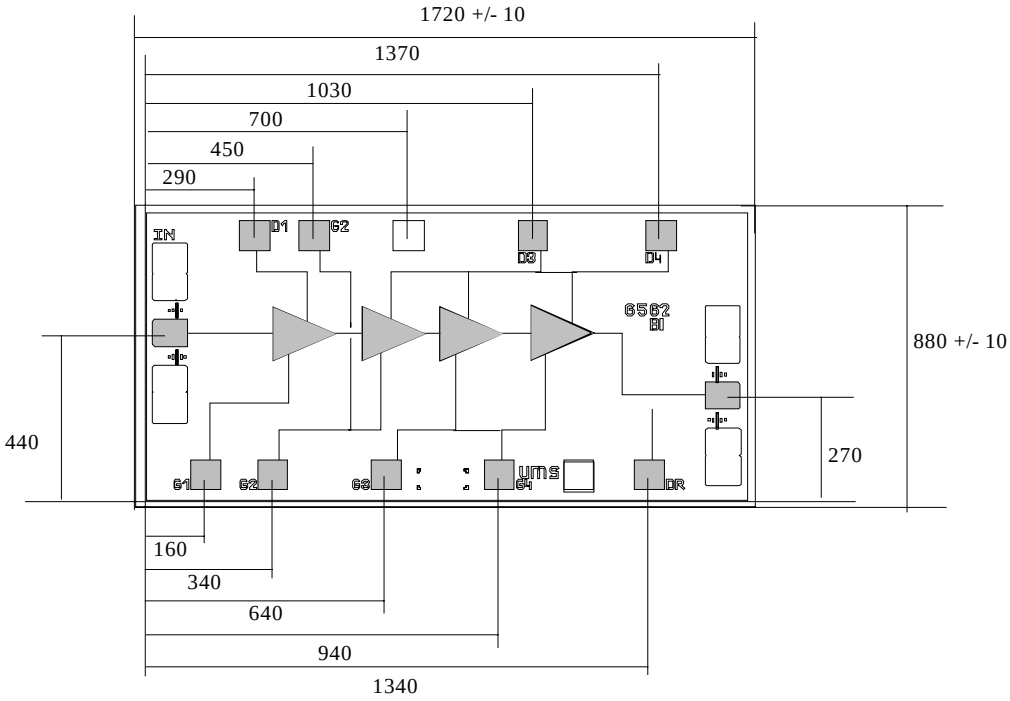
Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is recommended.



Bonding pad positions.

(Chip thickness : 100µm. All dimensions are in micrometers)

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Ordering Information

Chip form : CHA3093a99F/00

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