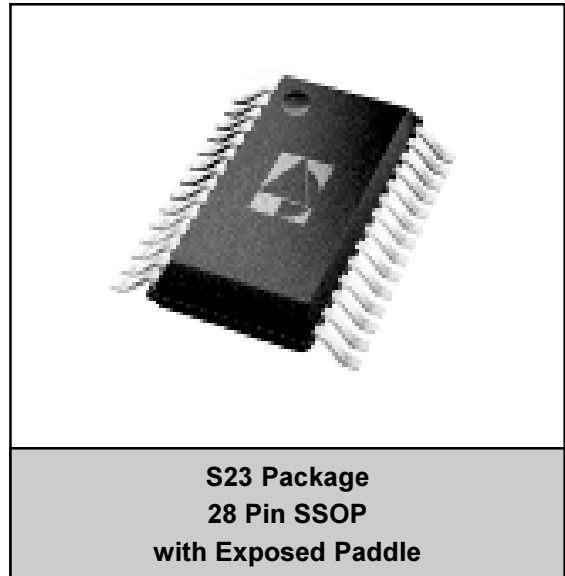


FEATURES

- Low cost integrated amplifier with step attenuator
- Attenuation Range: 0-56 dB, adjustable in 2 dB increments via a 3 wire serial control
- Meets DOCSIS distortion requirements at a +60dBmV output signal level
- Programmable address allows multiple parts to share control bus
- Programmable 2 bit data port output
- Low distortion and low noise
- Frequency range: 5-100 MHz
- 5 Volt operation
- -40 to +85 °C temperature range

APPLICATIONS

- DOCSIS Compliant IP Telephony Systems
- CATV Interactive Set-Top Box
- OpenCable Set-Top Box
- Residential Gateway



PRODUCT DESCRIPTION

The ARA3000 is designed to provide additional reverse path amplification and isolation in IP Telephony systems. It incorporates a digitally controlled precision step attenuator, followed by a single-stage output amplifier that exceeds DOCSIS distortion and noise requirements at a +60dBmV output level while only requiring a single polarity +5V supply. The precision attenuator can handle input powers up to +58 dBmV, and provides up to 56 dB of

attenuation in 2 dB increments. The output amplifier stage can be shut down and bypassed by a low insertion loss switch on-chip to save power. The ARA3000 has a programmable address that allows multiple devices to share a common control bus, and a 2-bit data port for control of external devices. The ARA3000 is offered in a 28-pin SSOP package featuring an exposed paddle on the bottom of the package.

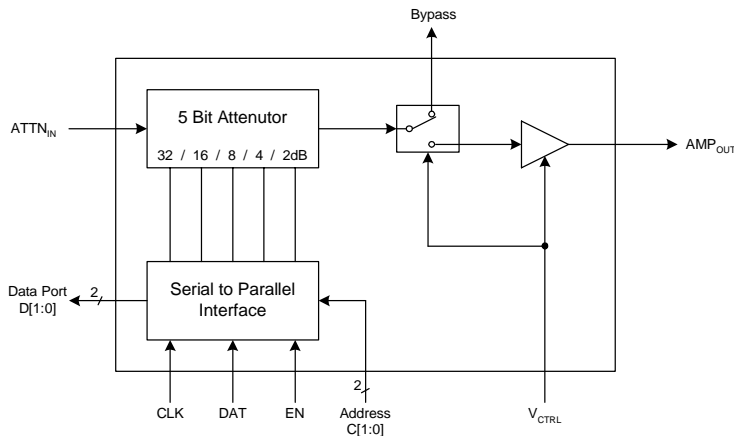


Figure 1. Functional Block Diagram

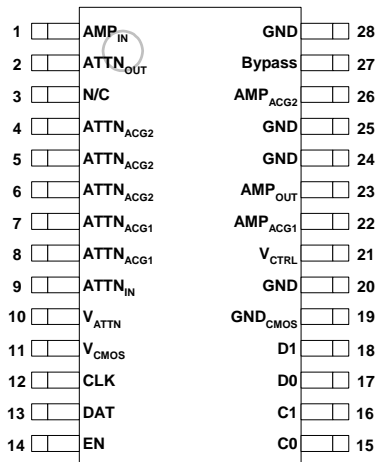


Figure 2: Pin Out

Table 1: Pin Description

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	AMP _{IN}	Amplifier Input	15	C0	Device Address 0
2	ATTN _{OUT}	Attenuator Output ⁽²⁾	16	C1	Device Address 1
3	N/C	No Connection ⁽¹⁾	17	D0	Data Port Output 0
4	ATTN _{ACG2}	Attenuator AC Ground 2 ⁽³⁾	18	D1	Data Port Output 1
5	ATTN _{ACG2}	Attenuator AC Ground 2 ⁽³⁾	19	GND _{CMOS}	Ground for Digital CMOS Circuit
6	ATTN _{ACG2}	Attenuator AC Ground 2 ⁽³⁾	20	GND	Ground
7	ATTN _{ACG1}	Attenuator AC Ground 1 ⁽³⁾	21	V _{CTRL}	Amplifier Control (Enable / Bypass)
8	ATTN _{ACG1}	Attenuator AC Ground 1 ⁽³⁾	22	AMP _{ACG1}	Amplifier AC Ground 1 ⁽³⁾
9	ATTN _{IN}	Attenuator Input ⁽²⁾	23	AMP _{OUT}	Amplifier Output
10	V _{ATTN}	Attenuator Supply	24	GND	Ground
11	V _{CMOS}	Supply For Digital CMOS Circuit	25	GND	Ground
12	CLK	Clock	26	AMP _{ACG2}	Amplifier AC Ground 2 ⁽³⁾
13	DAT	Data	27	Bypass	Amplifier Bypass Output ⁽²⁾
14	EN	Enable	28	GND	Ground

Notes:

(1) The N/C pin should be grounded

(2) Pins should be AC-coupled. No external DC bias should be applied.

(3) Pins should be AC-grounded. No external DC bias should be applied.

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Analog Supply (pins 10, 23)	0	9	VDC
Digital Supply: V _{CMOS} (pin 11)	0	6	VDC
Amplifier Control: V _{CTRL} (pin 21)	-5	6	V
RF Power at Input (pin 9)	-	58	dBmV
Digital Interface (pins 12, 13, 14, 15, 16)	-0.5	V _{CMOS} +0.5	V
Storage Temperature	-55	+200	°C
Soldering Temperature	-	260	°C
Soldering Time	-	5	Sec

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Notes:

1. Pins 2, 9 and 27 should be AC-coupled. No external DC bias should be applied.
2. Pin 1 should be pulled to ground through a resistor. No external DC bias should be applied.
3. Pins 4, 5, 6, 7, 8, 22 and 26 should be AC-grounded. No external DC bias should be applied.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT
Analog Supply: V _{DD} (pins 10, 23)	4.5	5	7	VDC
Digital Supply: V _{CMOS} (pin 11)	3.0	-	5.5	VDC
Digital Interface (pins 12, 13, 14, 15, 16)	0	-	V _{CMOS}	V
Amplifier Control: V _{CTRL} (pin 21)	0	3	5.5	V
Case Temperature	-40	25	85	°C

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Table 4: DC Electrical Specifications

$T_A=25^{\circ}\text{C}$; $V_{DD}, V_{CMOS} = +5.0\text{ VDC}$; $V_{CTRL} = +5.0\text{ V}$ (Amp enabled); $V_{CTRL} = 0\text{ V}$ (Amp bypassed)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Analog Supply Current (pins 10, 23)	- -	120 12	- -	mA	Amplifier enabled Amplifier bypassed
CMOS Digital Supply Current (pin 11)	-	2	-	mA	Max attenuation setting
Total Power Consumption	- -	610 70	- -	mW mW	Amplifier enabled Amplifier bypassed

Table 5: AC Electrical Specifications

$T_A=25^{\circ}\text{C}$; $V_{DD}, V_{CMOS} = +5.0\text{ VDC}$; $V_{CTRL} = +5.0\text{ V}$ (Amp enabled); $V_{CTRL} = 0\text{ V}$ (Amp bypassed)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Gain	14	16	-	dB	0 dB attenuation setting, amplifier enabled
	-2.5	-1.7	-	dB	0 dB attenuation setting, amplifier bypassed
Gain Flatness	-	0.5	-	dB	5 to 42 MHz
Gain Variation over Temperature	-	-0.006	-	dB/°C	
Attenuation Steps					
2 dB	1.54	1.75	2.0	dB	Monotonic
4 dB	3.6	3.9	4.2		
8 dB	7.7	8.1	8.3		
16 dB	15.5	15.9	16.3		
32 dB	30.2	30.7	31.2		
Maximum Isolation	-	60	-	dB	62 dB attenuation setting, amplifier disabled
2 nd Harmonic Distortion Level	-	-55	-48	dBc	$P_{OUT} = +60\text{ dBmV}$ into 75 Ohms, amplifier enabled
	-	-60	-48	dBc	$P_{IN} = +58\text{ dBmV}$ from 75 Ohms, amplifier bypassed
3 rd Harmonic Distortion Level	-	-60	-48	dBc	$P_{OUT} = +60\text{ dBmV}$ into 75 Ohms, amplifier enabled
	-	-60	-48	dBc	$P_{IN} = +58\text{ dBmV}$ from 75 Ohms, amplifier bypassed

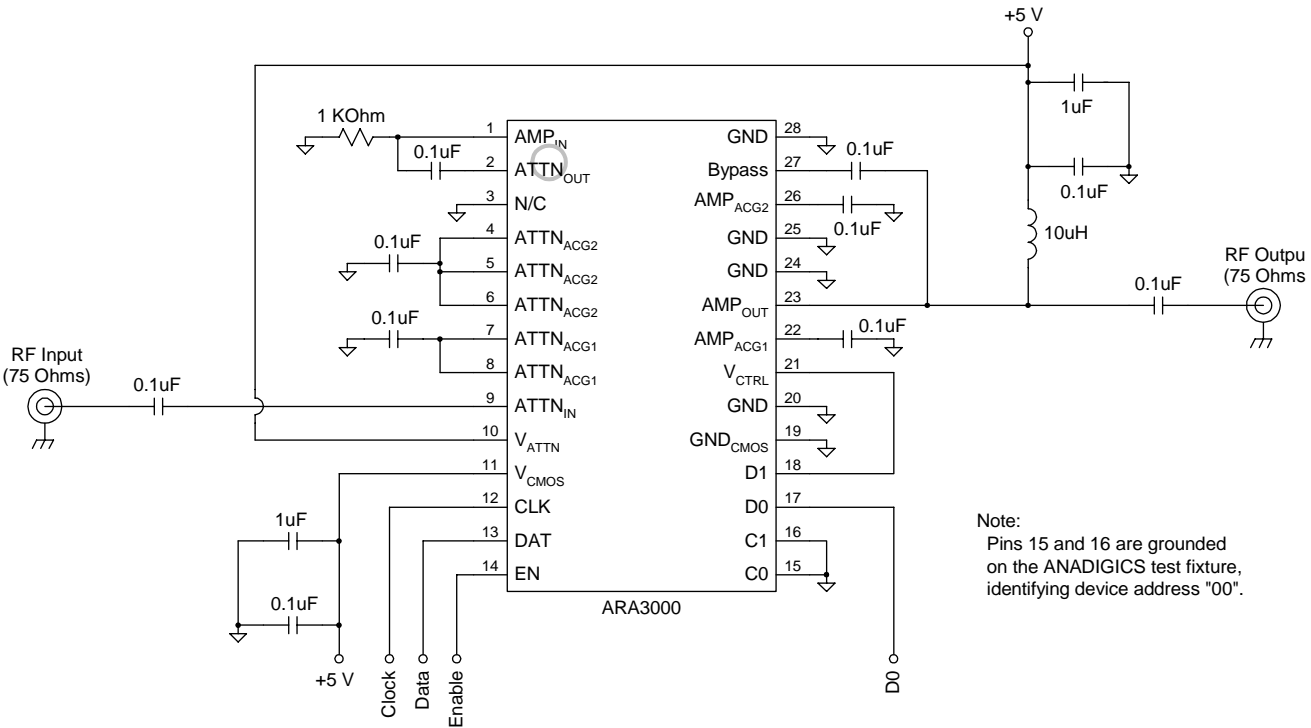
Note: As measured in ANADIGICS test fixture

continued: AC Electrical Specifications

$T_A=25^{\circ}\text{C}$; $V_{DD}, V_{CMOS} = +5.0\text{ VDC}$; $V_{CTRL} = +5.0\text{ V}$ (Amp enabled); $V_{CTRL} = 0\text{ V}$ (Amp bypassed)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
3rd Order Output Intercept	78	-	-	dBmV	Amplifier enabled
1 dB Gain Compression Point	-	70	-	dBmV	Amplifier enabled
Noise Figure	-	3.5	-	dB	
Input Impedance	-	75	-	Ohms	
Input Return Loss	-	-20 -13	-	dB	Amplifier enabled Amplifier bypassed
Output Impedance	-	75	-	Ohms	
Output Return Loss	-	-15 -13	-	dB	Amplifier enabled Amplifier bypassed

Note: As measured in ANADIGICS test fixture



Note:
 Pins 15 and 16 are grounded
 on the ANADIGICS test fixture,
 identifying device address "00".

Figure 3: Test Circuit

LOGIC PROGRAMMING

Programming Instructions

The programming word is set through a 16 bit shift register via the data, clock and enable lines. The data is entered in order with the most significant bit (MSB) first and the least significant bit (LSB) last.

The enable line must be low for the duration of the data entry, then set high to latch the shift register. The rising edge of the clock pulse shifts each data value into the register.

Table 6: Programming Word

DATA BIT	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Value	P7	P6	P5	P4	P3	P2	P1	P0	0	0	0	1	C1	C0	A1	A0

Table 7: Data Description

VALUE	REGISTER ADDRESS "00" FUNCTION	REGISTER ADDRESS "11" FUNCTION (1=on, 0=bypass)
P7	N/A	N/A
P6	N/A	N/A
P5	N/A	32 dB Attenuator Bit
P4	N/A	16 dB Attenuator Bit
P3	N/A	8 dB Attenuator Bit
P2	N/A	4 dB Attenuator Bit
P1	External Data Port 1 Output	2 dB Attenuator Bit
P0	External Data Port 0 Output	N/A

Table 8: Device Address

		LOGIC LEVEL INPUT TO ADDRESS DEVICE	
C1	C0	Pin 16 (C1)	Pin 15 (C0)
0	0	0	0
1	0	1	0
0	1	0	1
1	1	1	1

The device is selected when the logic inputs at pins 16 and 15 match the values of data bits C1 and C0, respectively.

Table 9: Register Address

A1	A0	FUNCTION
0	0	Data Port Output Enabled
1	1	Attenuator Control Enabled

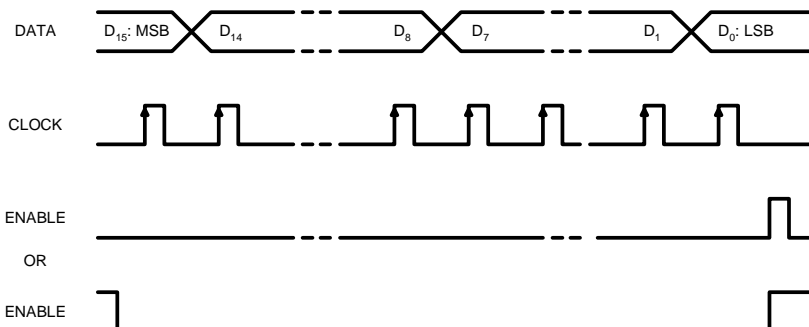


Figure 4: Serial Data Input Timing

APPLICATION INFORMATION

Amplifier Enable and Disable/Bypass

The amplifier in the ARA3000 can be shut down and bypassed via external control pin V_{CTRL} (pin 21). By applying a logic high voltage to this pin, the amplifier is enabled and the output is routed to AMP_{OUT} (pin 23). A logic low will disable the amplifier, bypass it, and route the attenuator output to the Bypass pin (pin 27).

A practical way to implement amplifier control is to connect one of the data port outputs to the V_{CTRL} input, allowing the attenuator to be controlled through the serial programming interface.

Output Power Control

The amplifier is designed to achieve the specified distortion levels at a nominal output power of +60 dBmV. When higher input powers are applied to the device, the attenuator should be adjusted to maintain the appropriate output power.

Thermal Layout Considerations

The device package for the ARA3000 features an

exposed paddle on the bottom of the package body. Use of the paddle is an integral part of the device design. Soldering this paddle to the ground plane of the PC board will ensure the lowest possible thermal resistance for the device, and will result in the longest MTF (mean time to failure.)

A PC board layout that optimizes the benefits of the paddle is shown in Figure 5. The via holes located under the body of the device must be plated through to a ground plane layer of metal, in order to provide a sufficient heat sink. The recommended solder mask outline is shown in Figure 6.

ESD Sensitivity

Electrostatic discharges can cause permanent damage to this device. Electrostatic charges accumulate on test equipment and the human body, and can discharge without detection. Proper precautions and handling are strongly recommended. Refer to the ANADIGICS application note on ESD precautions.

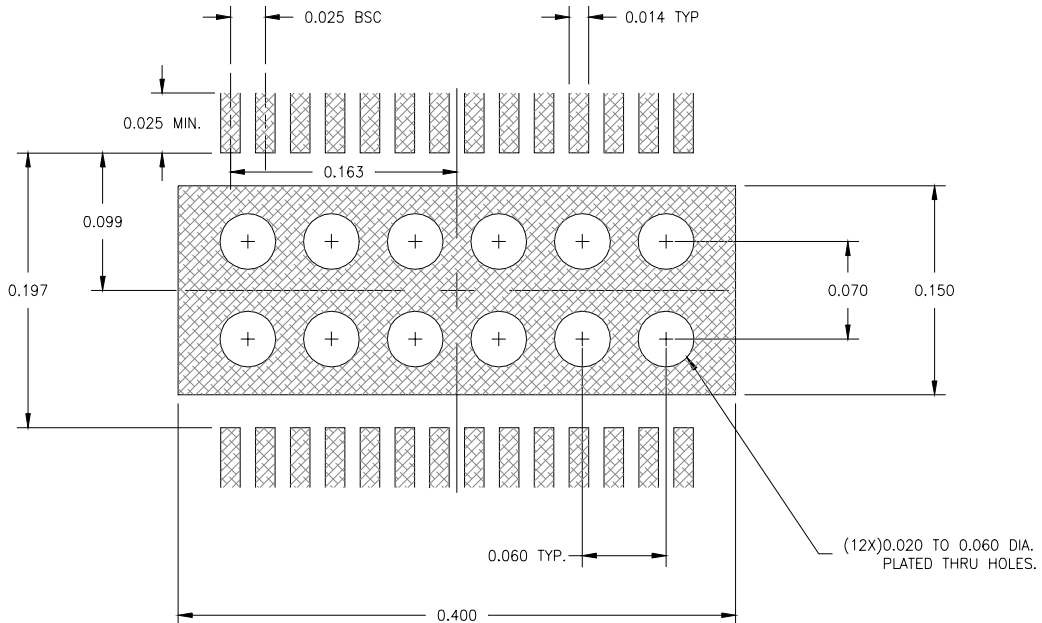


Figure 5: PC Board Layout

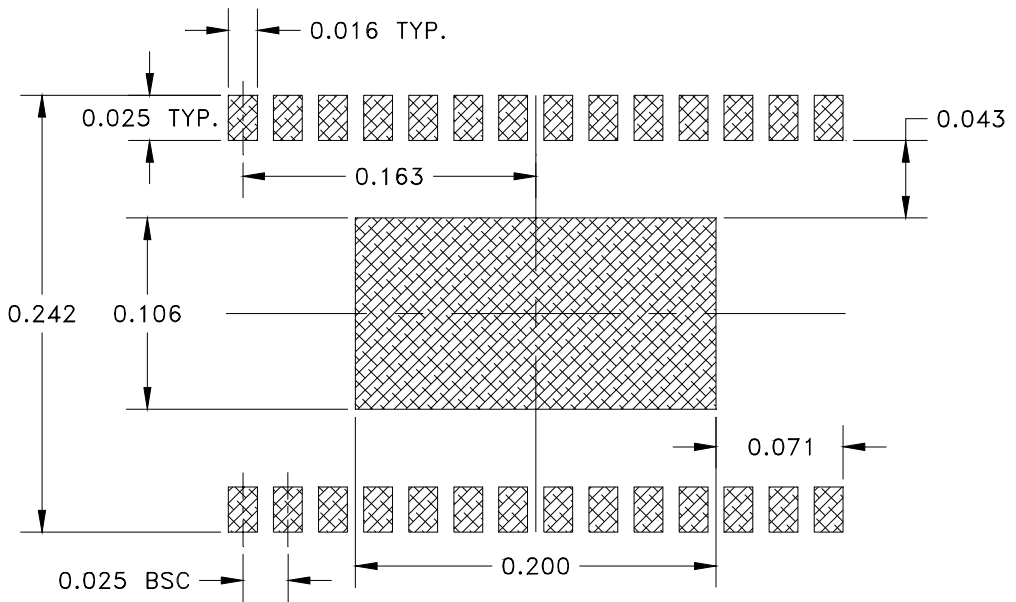
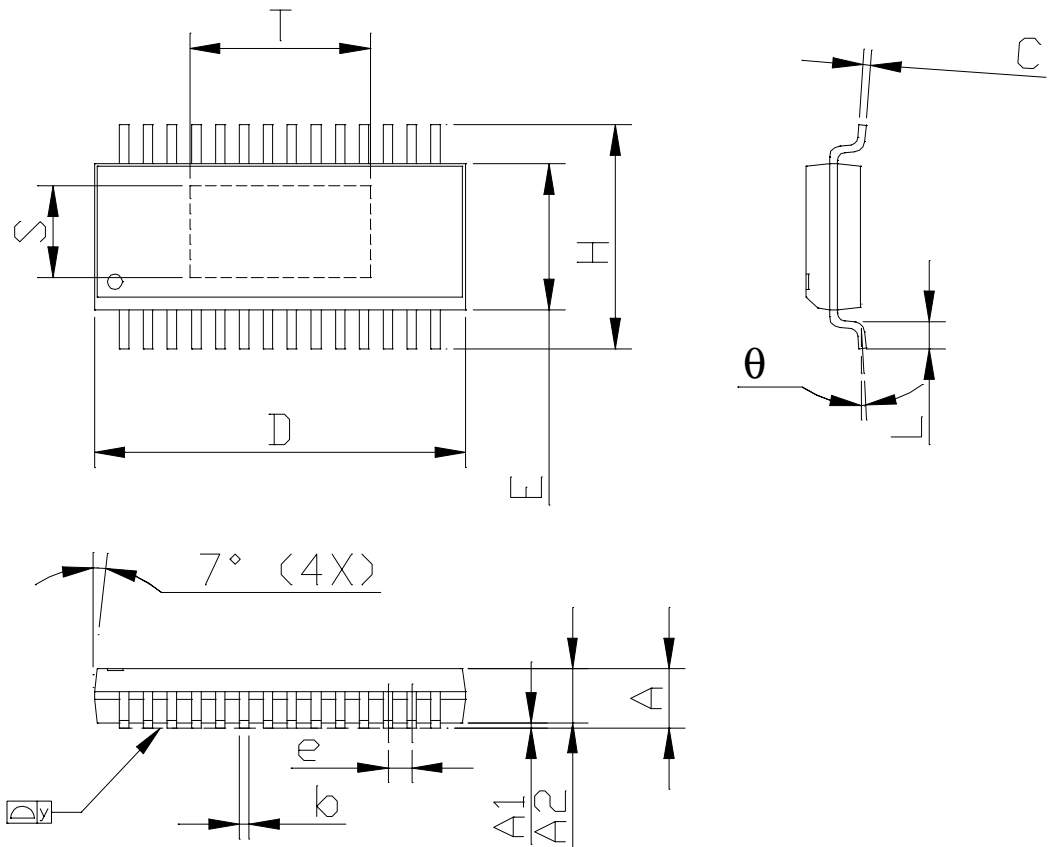


Figure 6: Solder Mask Outline

PACKAGE OUTLINE



- NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS
 2. TOLERANCE 0.004in.[0.10 mm] UNLESS OTHERWISE SPECIFIED
 3. CONTROLLING DIMENSION ARE INCHES.
 4. REF. - MO-137

SYMBOLS	DIMENSIONS IN INCHES		DIMENSIONS IN MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.057	0.061	1.45	1.55
A1	0.000	0.004	0.00	0.10
A2	0.057 (NOMINAL)		1.45 (NOMINAL)	
b	0.008	0.012	0.20	0.30
C	0.007	0.010	0.18	0.25
D	0.386	0.394	9.80	10.00
E	0.150	0.157	3.81	4.00
H	0.228	0.244	5.80	6.20
e	0.025 BSC		.64 BSC	
L	0.016	0.050	0.40	1.27
y	---	0.004	---	0.10
θ	0°	8°	0°	8°
T	---	0.190	---	4.82
S	---	0.096	---	2.43

Figure 7: S23 Package Outline - 28 Pin SSOP with Exposed Paddle

COMPONENT PACKAGING

Volume quantities of the ARA3000 are supplied on tape and reel. Each reel holds 3,500 pieces. Smaller quantities are available in plastic tubes of 50 pieces.

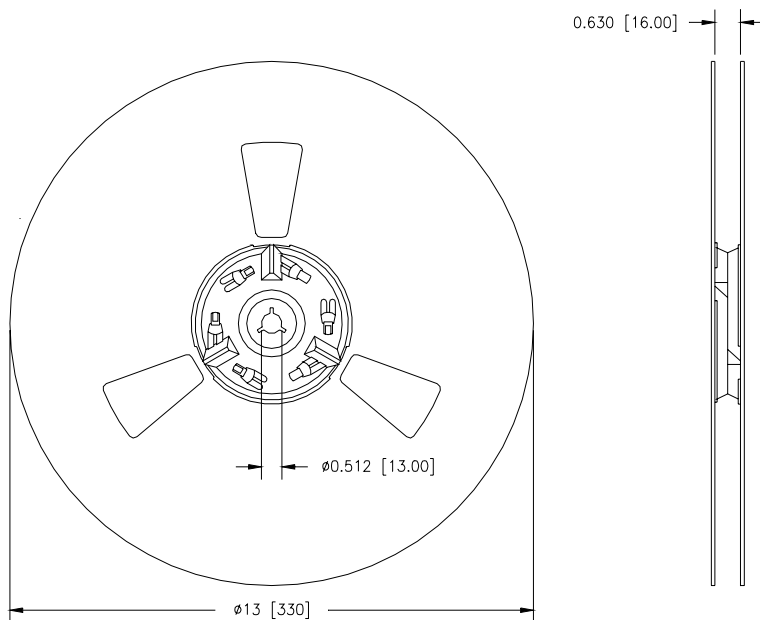


Figure 8: Reel Dimensions

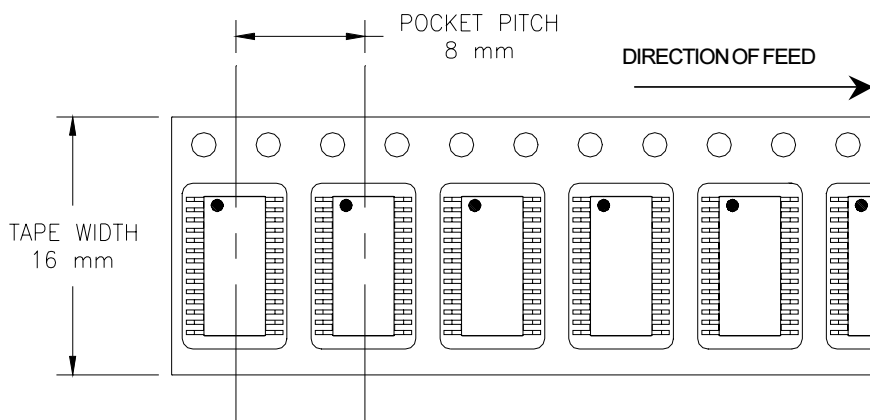


Figure 9: Tape Dimensions

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
ARA3000S23P1	-40 to 85 °C	28 Pin SSOP with Exposed Paddle	3,500 piece tape and reel
ARA3000S23P0	-40 to 85 °C	28 Pin SSOP with Exposed Paddle	Plastic tubes (50 pieces per tube)

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