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April 2015

# FDMC86262P

## P-Channel PowerTrench<sup>®</sup> MOSFET -150 V, -2 A, 307 mΩ

### Features

- Max  $r_{DS(on)}$  = 307 mΩ at  $V_{GS} = -10$  V,  $I_D = -2$  A
- Max  $r_{DS(on)}$  = 356 mΩ at  $V_{GS} = -6$  V,  $I_D = -1.8$  A
- Very Low  $r_{DS(on)}$  Mid Voltage P-Channel Silicon Technology Optimised for Low Qg
- Optimised for Fast Switching Applications as well as Load Switch Applications
- 100% UIL Tested
- RoHS Compliant

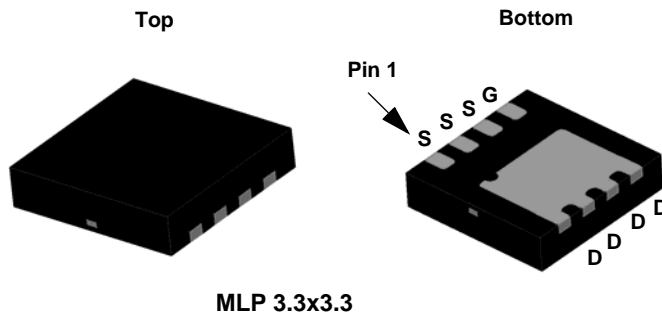


### General Description

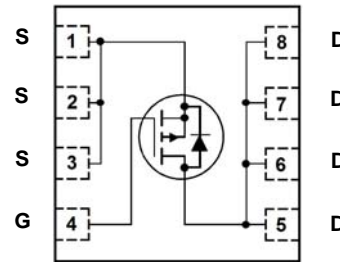
This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> technology. This very high density process is especially tailored to minimize on-state resistance and optimized for superior switching performance.

### Applications

- Active Clamp Switch
- Load Switch



MLP 3.3x3.3



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-150	V
$V_{GS}$	Gate to Source Voltage	$\pm 25$	V
$I_D$	Drain Current -Continuous	$T_C = 25^\circ\text{C}$ (Note 5)	-8.4
	-Continuous	$T_C = 100^\circ\text{C}$ (Note 5)	-5.3
	-Continuous	$T_A = 25^\circ\text{C}$ (Note 1a)	-2
	-Pulsed	(Note 4)	-35
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	37
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	40
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	2.3
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3.1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86262P	FDMC86262P	Power 33	13"	12 mm	3000 units

FDMC86262P P-Channel PowerTrench<sup>®</sup> MOSFET

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250 \mu\text{A}, V_{GS} = 0 \text{ V}$	-150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		-86		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -120 \text{ V}, V_{GS} = 0 \text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250 \mu\text{A}$	-2	-2.9	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10 \text{ V}, I_D = -2 \text{ A}$		241	307	m $\Omega$
		$V_{GS} = -6 \text{ V}, I_D = -1.8 \text{ A}$		266	356	
		$V_{GS} = -10 \text{ V}, I_D = -2 \text{ A}, T_J = 125^\circ\text{C}$		425	541	
$g_{FS}$	Forward Transconductance	$V_{DS} = -10 \text{ V}, I_D = -2 \text{ A}$		5.4		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -75 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		632	885	pF
$C_{oss}$	Output Capacitance			45	65	pF
$C_{rss}$	Reverse Transfer Capacitance			1.3	2.0	pF
$R_g$	Gate Resistance		0.1	3	6	$\Omega$

### Switching Characteristics

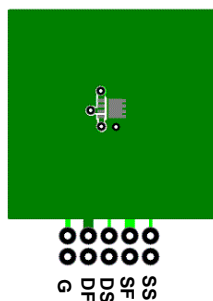
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -75 \text{ V}, I_D = -2 \text{ A}, V_{GS} = -10 \text{ V}, R_{GEN} = 6 \Omega$		8.5	17	ns	
$t_r$	Rise Time			2.2	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			15	26	ns	
$t_f$	Fall Time			5.6	11	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0 \text{ V to } -10 \text{ V}$		9.1	13	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ V to } -6 \text{ V}$	$V_{DD} = -75 \text{ V}, I_D = -2 \text{ A}$		5.6	7.9	nC
$Q_{gs}$	Gate to Source Charge				2.5		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				1.6		nC

### Drain-Source Diode Characteristics

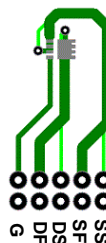
$V_{SD}$	Source-Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = -2 \text{ A}$ (Note 2)		-0.8	-1.3	V
$t_{rr}$	Reverse Recovery Time	$I_F = -2 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		72	116	ns
$Q_{rr}$	Reverse Recovery Charge			166	266	nC

Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $53^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b)  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty cycle < 2.0%.

3. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3 \text{ mH}$ ,  $I_{AS} = -5 \text{ A}$ ,  $V_{DD} = -150 \text{ V}$ ,  $V_{GS} = -10 \text{ V}$ .

4. Pulsed Id please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.

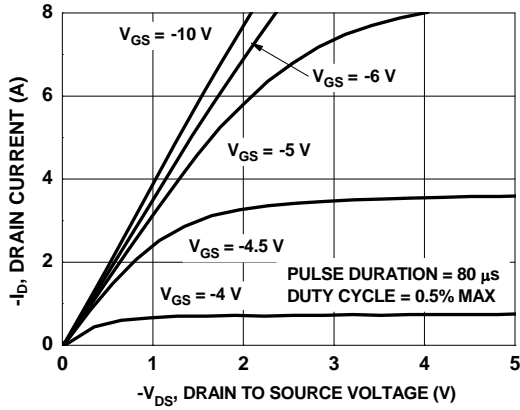


Figure 1. On Region Characteristics

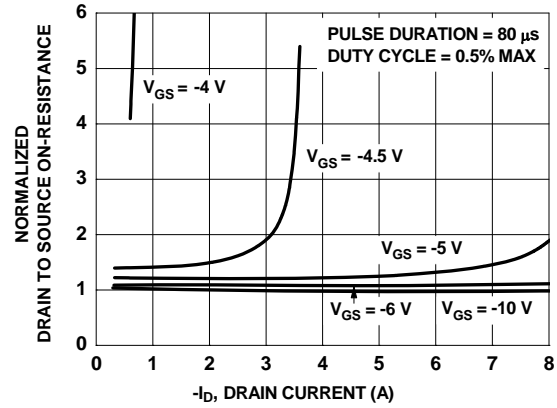


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

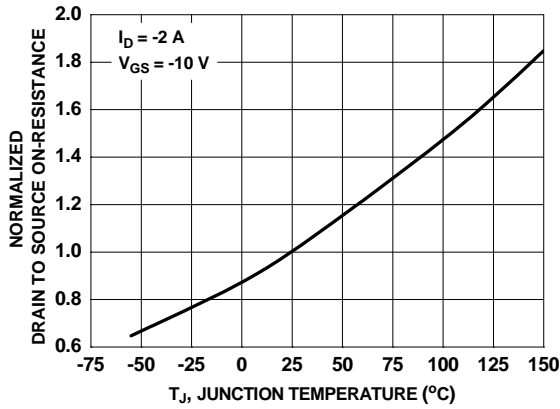


Figure 3. Normalized On Resistance vs. Junction Temperature

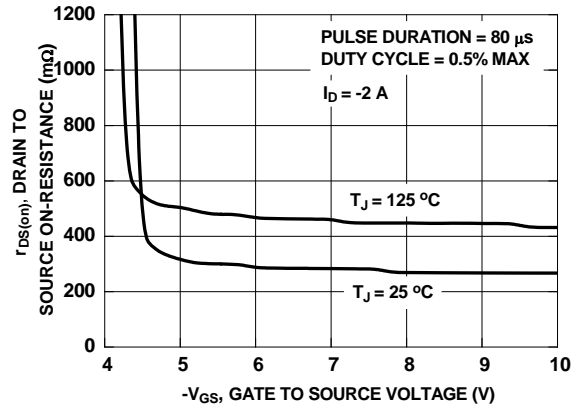


Figure 4. On-Resistance vs. Gate to Source Voltage

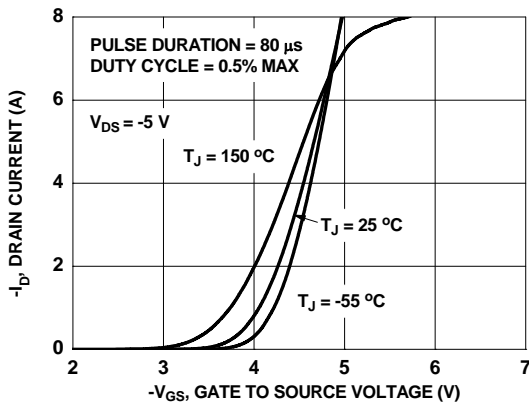


Figure 5. Transfer Characteristics

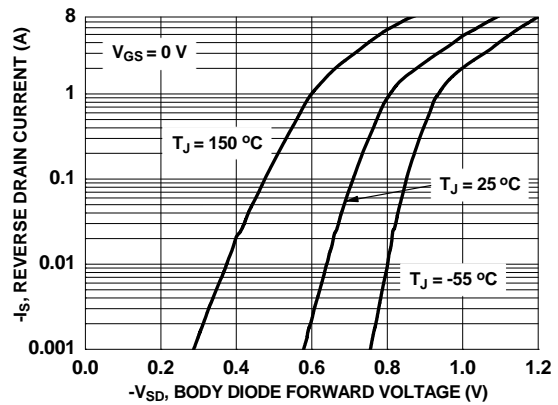
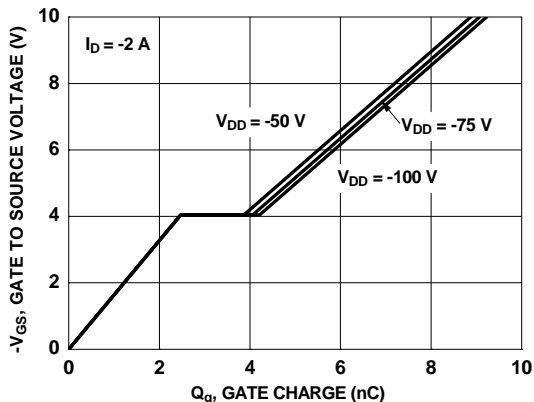
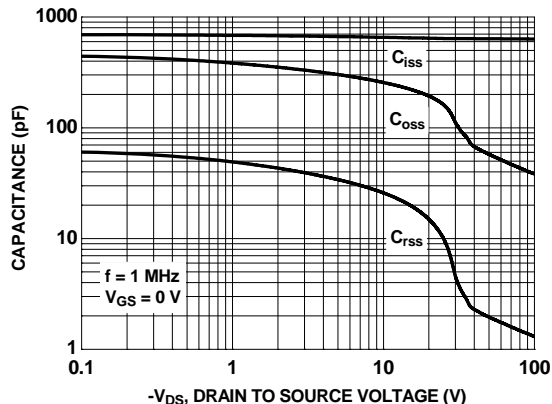


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

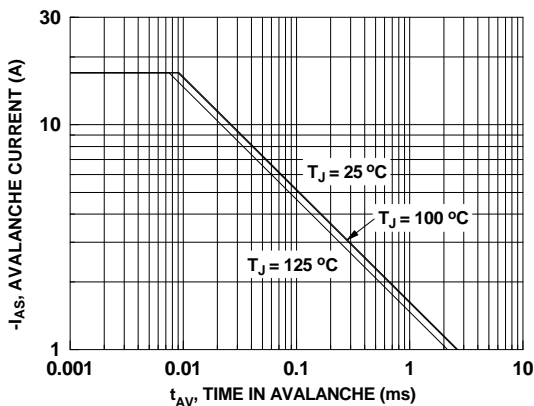
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



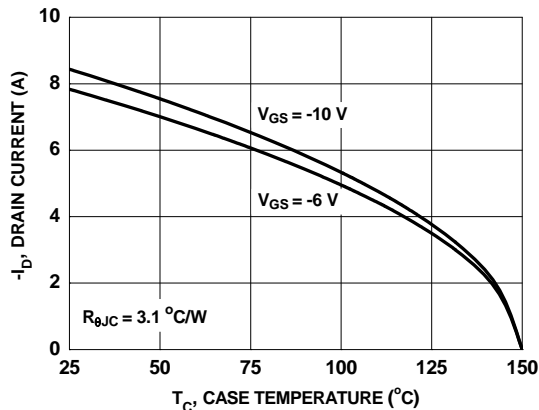
**Figure 7. Gate Charge Characteristics**



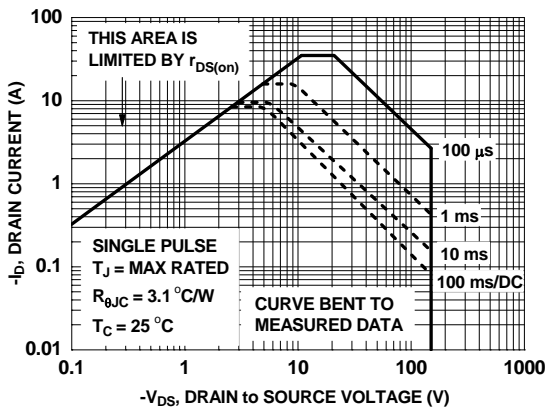
**Figure 8. Capacitance vs. Drain to Source Voltage**



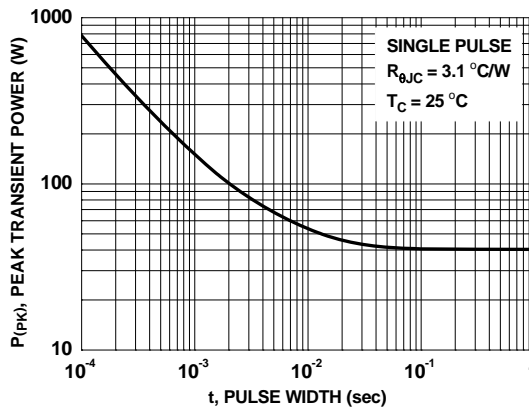
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

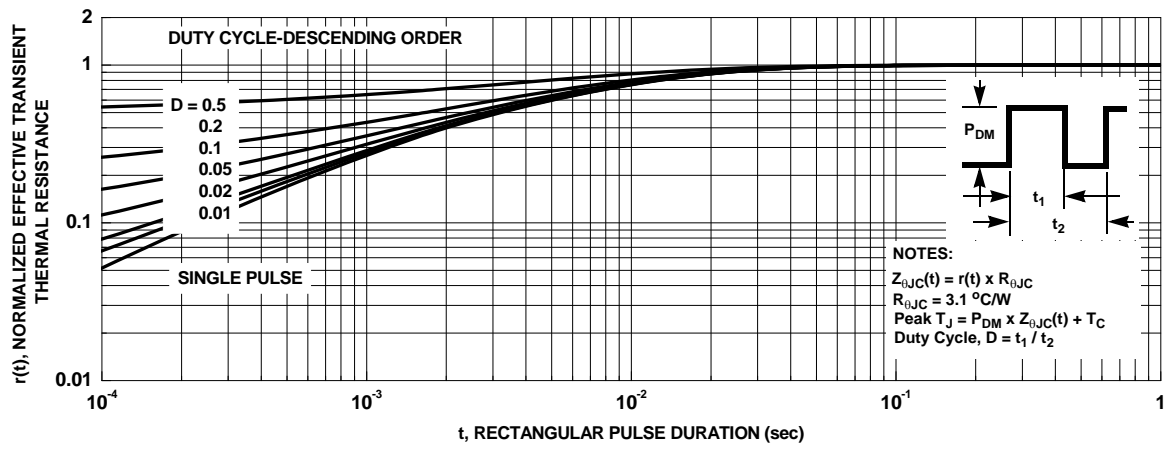


**Figure 11. Forward Bias Safe Operating Area**

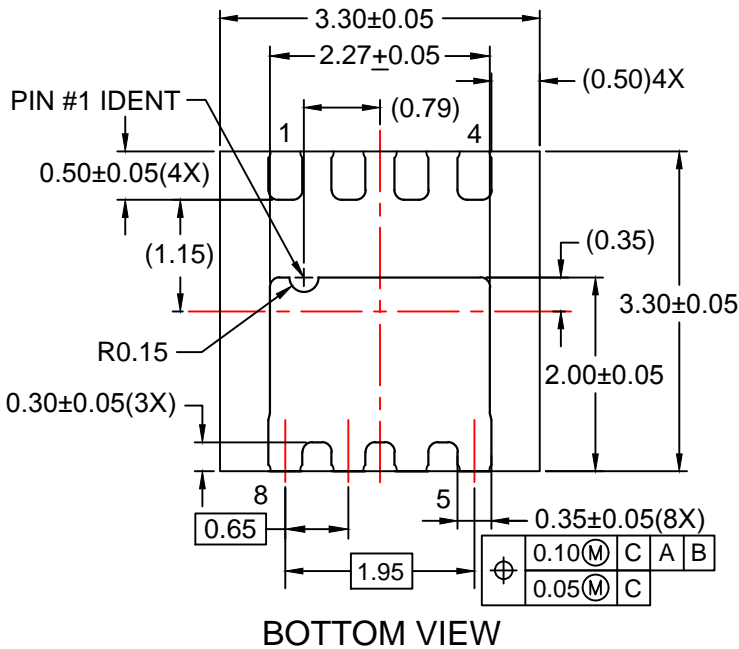
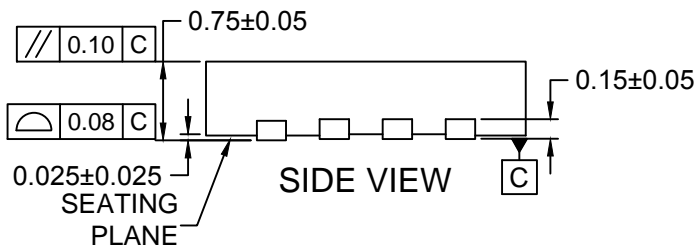
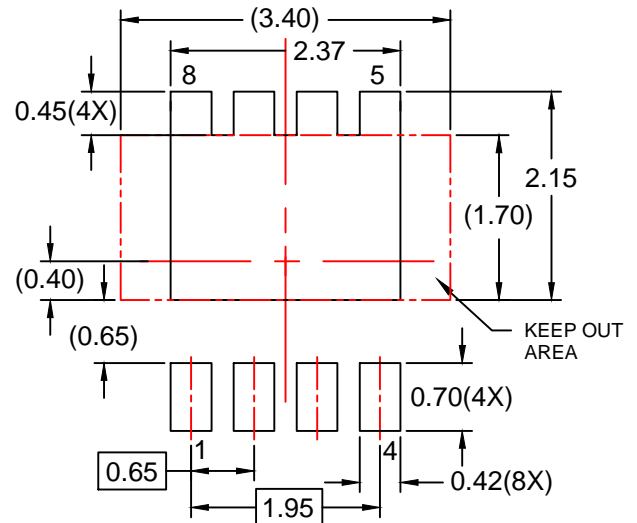
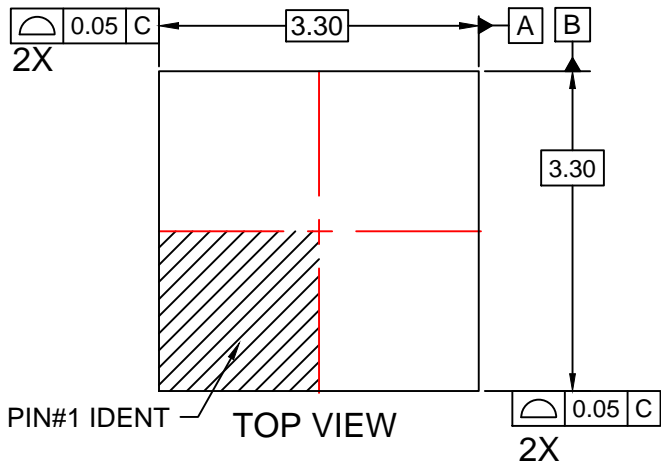


**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



**Figure 13. Junction-to-Case Transient Thermal Response Curve**



#### NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Srev3.



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