HM10S802

8 BIT 384 CHANNEL TFT-LCD SOURCE DRIVER

Mar. 6, 2001
Ver. 1.3

hynix Semiconductor

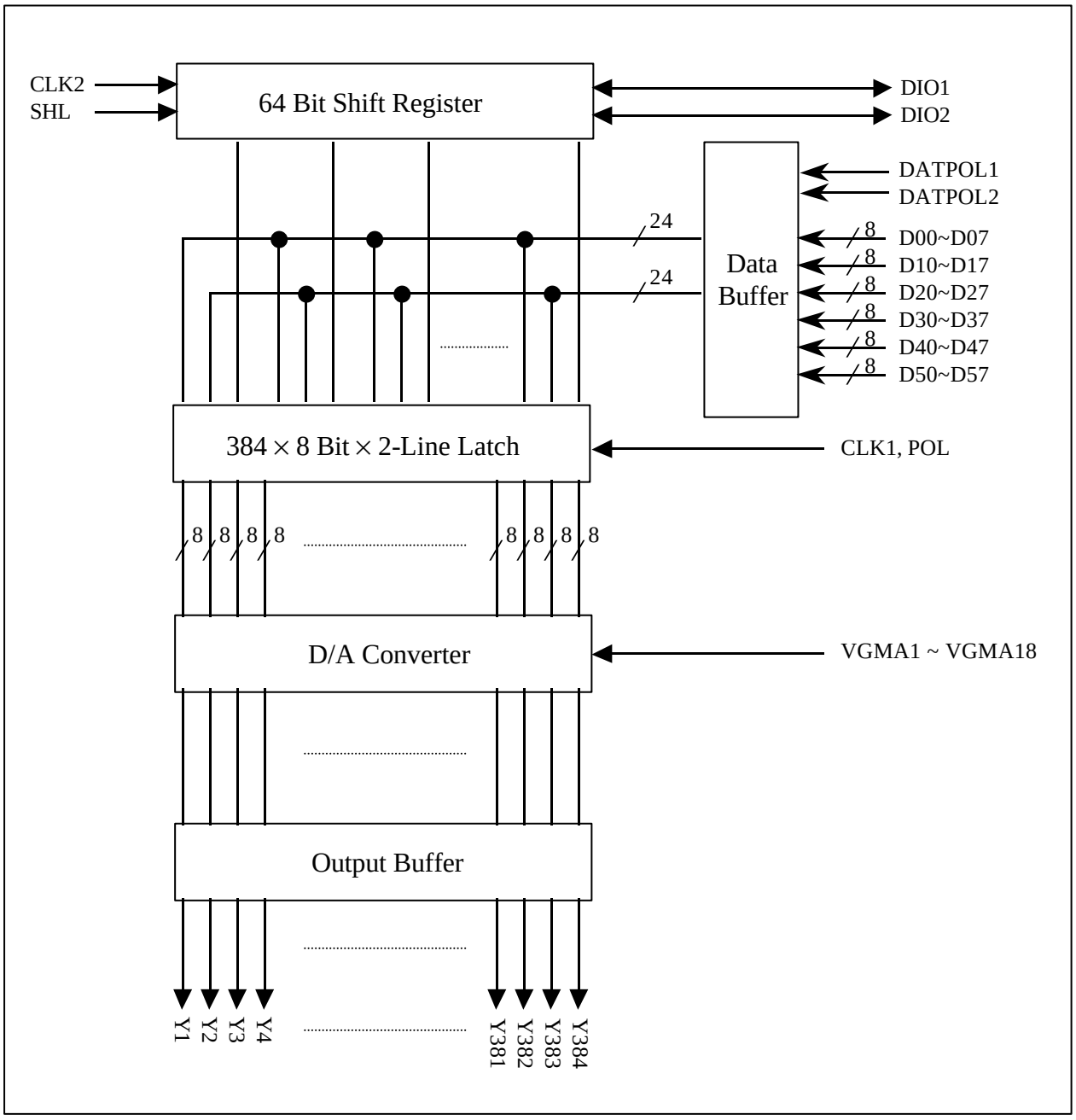
Description

The HM10S802 is a source driver for pixel inversion/N-line inversion LCD modules used in monitor or note PC applications. It accepts 8-bit × 6 dot digital data and provides direct drive, 512 voltages, 384 outputs, and full 11.6 ~ 14.6Vp-p dynamic range to drive 16,777,216 color TFT displays.

Features

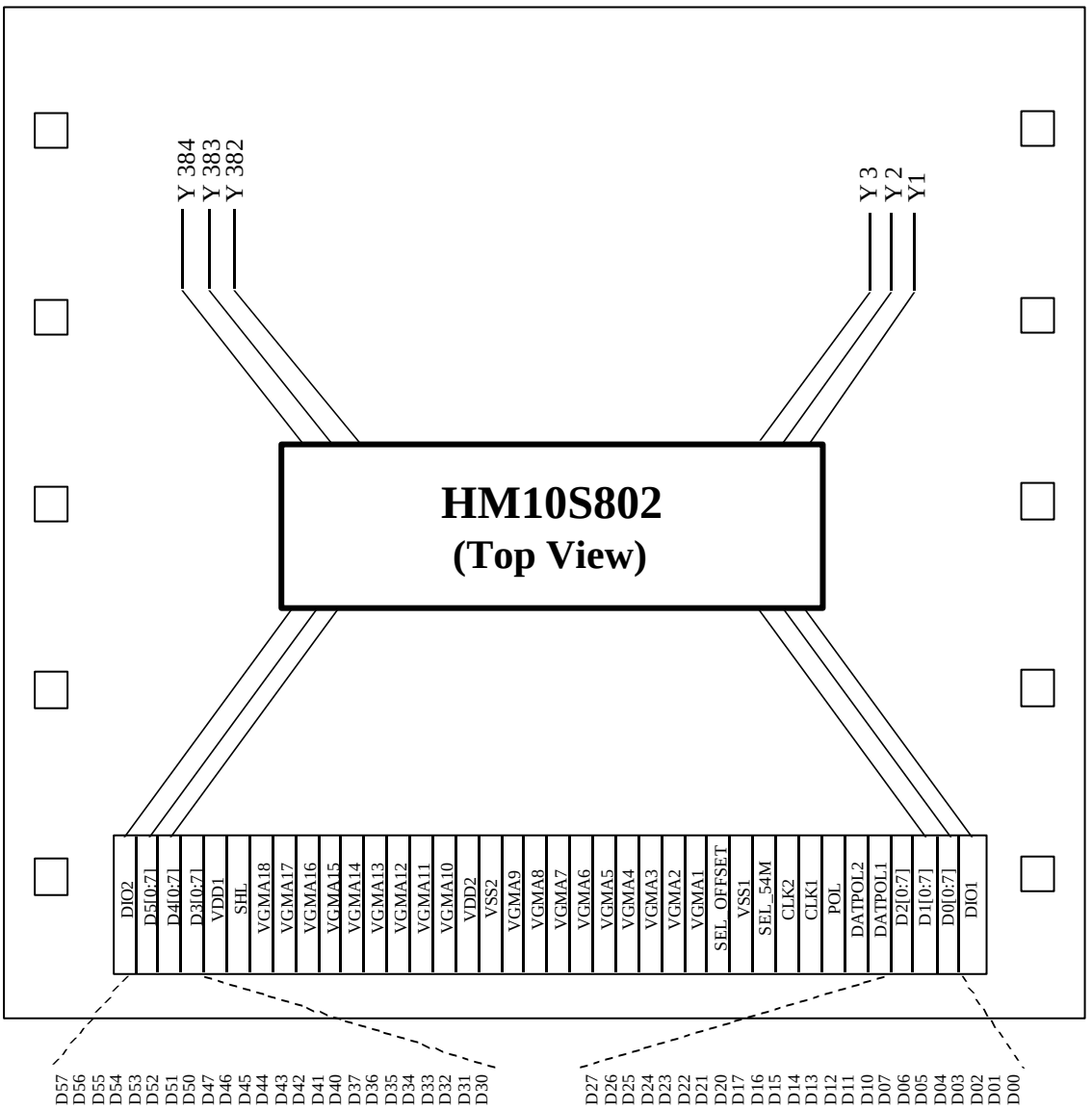
- TFT active matrix LCD source driver LSI
- 256 G/S is possible through 18 (9 by 2) reference voltages and D/A converter
- Both dot inversion display and N-line inversion display are possible
- CMOS level input
- Compatible with gamma-correction
- Input data inversion function (DATPOL1,2)
- Logic supply voltage : 2.5V ~ 3.6V
- LCD driver supply voltage : 12V ~ 15V
- Output dynamic range : 11.6 ~ 14.6V_{P-P}
- Output : 384 outputs
- Maximum operating frequency : 65MHz (internal data transmission rate at 2.5V operation)
- TCP (Tape Carrier Package)
- Adoption of SHL (shift direction selection) port for easy LCD wiring

Block Diagram



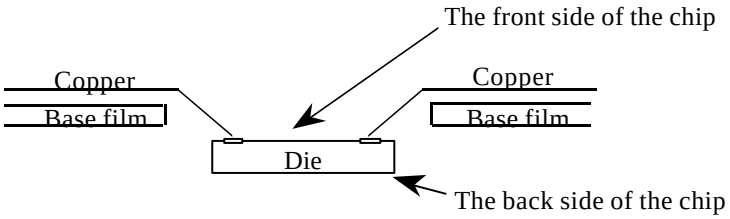
[Fig. 1] Block diagram of HM10S802

TCP Pin Configuration



[Fig. 2] TCP pin configuration of HM10S802

NOTICE : This is seen from the front side of the TCP.
Inner lead bonding direction is Face Up as shown below.
The number of dummy pads could be changed according to the situation.



Pin Description

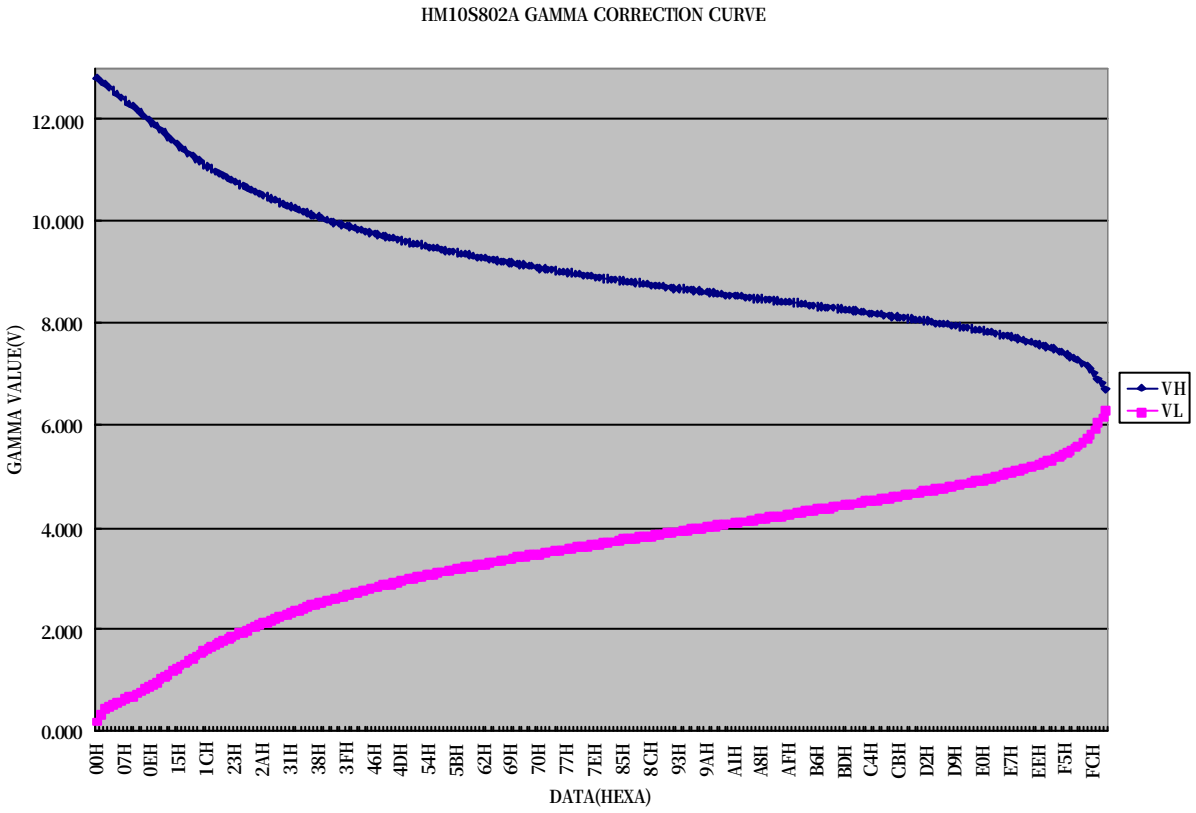
<table>
<tr><th>PIN NAME</th><th>INPUT / OUTPUT</th><th>FUNCTION</th></tr>
<tr><td>D0[0:7]
D1[0:7]
D2[0:7]
D3[0:7]
D4[0:7]
D5[0:7]</td><td>Input</td><td>R,G,B 8bit digital video signals
Dx0 : LSB, Dx7 : MSB
Data inputs which select one of 256 reference voltages
(Refer to Timing Diagram 2)</td></tr>
<tr><td>DIO1
DIO2</td><td>Input / Output</td><td>Data latch enable.
Start pulse input port of internal shift register
[Table 1] Relation between SHL and DIOx
<table>
<tr><th></th><th>SHL = H</th><th>SHL = L</th></tr>
<tr><td>DIO1</td><td>Right shift input</td><td>Left shift output</td></tr>
<tr><td>DIO2</td><td>Right shift output</td><td>Left shift input</td></tr>
</table></td></tr>
<tr><td>SHL</td><td>Input</td><td>Shift direction pin
SHL = H : Right shift, Y1 → Y384
SHL = L : Left shift, Y384 → Y1</td></tr>
<tr><td>CLK2</td><td>Input</td><td>Data clock pin
Data(Dx[0:7]), CLK1 and DIOx inputs are latched on the rising edge of this clock.</td></tr>
<tr><td>VDD2
VDD1
VSS2
VSS1</td><td>Input</td><td>Analog block voltage source : typically 13Volts above VSS2.
Digital block voltage source : typically 3.3Volts above VSS1.
Analog block reference voltage, typically 0Volts.
Digital block reference voltage, typically 0Volts.</td></tr>
<tr><td>VGMA1
~
VGMA18</td><td>Input</td><td>Input the gamma corrected power supplies from external source.
VGMA1 : The highest voltage in high voltage region
VGMA9 : The lowest voltage in high voltage region
VGMA10 : The highest voltage in low voltage region
VGMA18 : The lowest voltage in low voltage region
VDD2 > VGMA1 > VGMA2 …. > VGMA17 > VGMA18 > VSS2
Keep gray-scale power supply unchanged during the gray-scale voltage output.</td></tr>
<tr><td>CLK1</td><td>Input</td><td>Data transfer pin
On the rising edge of this input, the latched data are transferred to D/A Converter / Output buffer and after ‘ tpdDZ’ from rising edge of this input, the acquired analog voltages are driven to the outputs.(see page 21)</td></tr>
</table>

<table>
<tr><th>PIN NAME</th><th>INPUT / OUTPUT</th><th>FUNCTION</th></tr>
<tr><td>POL</td><td>Input</td><td>Polarity control pin.
This input pin is set to a logic high or a logic low state and selects the output polarity as shown below.
The sampling of this input begins with the rising edge of the CLK1 signal.

[Table 2] Relation between POL and output polarity
<table><tr><th>POL</th><th>Y_{2N-1}</th><th>Y_{2N}</th></tr><tr><td>L</td><td>VGMA1 to VGMA9</td><td>VGMA10 to VGMA18</td></tr><tr><td>H</td><td>VGMA10 to VGMA18</td><td>VGMA1 to VGMA9</td></tr></table>Y_{2N-1} : Odd number outputs
Y_{2N} : Even number outputs</td></tr>
<tr><td>DATPOL1
DATPOL2</td><td>Input</td><td>DATPOL1,2 = L : Display data are not inverted.
DATPOL1 = H : Display data of D0[0:7] ~ D2[0:7] are inverted
DATPOL2 = H : Display data of D3[0:7] ~ D5[0:7] are inverted</td></tr>
<tr><td>Y1 ~ Y384</td><td>Output</td><td>The D/A converted 256 gray-scale analog voltage is output.
(Refer to Timing Diagram 2)</td></tr>
<tr><td>SEL_54M</td><td>Input
(pull-up)</td><td>Selects high frequency / low frequency operation mode
fCLK2 of 54MHz operation mode is default
Pull-down(fCLK2 of 27MHz operation mode) can be used by TCP option (Rpu = 100kΩ)</td></tr>
<tr><td>SEL_
OFFSET</td><td>Input
(pull-up)</td><td>Selects offset cancellation timing signal generation method
Timing signal generation from timer is default
Pull-down(timing signal generation from counter) can be used by TCP option (Rpu = 100kΩ)</td></tr>
</table>

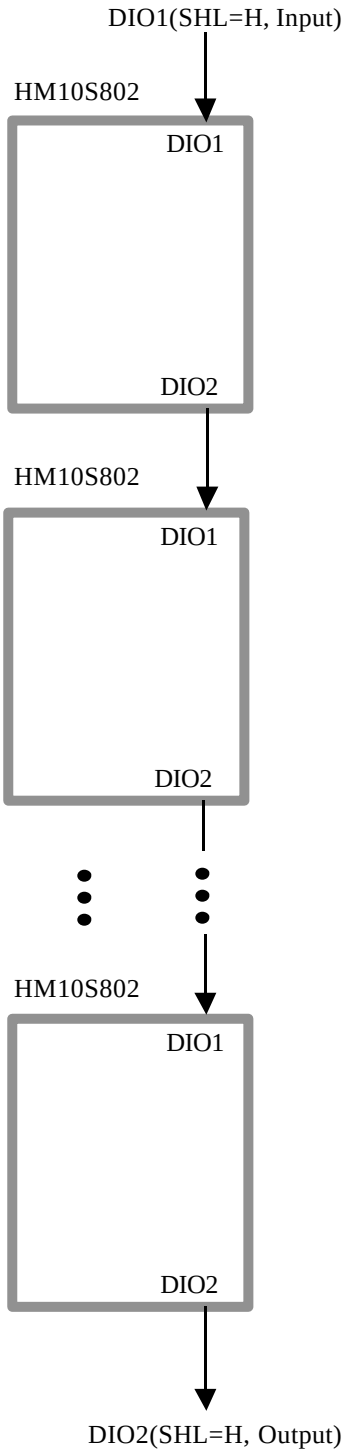
Device Description

The HM10S802 provides a full dynamic range of (VDD2-0.4)Vp-p from VDD2 supplies on 384 outputs. Full range output drive allows direct drive of TFT LCD displays, eliminating the need for Vcom or supply modulation electronics. This feature significantly reduces power consumption and component count.
In addition, the HM10S802 supports both pixel inversion and N-line inversion. Outputs are supported with individual high drive, high slew operational amplifier style buffers. The internal bi-directional shift registers allow to use in single bank full motion video. A total of 512 voltages can be output for an active matrix display with variable increments between each voltage as shown below.



[Fig. 3] HM10S802 Gamma correction curve

Digital data inputs to the chip are used to select one of the 512 voltages for driving an individual output. To implement variations of the existing characteristic curve, 18 external D/A voltage taps, 9 in the lower region and 9 in the higher region, are provided to allow the user to force voltages on several points in the D/A resistor string.



XGA system : 8 drivers, SXGA system : 10 drivers

[Fig. 4] Output driver control inputs

Relationship between input data and output voltage value

DATAH	V node	VH	PIN	R (HIGH)	VL	PIN	R (LOW)
00H	255	12.800	VGMA1	0.00	0.200	VGMA18	0.00
01H	254	12.742	VGMA2	114.60	0.334	VGMA17	262.70
02H	253	12.683		114.60	0.467		262.70
03H	252	12.620		125.10	0.498		61.80
04H	251	12.556		125.10	0.530		61.80
05H	250	12.493		124.30	0.564		67.30
06H	249	12.430		124.30	0.598		67.30
07H	248	12.368		121.90	0.635		71.60
08H	247	12.306		121.90	0.671		71.60
09H	246	12.245		120.90	0.710		76.20
0AH	245	12.183		120.90	0.749		76.20
0BH	244	12.122		119.90	0.789		80.30
0CH	243	12.061		119.90	0.830		80.30
0DH	242	11.999		122.90	0.874		86.80
0EH	241	11.936		122.90	0.918		86.80
0FH	240	11.868		134.60	0.969		99.80
10H	239	11.799		134.60	1.020		99.80
11H	238	11.730		136.00	1.073		105.30
12H	237	11.661		136.00	1.127		105.30
13H	236	11.593		133.20	1.181		106.80
14H	235	11.526		133.20	1.236		106.80
15H	234	11.463		123.90	1.288		102.20
16H	233	11.400		123.90	1.339		102.20
17H	232	11.341		114.80	1.389		96.70
18H	231	11.283		114.80	1.438		96.70
19H	230	11.228		107.90	1.485		92.50
1AH	229	11.173		107.90	1.532		92.50
1BH	228	11.123		99.60	1.576		86.60
1CH	227	11.072		99.60	1.620		86.60
1DH	226	11.025		91.90	1.661		80.70
1EH	225	10.979		91.90	1.702		80.70
1FH	224	10.935	VGMA3	86.40	1.741	VGMA16	76.70
20H	223	10.891		86.40	1.780		76.70
21H	222	10.849		82.20	1.817		73.40
22H	221	10.807		82.20	1.855		73.40
23H	220	10.767		78.40	1.890		70.60
24H	219	10.728		78.40	1.926		70.60
25H	218	10.689		75.20	1.961		68.00
26H	217	10.651		75.20	1.995		68.00
27H	216	10.614		72.20	2.029		65.70
28H	215	10.578		72.20	2.062		65.70
29H	214	10.543		68.90	2.094		63.00
2AH	213	10.508		68.90	2.126		63.00
2BH	212	10.474		66.60	2.157		61.10
2CH	211	10.440		66.60	2.188		61.10
2DH	210	10.407		64.30	2.219		59.30
2EH	209	10.375		64.30	2.249		59.30
2FH	208	10.343		62.60	2.278		57.90
30H	207	10.311		62.60	2.308		57.90
31H	206	10.280		60.60	2.336		56.20
32H	205	10.249		60.60	2.365		56.20
33H	204	10.220		57.70	2.392		53.70
34H	203	10.191		57.70	2.419		53.70
35H	202	10.163		55.10	2.445		51.40
36H	201	10.135		55.10	2.472		51.40
37H	200	10.108		52.80	2.497		49.40
38H	199	10.081		52.80	2.522		49.40
39H	198	10.055		50.70	2.546		47.60
3AH	197	10.029		50.70	2.570		47.60
3BH	196	10.005		48.70	2.593		45.80
3CH	195	9.980		48.70	2.617		45.80
3DH	194	9.956		46.90	2.639		44.30
3EH	193	9.932		46.90	2.662		44.30
3FH	192	9.909	VGMA4	45.30	2.684	VGMA15	42.80
40H	191	9.886		45.30	2.705		42.80
41H	190	9.864		43.70	2.726		41.50
42H	189	9.842		43.70	2.747		41.50
43H	188	9.820		42.30	2.768		40.30
44H	187	9.799		42.30	2.788		40.30
45H	186	9.778		41.00	2.808		39.10
46H	185	9.757		41.00	2.828		39.10
47H	184	9.737		39.80	2.848		38.10
48H	183	9.717		39.80	2.867		38.10
49H	182	9.697		38.60	2.886		37.10
4AH	181	9.677		38.60	2.905		37.10
4BH	180	9.658		37.60	2.923		36.20

4CH	179	9.639		37.60	2.941		36.20
4DH	178	9.620		36.60	2.959		35.30
4EH	177	9.602		36.60	2.977		35.30
4FH	176	9.584		35.60	2.995		34.40
50H	175	9.566		35.60	3.012		34.50
51H	174	9.548		34.70	3.029		33.70
52H	173	9.530		34.70	3.047		33.70
53H	172	9.513		33.90	3.063		33.00
54H	171	9.496		33.90	3.080		33.00
55H	170	9.479		33.10	3.097		32.30
56H	169	9.462		33.10	3.113		32.30
57H	168	9.446		32.30	3.129		31.70
58H	167	9.429		32.30	3.145		31.70
59H	166	9.413		31.60	3.161		31.10
5AH	165	9.397		31.60	3.177		31.10
5BH	164	9.382		30.90	3.192		30.60
5CH	163	9.366		30.90	3.208		30.60
5DH	162	9.351		30.30	3.223		30.00
5EH	161	9.335		30.30	3.238		30.00
5FH	160	9.320		29.70	3.253		29.50
60H	159	9.305		29.70	3.268		29.50
61H	158	9.290		29.10	3.283		29.10
62H	157	9.275		29.10	3.298		29.10
63H	156	9.261		28.50	3.313		28.60
64H	155	9.246		28.50	3.327		28.60
65H	154	9.232		28.00	3.341		28.20
66H	153	9.218		28.00	3.356		28.20
67H	152	9.204		27.50	3.370		27.80
68H	151	9.190		27.50	3.384		27.80
69H	150	9.176		27.00	3.398		27.40
6AH	149	9.162		27.00	3.412		27.40
6BH	148	9.149		26.50	3.426		27.10
6CH	147	9.136		26.50	3.439		27.10
6DH	146	9.122		26.10	3.453		26.70
6EH	145	9.109		26.10	3.467		26.70
6FH	144	9.096		25.70	3.480		26.40
70H	143	9.083		25.70	3.493		26.40
71H	142	9.070		25.30	3.507		26.10
72H	141	9.057		25.30	3.520		26.10
73H	140	9.044		24.90	3.533		25.80
74H	139	9.032		24.90	3.546		25.80
75H	138	9.019		24.50	3.559		25.60
76H	137	9.007		24.50	3.572		25.60
77H	136	8.995		24.10	3.585		25.30
78H	135	8.982		24.10	3.598		25.30
79H	134	8.970		23.80	3.611		25.10
7AH	133	8.958		23.80	3.623		25.10
7BH	132	8.946		23.50	3.636		24.90
7CH	131	8.934		23.50	3.649		24.90
7DH	130	8.923		23.10	3.661		24.70
7EH	129	8.911		23.10	3.674		24.70
7FH	128	8.899	VGMA5	22.80	3.686	VGMA14	24.50
80H	127	8.888		22.80	3.699		24.50
81H	126	8.876		22.50	3.711		24.30
82H	125	8.865		22.50	3.724		24.30
83H	124	8.854		22.20	3.736		24.20
84H	123	8.842		22.20	3.748		24.20
85H	122	8.831		22.00	3.760		24.00
86H	121	8.820		22.00	3.773		24.00
87H	120	8.809		21.70	3.785		23.90
88H	119	8.798		21.70	3.797		23.90
89H	118	8.787		21.40	3.809		23.80
8AH	117	8.776		21.40	3.821		23.80
8BH	116	8.765		21.20	3.833		23.70
8CH	115	8.754		21.20	3.845		23.70
8DH	114	8.744		21.00	3.857		23.60
8EH	113	8.733		21.00	3.869		23.60
8FH	112	8.723		20.70	3.881		23.50
90H	111	8.712		20.70	3.893		23.50
91H	110	8.702		20.50	3.905		23.50
92H	109	8.691		20.50	3.917		23.40
93H	108	8.681		20.30	3.929		23.40
94H	107	8.671		20.30	3.941		23.40
95H	106	8.660		20.10	3.952		23.30
96H	105	8.650		20.10	3.964		23.30
97H	104	8.640		19.90	3.976		23.30
98H	103	8.630		19.90	3.988		23.30

99H	102	8.620		19.70	4.000		23.30
9AH	101	8.610		19.70	4.012		23.30
9BH	100	8.600		19.50	4.024		23.30
9CH	99	8.590		19.50	4.035		23.30
9DH	98	8.580		19.40	4.047		23.30
9EH	97	8.570		19.40	4.059		23.30
9FH	96	8.561		19.20	4.071		23.30
A0H	95	8.551		19.20	4.083		23.30
A1H	94	8.541		19.00	4.095		23.30
A2H	93	8.532		19.00	4.106		23.30
A3H	92	8.522		19.00	4.118		23.40
A4H	91	8.512		18.90	4.130		23.40
A5H	90	8.503		18.70	4.142		23.40
A6H	89	8.493		18.70	4.154		23.40
A7H	88	8.484		18.60	4.166		23.50
A8H	87	8.474		18.60	4.178		23.50
A9H	86	8.465		18.40	4.190		23.60
AAH	85	8.456		18.40	4.202		23.60
ABH	84	8.446		18.30	4.214		23.70
ACH	83	8.437		18.30	4.226		23.70
ADH	82	8.428		18.20	4.238		24.00
AEH	81	8.419		18.20	4.250		24.00
AFH	80	8.409		18.00	4.263		25.50
B0H	79	8.400		18.00	4.276		25.50
B1H	78	8.390		20.00	4.289		25.30
B2H	77	8.380		20.00	4.302		25.30
B3H	76	8.370		20.00	4.315		25.30
B4H	75	8.360		20.00	4.328		25.30
B5H	74	8.349		20.00	4.341		25.30
B6H	73	8.339		20.00	4.353		25.30
B7H	72	8.329		20.10	4.366		25.30
B8H	71	8.319		20.10	4.379		25.30
B9H	70	8.309		20.10	4.392		25.30
BAH	69	8.298		20.10	4.405		25.30
BBH	68	8.288		20.20	4.418		25.30
BCH	67	8.278		20.20	4.431		25.30
BDH	66	8.267		20.40	4.444		25.30
BEH	65	8.257		20.40	4.456		25.30
BFH	64	8.247	VGMA6	20.50	4.469	VGMA13	25.30
C0H	63	8.236		20.50	4.482		25.30
C1H	62	8.226		20.70	4.495		25.30
C2H	61	8.215		20.70	4.508		25.30
C3H	60	8.205		20.90	4.521		25.30
C4H	59	8.194		20.90	4.534		25.30
C5H	58	8.183		21.10	4.547		25.60
C6H	57	8.172		21.10	4.560		25.60
C7H	56	8.162		21.40	4.573		25.80
C8H	55	8.151		21.40	4.586		25.80
C9H	54	8.140		21.70	4.599		26.10
CAH	53	8.129		21.70	4.612		26.10
CBH	52	8.117		22.10	4.626		26.40
CCH	51	8		22.10 6	4.639		26.40
CDH	50	8.095		22.50	4.653		26.80
CEH	49	8.083		22.50	4.666		26.80
CFH	48	8.072		22.90	4.680		27.30
D0H	47	8.060		22.90	4.694		27.30
D1H	46	8.048		23.40	4.708		27.80
D2H	45	8.036		23.40	4.722		27.80
D3H	44	8.024		24.00	4.737		28.40
D4H	43	8.012		24.00	4.751		28.40
D5H	42	7.999		24.60	4.766		29.10
D6H	41	7.987		24.60	4.781		29.10
D7H	40	7.974		25.30	4.796		30.00
D8H	39	7.961		25.30	4.811		30.00
D9H	38	7.948		26.10	4.827		30.70
DAH	37	7.935		26.10	4.843		30.70
DBH	36	7.921		27.00	4.858		30.70
DCH	35	7.907		27.00	4.874		30.70
DDH	34	7.893		28.00	4.890		32.80
DEH	33	7.879		28.00	4.907		32.80
DFH	32	7.864	VGMA7	29.10	4.925	VGMA12	34.10
E0H	31	7.849		29.10	4.942		34.10
E1H	30	7.834		30.40	4.960		35.60
E2H	29	7.818		30.40	4.978		35.60
E3H	28	7.802		31.90	4.997		37.20
E4H	27	7.786		31.90	5.016		37.20
E5H	26	7.769		33.60	5.036		39.20

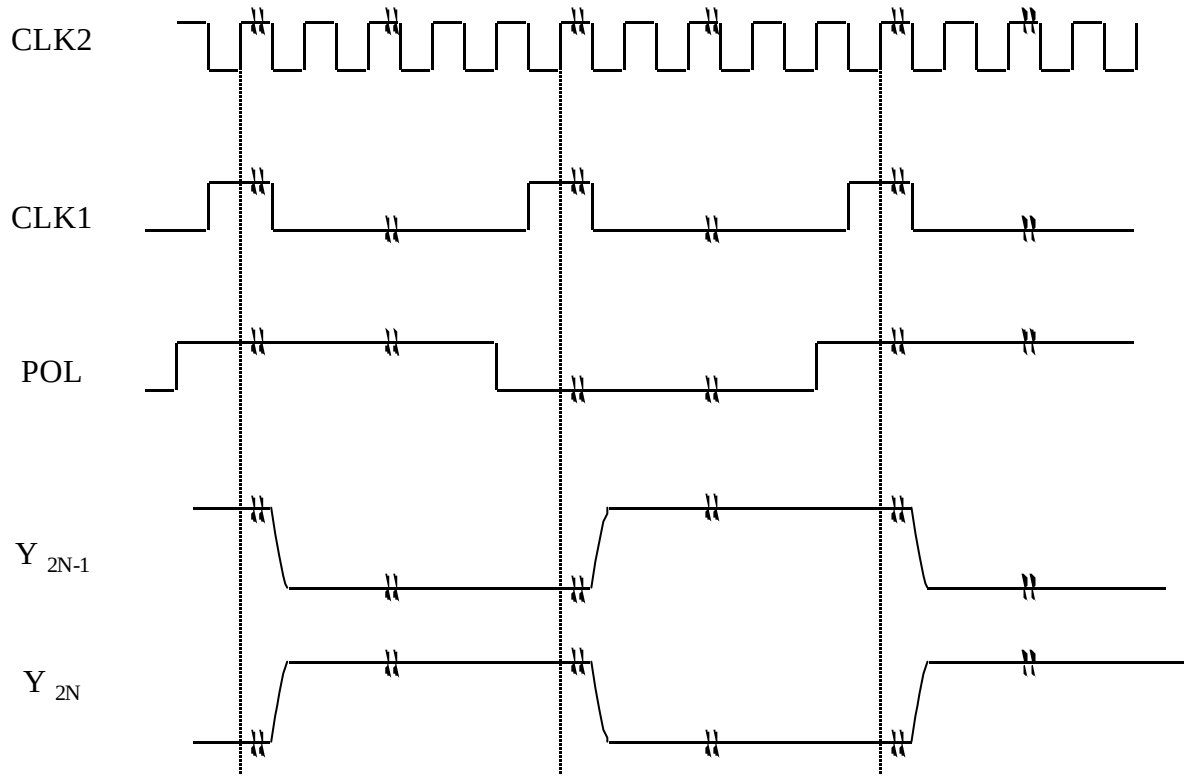
E6H	25	7.752		33.60	5.056		39.20
E7H	24	7.733		35.60	5.077		41.50
E8H	23	7.715		35.60	5.098		41.50
E9H	22	7.696		38.00	5.120		44.20
EAH	21	7.677		38.00	5.143		44.20
EBH	20	7.656		40.80	5.167		47.40
ECH	19	7.635		40.80	5.191		47.40
EDH	18	7.613		44.20	5.217		51.40
EEH	17	7.590		44.20	5.243		51.40
EFH	16	7.566		48.40	5.272		56.30
F0H	15	7.541		48.40	5.301		56.30
F1H	14	7.514		53.70	5.332		62.40
F2H	13	7.487		53.70	5.364		62.40
F3H	12	7.456		60.60	5.401		72.40
F4H	11	7.425		60.60	5.438		72.40
F5H	10	7.389		69.90	5.480		83.30
F6H	9	7.354		69.90	5.522		83.30
F7H	8	7.312		83.10	5.572		97.90
F8H	7	7.269		83.10	5.622		97.90
F9H	6	7.217		103.30	5.684		121.90
FAH	5	7.164		103.30	5.746		121.90
FBH	4	7.094		138.00	5.828		162.70
FCH	3	7.024		138.00	5.911		162.70
FDH	2	6.916		212.50	6.041		255.00
FEH	1	6.808	VGMA8	212.50	6.170	VGMA11	255.00
FFH	0	6.700	VGMA9	212.50	6.300	VGMA10	255.00

Notes:

This is the sample reationship between input data and output voltage value, so can be changed according to customer' s request.

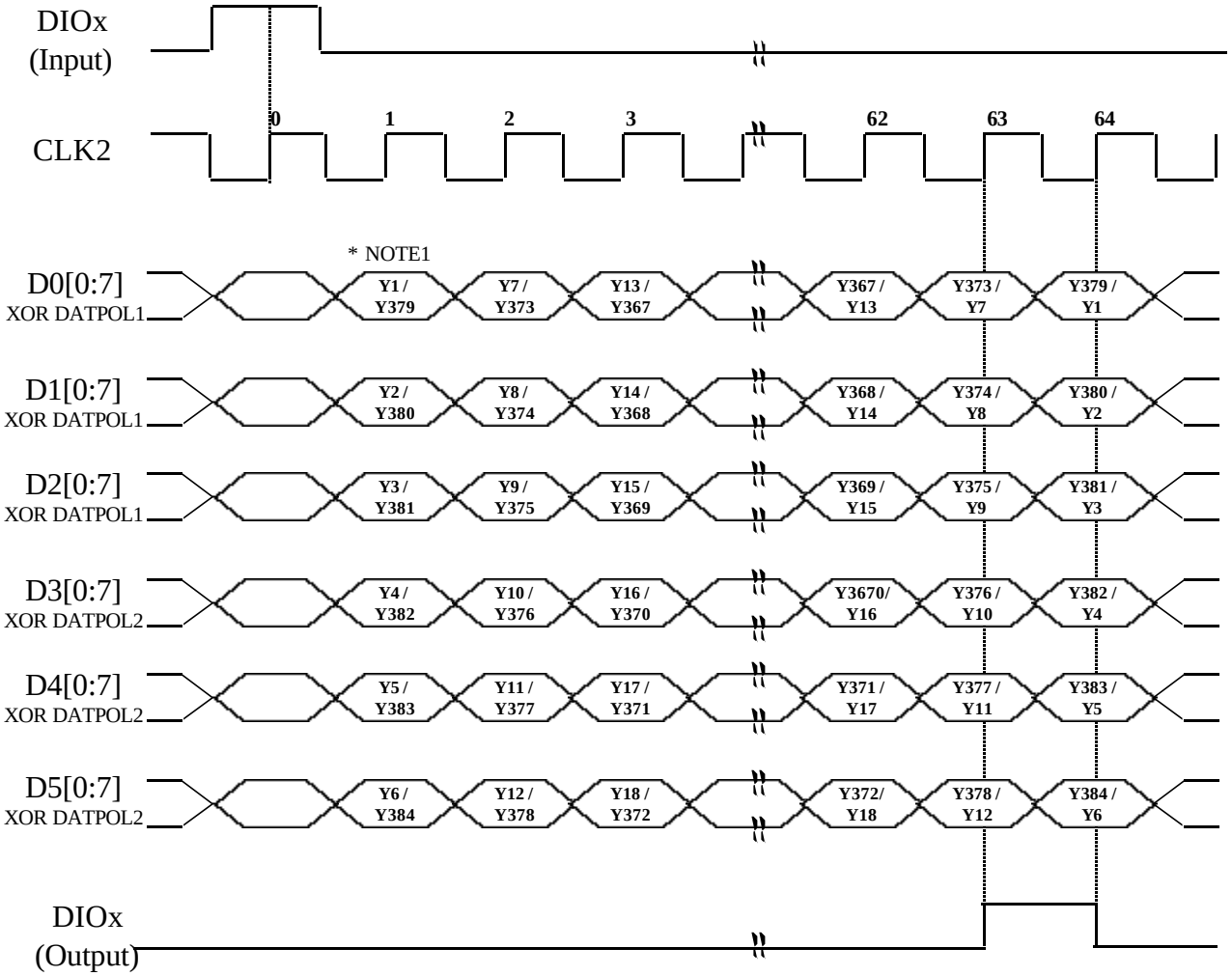
Timing Diagram 1

- CLK1, POL, and Output waveforms



Timing Diagram 2

- DIOx and Data latch sequence

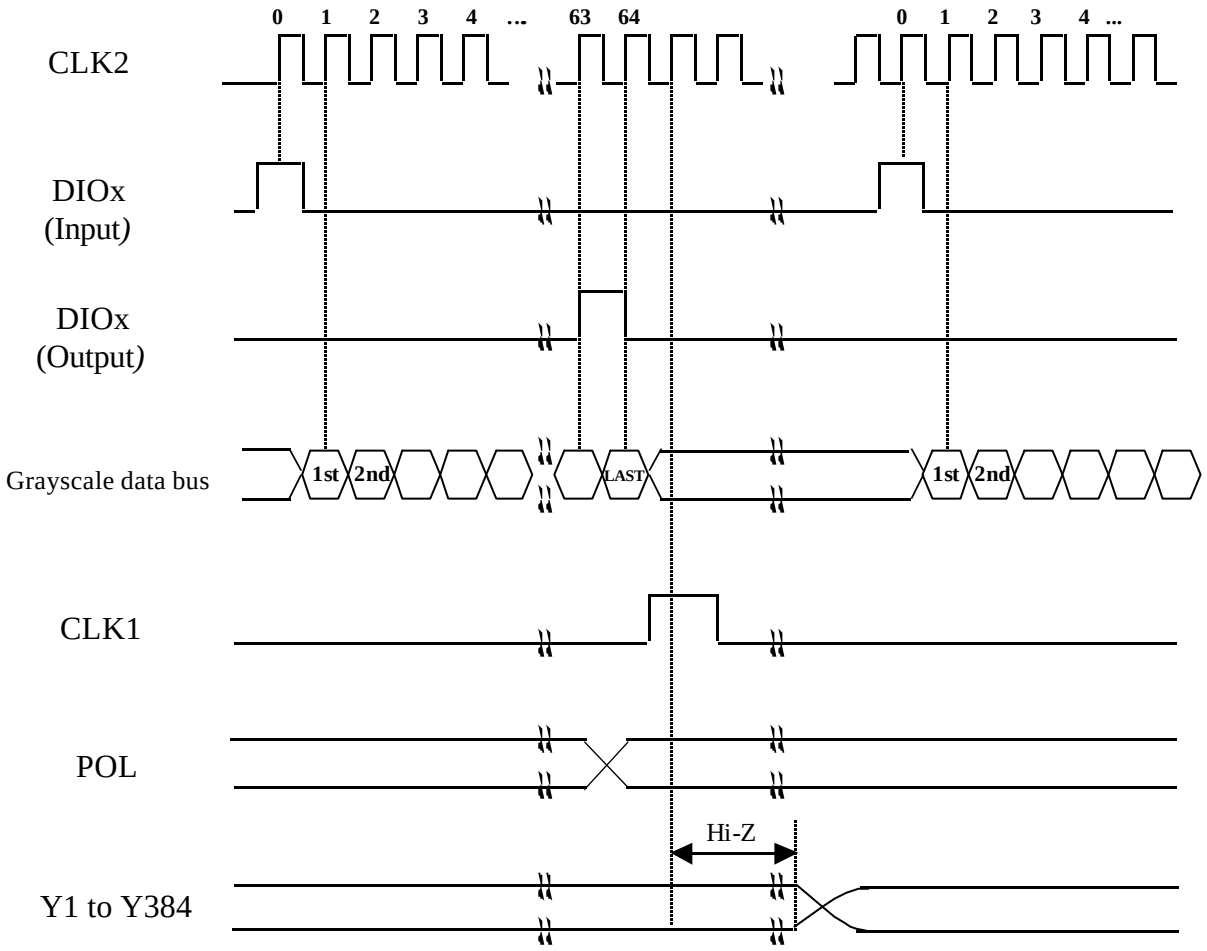


- Relationship between Input Data Value and Output Voltage

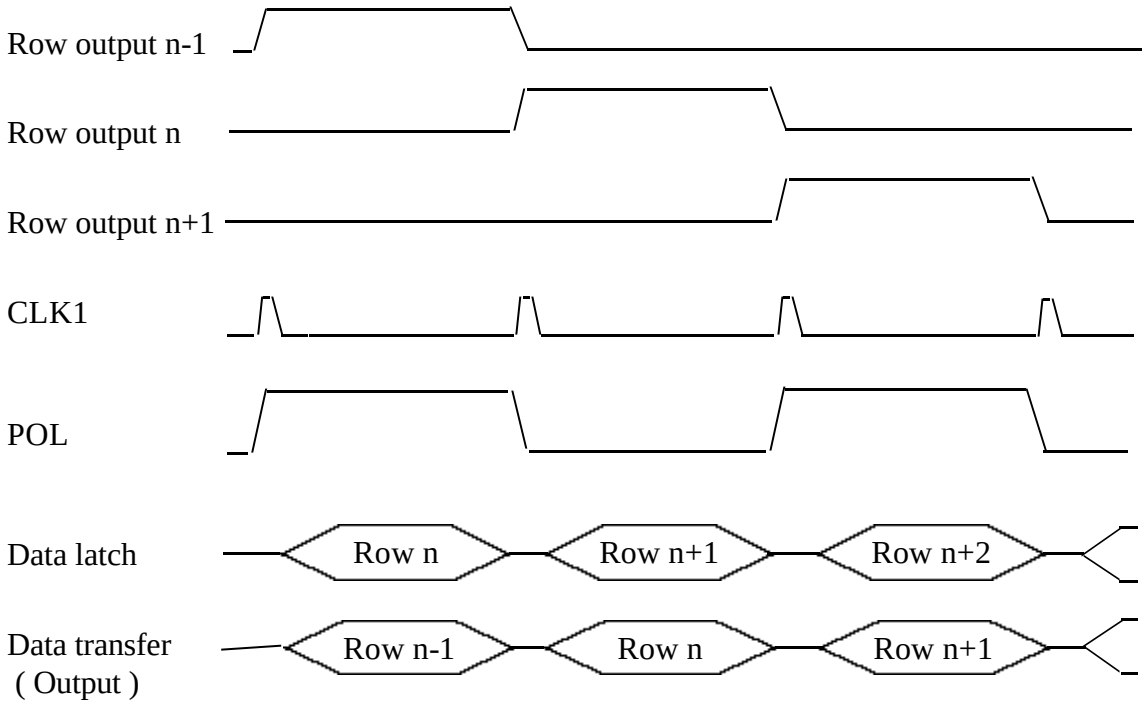
Output	Y1	Y2	Y3	---	Y382	Y383	Y384
SHL=H	First			→	Last		
SHL=L	Last			←	First		
Data	D00~D07	D10~D17	D20~D27	---	D30~D37	D40~D47	D50~D57

Timing Diagram 3

- DIOx and CLK1 operations



Timing Diagram 4



Absolute Maximum Ratings

[Table 3] Absolute Maximum Ratings (VSS1 = VSS2 = 0V)

Parameter	Symbol	Ratings	Unit
Logic supply voltage	VDD1	-0.3 ~ +6.0	V
Driver supply voltage	VDD2	-0.3 ~ +16.0	V
Input voltage	VGMA1 ~ 18	-0.3 ~ VDD2+0.3	V
	Others	-0.3 ~ VDD1+0.3	
Output voltage	Y1 ~ Y384	-0.3 ~ VDD2+0.3	V
	DIO1,2	-0.3 ~ VDD1+0.3	
Operating temperature	Top	-25 ~ +75	℃
Storage temperature	Tstg	-55 ~ +125	℃

CAUTIONS:

If LSIs are stressed beyond those listed above "absolute maximum ratings", they may be permanently destroyed. These are stress ratings only, and functional operation of the devices at these or any other condition beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Power On sequence : VDD1 is first and VDD2, GMAx and control signal input are next irrespective of their order

Power Off sequence : reverse order of Power On sequence

Recommended Operating Conditions

[Table 4] Recommended Operating Conditions (Top = -25 ~ +75 ℃, VSS1 = VSS2 = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic supply voltage	VDD1	2.5	3.0	3.6	V
Driver supply voltage	VDD2	12	13	15	V
Gamma corrected voltage	VGMA1 ~ 9	0.5VDD2	-	VDD2 - 0.2	V
	VGMA10 ~ 18	VSS2 + 0.2	-	0.5VDD2	
Driver part output voltage	Vyo	VSS2 + 0.2	-	VDD2 - 0.2	V
Maximum clock frequency	fmax	VDD1 = 2.5V		65	MHz

DC Characteristics

[Table 5] DC Characteristics (Top = -25 ~ +75 ℃, VDD1 = 2.5 ~ 3.6V, VDD2 = 12 ~ 15V, VSS1 = VSS2 = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH	-	0.7VDD1	-	VDD1	V
Low level input voltage	VIL	-	0	-	0.3VDD1	V
Input leakage current	IL	-	-10	-	10	uA
Pull-down input current	IIL	SEL_54M pin	-	-	50	uA
High level output voltage	VOH	-	VDD1-0.5	-	-	V
Low level output voltage	VOL	-	-	-	0.5	V
Driver output current	IVOH	VDD2=13V Vx=6.5V, Vyo=12.8V (1)	-	-2	- -	mA
	IVOL	VDD2=13V Vx=6.5V, Vyo=0.2V (1)	-	2	-	mA
Output voltage deviation	ΔV_O (2)	VSS2+0.2V ~ VDD2-1.5V	-	±7	±15	mV
		VDD2-1.5V ~ VDD2-0.2V	-	±10	±20	mV
Output RMS voltage deviation	dVrms (3)	Input data : 00H ~ FFH	-(ΔV + 2)	-	ΔV + 2	mV
Output voltage range	Vyo	Input data : 00H ~ FFH	VSS2+0.2	-	VDD2-0.2	V
Logic part dynamic current	IDD1 (4)	-	-	1.34	2.94	mA
Driver part dynamic current	IDD2 (5)	-	-	20.1	29.5	mA

Notes:

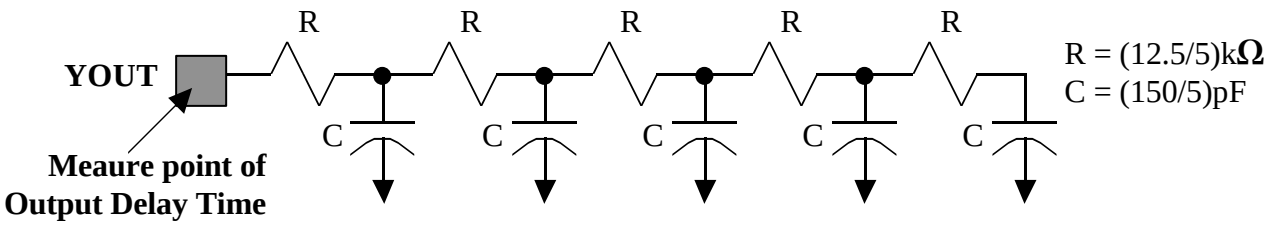
1. Vyo is the output voltage of analog output pins Y1 to Y384
   Vx is the voltage applied to analog output pins Y1 to Y384
2. ΔV_O is the output to output and driver to driver relative offset error.
3. dVrms is the output to output and driver to driver peak to peak error.
   ΔV is the minimum code step size.
4. CLK1 period is defined to be 15.6us at fCLK2=54MHz (SXGA 60Hz), data toggle at every CLK2 (00H -> FFH -> 00H ..).
5. CLK1 period is defined to be 15.6us at fCLK2=54MHz (SXGA 60Hz), data pattern = 00000000, VGMA1=(VDD2 - 0.2)V, VGMA9=(VDD2/2 + 0.2)V, VGMA10=(VDD2/2 - 0.2)V, VGMA18=(VSS2 + 0.2)V, Load=12.5KΩ/150pF (refer to Fig. 5). This is equivalent to an all black display.

AC Characteristics

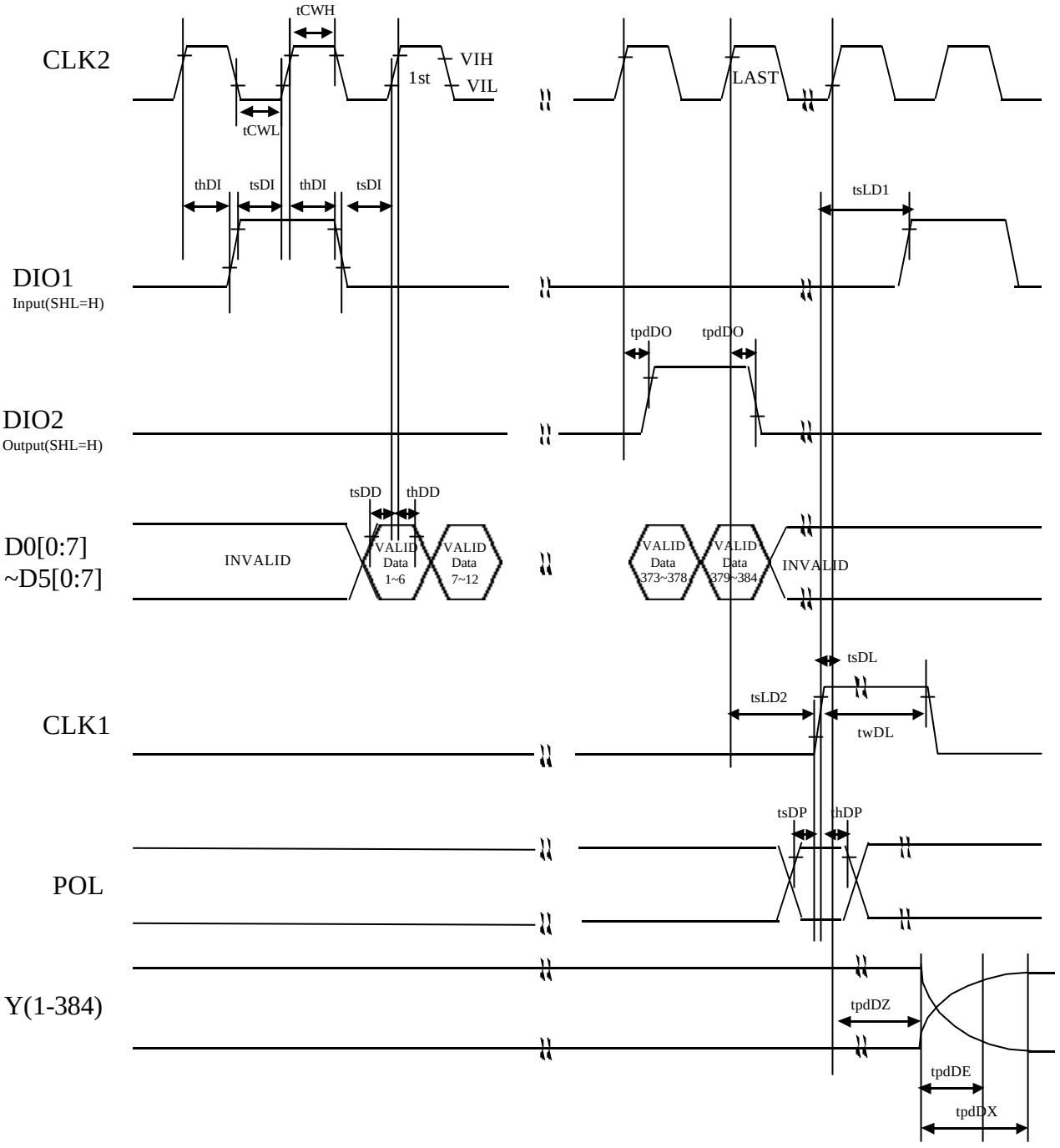
[Table 6] AC Characteristics (Top = -25 ~ +75 ℃, VDD1 = 2.5 ~ 3.6V, VDD2 = 12 ~ 15V, VSS1 = VSS2 = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data Clock Frequency (1)	fCLK2	–	27	54	65	MHz
CLK2 Pulse Width High	tCWH	–	4	–	–	ns
CLK2 Pulse Width Low	tCWL	–	4	–	–	ns
Enable Setup Time	tsDI	–	0	–	–	ns
Enable Hold Time	thDI	–	4	–	–	ns
Data(Dx[0:7], DATPOLx) Setup Time	tsDD	–	0	–	–	ns
Data(Dx[0:7], DATPOLx) Hold Time	thDD	–	4			ns
CLK1 (2) Setup time	tsDL	–	4	–	–	ns
CLK1 High Duration	twDL	–	1	–	–	us
CLK1 to Enable Input Duration	tsLD1	–	2	–	–	CLK2 period
CLK1 to Enable Output Duration	tsLD2	–	1	–	–	CLK2 period
POL Setup Time	tsDP	–	4	–	–	ns
POL Hold Time	thDP	–	4	–	–	ns
Enable Output Delay Time	tpdDO	Load=15pF	3.5	–	10	ns
Output High-Z Time	tpdDZ	–	–	1	–	us
Output Delay Time 1 (3)	tpdDE	–	–	–	4	us
Output Delay Time 2 (4)	tpdDX	–	–	–	8	us

Notes::
1. CLK2 rise / fall time = 2.0ns max. (10%~90%)
2. Does not need to be synchronous to clock.
3. Target output voltage × 0.9
4. Target output voltage ± ΔVO
5. Load condition of analog output pin is shown in [Fig 5].



[Fig. 5] Load conditions of analog output pin.
The values of R and C could be changed according to the situation.



[Fig. 6] Timing diagram for cascaded devices with free-running CLK2