- **Organization . . . 16 777 216 × 1**
- **Single 5-V Power Supply (10% Tolerance)**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
SMJ417100-60	60 ns	15 ns	30 ns	110 ns
SMJ417100-70	70 ns	18 ns	35 ns	130 ns
SMJ417100-80	80 ns	20 ns	40 ns	150 ns
SMJ417100-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 2048 Cycles Refresh in 32 ms**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **All Inputs, Outputs and Clocks are TTL Compatible**
- **Operating Free-Air Temperature Range – 55°C to 125°C**

description

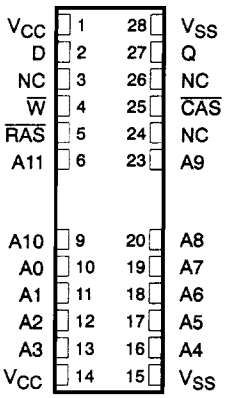
The SMJ417100 series are high-speed 16 777 216-bit dynamic random-access memories, organized as 16 777 216-bit words by one bit each. They employ EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns.

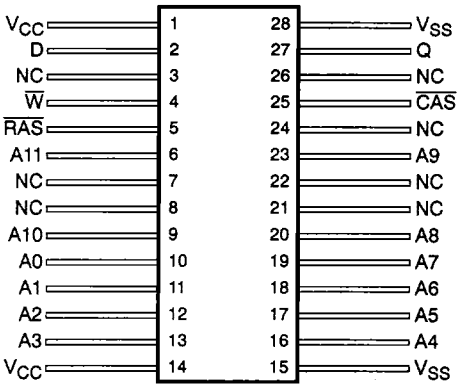
All inputs, outputs, and clocks, are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ417100 is offered in 450-mil 24/28-pin surface mount SOLCC (FNC suffix) and flatpack (HKB suffix) packages. The packages are characterized for operation from – 55°C to 125°C.

FNC PACKAGE†
(TOP VIEW)



HKB PACKAGE†
(TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Internal Connection
Q	Data Out
$\overline{RAS}$	Row-Address strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

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operation

enhanced page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by t_{RAS}, the maximum $\overline{RAS}$-low width.

The Column Address Buffers in this CMOS device are activated on the falling edge of $\overline{RAS}$. They act as a transparent or flow-through latch, while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses into these buffers and also serves as an output enable.

This feature allows the SMJ417100 to operate at a higher data bandwidth than conventional page-mode parts, since retrieval begins as soon as the column address is valid, rather than when $\overline{CAS}$ transitions low. The performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) and t_{RAC} have been satisfied. In the event that the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0–A11)

Twenty-four address bits are required to decode 1 of 16 777 216 storage cell locations. Twelve row-address bits are set on inputs A0 through A11 and latched during a normal access. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable $\overline{W}$ input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data-in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out (Q)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fan-out of two Series 54 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, or t_{CPA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output does not change, but retains the state just read.

refresh

A refresh operation must be performed at least once every thirty-two milliseconds to retain data. This can be achieved by strobing each of the 2048 rows (A0–A10). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at a high (inactive) level, thus conserving power since the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after the specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. Valid data is maintained at the output throughout the hidden refresh cycle. An internal refresh address provides the refresh address during hidden refresh.

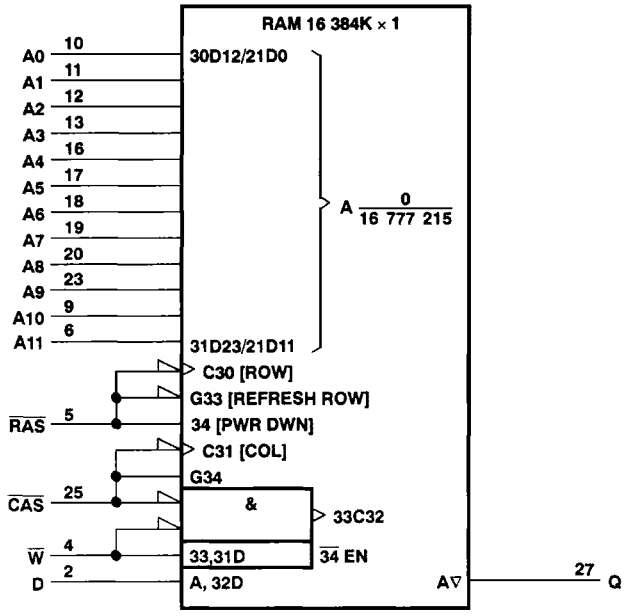
$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

power up

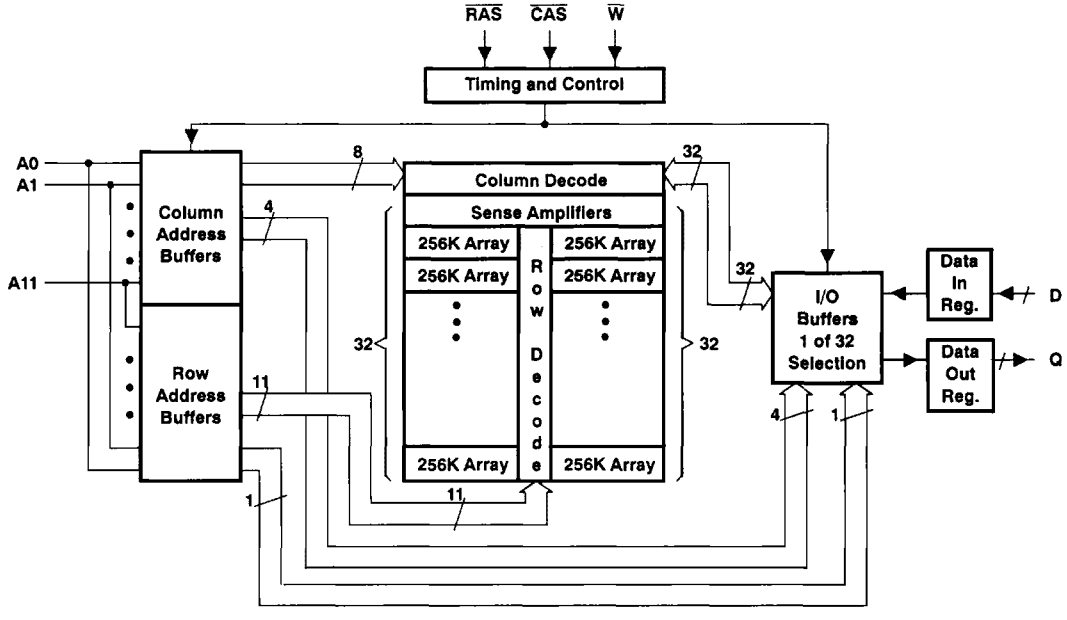
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin (see Note 1) . . . . . – 1 V to 7 V
Voltage on V_{CC} . . . . . – 1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . – 55°C to 125°C
Storage temperature range . . . . . – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ417100-60		SMJ417100-70		SMJ417100-80		SMJ417100-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)‡	V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)‡	V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		110		100		90		80	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		2		2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		1		1		1		1	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR)‡	$\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		110		100		90		80	mA
I_{CC4}	Average page current (see Note 4)‡	$\overline{RAS}$ low, $\overline{CAS}$ cycling		70		65		60		55	mA
I_{CC7}	Standby current output enable‡ (see Note 5)	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled		5		5		5		5	mA

‡ Minimum cycle, V_{CC} = 5.5 V.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.
5. Measured with indicated conditions following a normal read cycle.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			9	pF
$C_{i(D)}$	Input capacitance, data input			8	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			8	pF
$C_{i(W)}$	Input capacitance, write-enable input			8	pF
C_O	Output capacitance			14	pF

NOTE 6: Capacitance is sampled only at initial design and after any major change. Samples are tested at 0 V and 25° C with a 1 MHz signal applied to the pin under test. All other pins are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		SMJ417100-60		SMJ417100-70		SMJ417100-80		SMJ417100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 8)	0	15	0	18	0	20	0	25	ns

NOTES: 7. Valid data is presented at the output after all access times are satisfied but may go from a high-impedance state to an invalid data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

8. t_{OFF} is specified when the output is no longer dirven. The output is disabled by bringing $\overline{CAS}$ high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		SMJ417100-60		SMJ417100-70		SMJ417100-80		SMJ417100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 9)	110		130		150		180		ns
t_{RWC}	Read-write cycle time	130		153		175		210		ns
t_{PC}	Page-mode read or write cycle time (see Note 10)	40		45		50		55		ns
t_{PRWC}	Page-mode read-write cycle time	60		68		75		85		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 11)	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 11)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 12)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 13)	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		15		ns
t_{DH}	Data hold time (see Note 12)	10		15		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 14)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 14)	5		5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		15		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns

Continued next page.

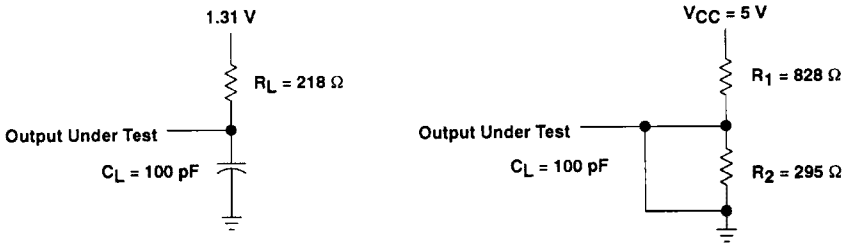
NOTES: 9. All cycle times assume t_T = 5 ns, referenced to V_{IH}(min) and V_{IL}(max).
10. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
11. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
12. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
13. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		SMJ417100-60		SMJ417100-70		SMJ417100-80		SMJ417100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	30		35		40		45		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	15		18		20		25		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 15)	15	30	15	35	15	40	15	55	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15)	20	45	20	52	20	60	20	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	60		70		80		100		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	35		40		45		50		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	35		40		45		50		ns
t_{REF}	Refresh time interval		32		32		32		32	ms

NOTE 15: The maximum value is specified only to assure access time.

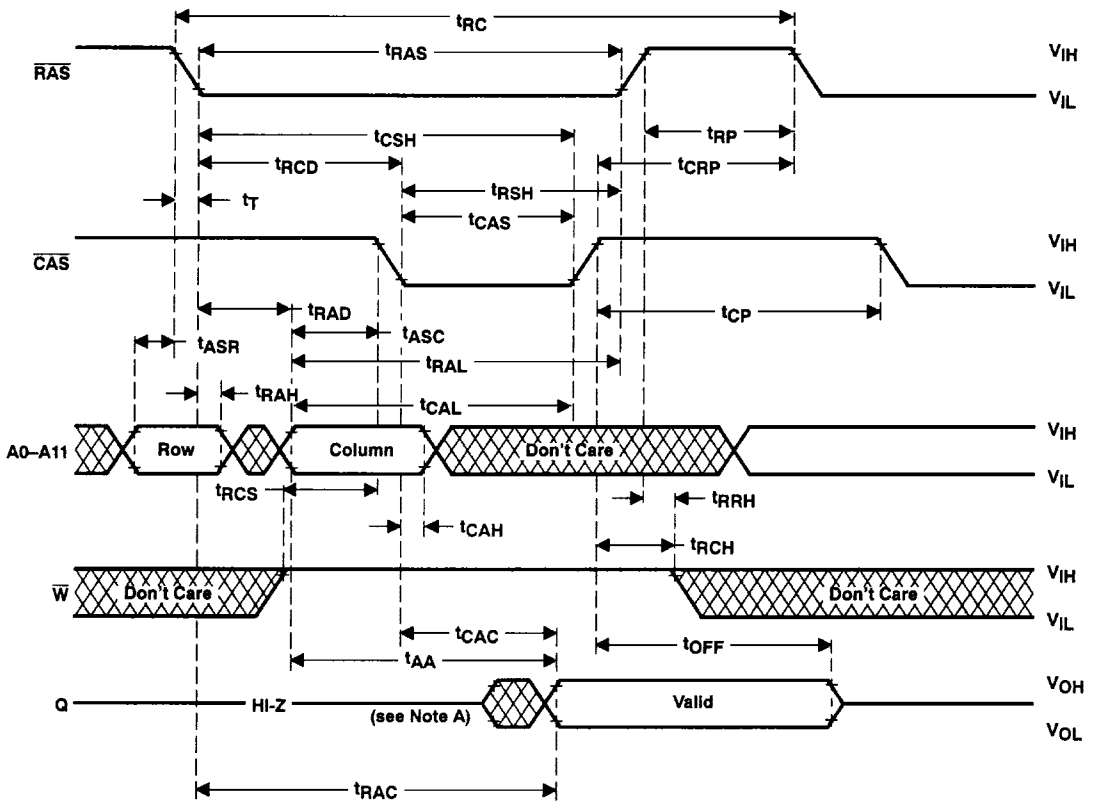
PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit (b) Alternate Load Circuit

Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

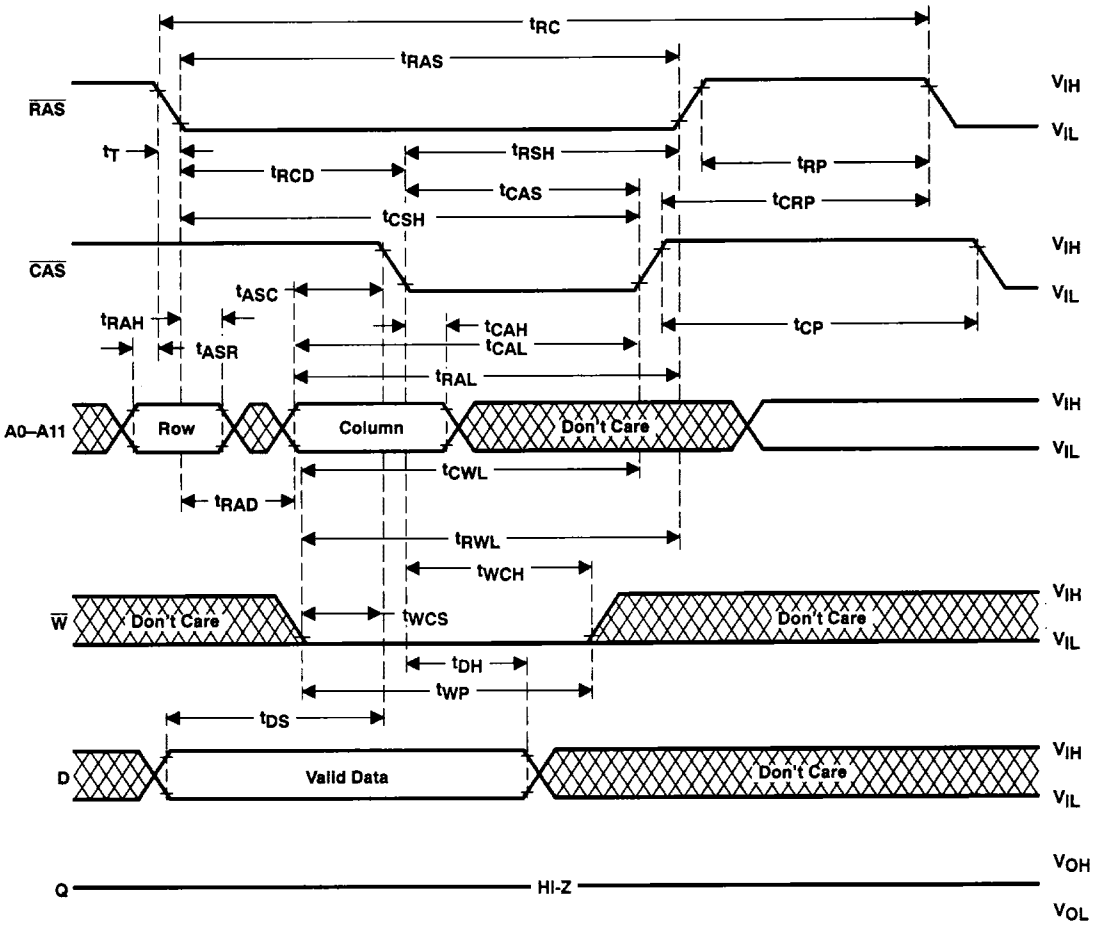


Figure 3. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

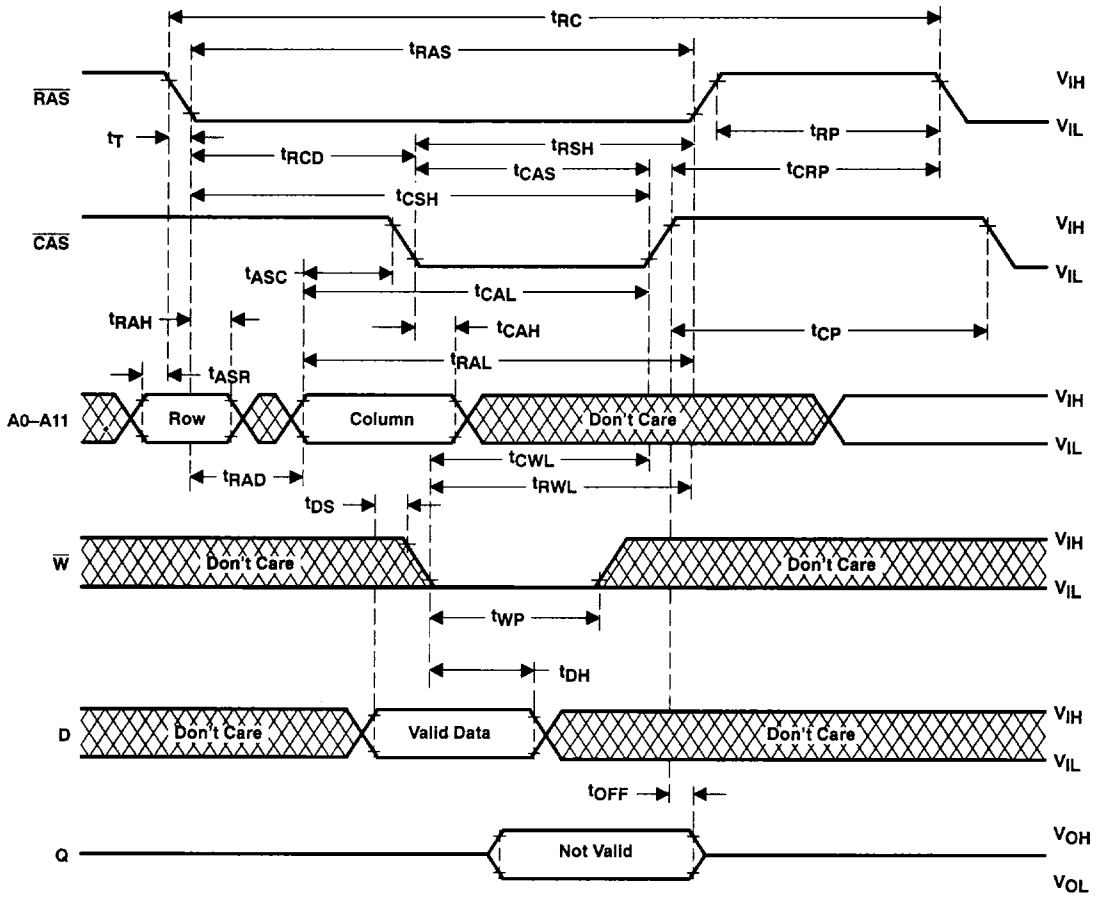
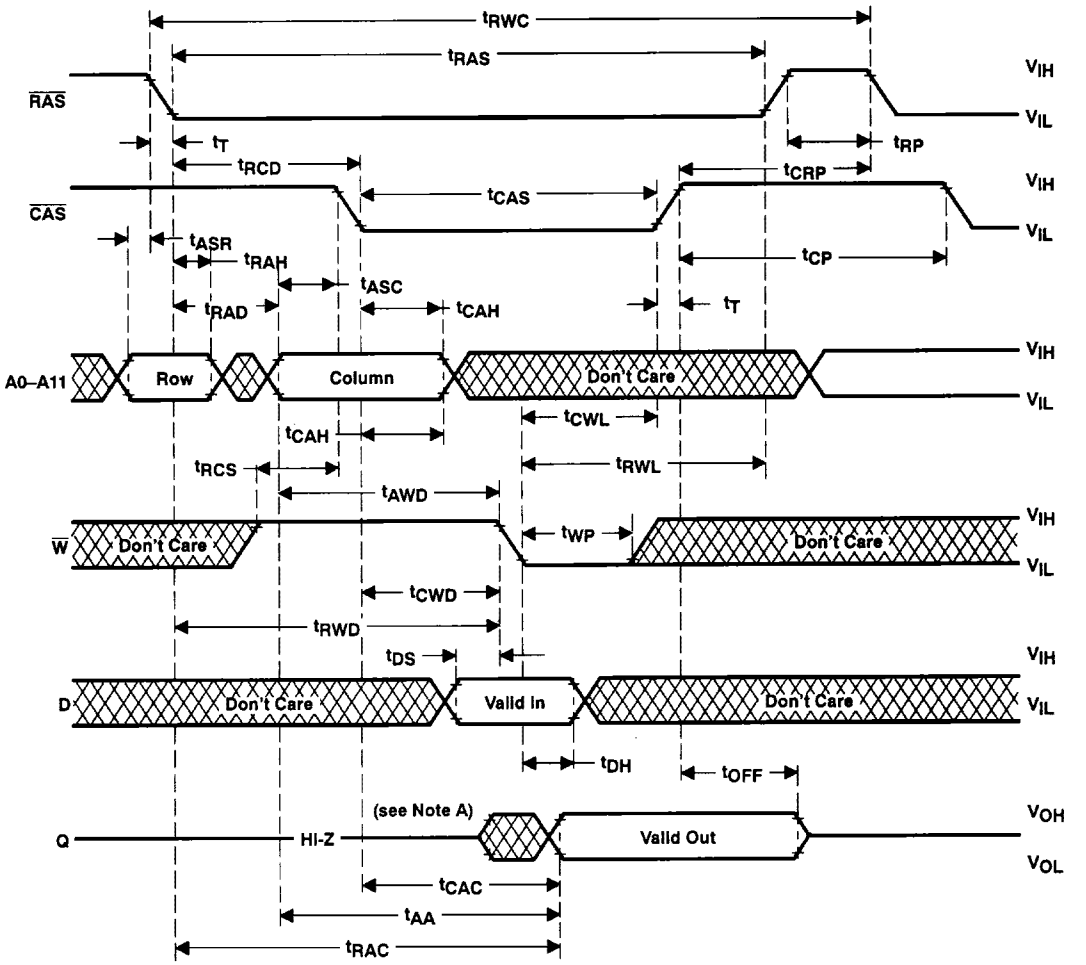


Figure 4. Write Cycle Timing

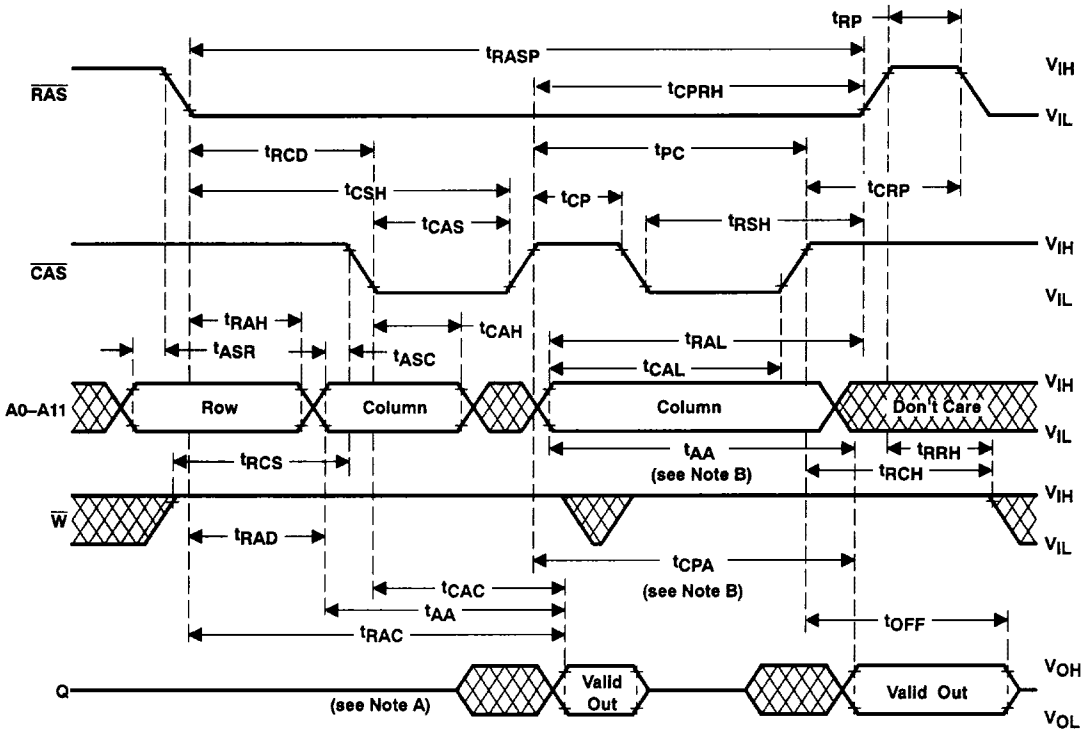
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 5. Read-Write Cycle Timing

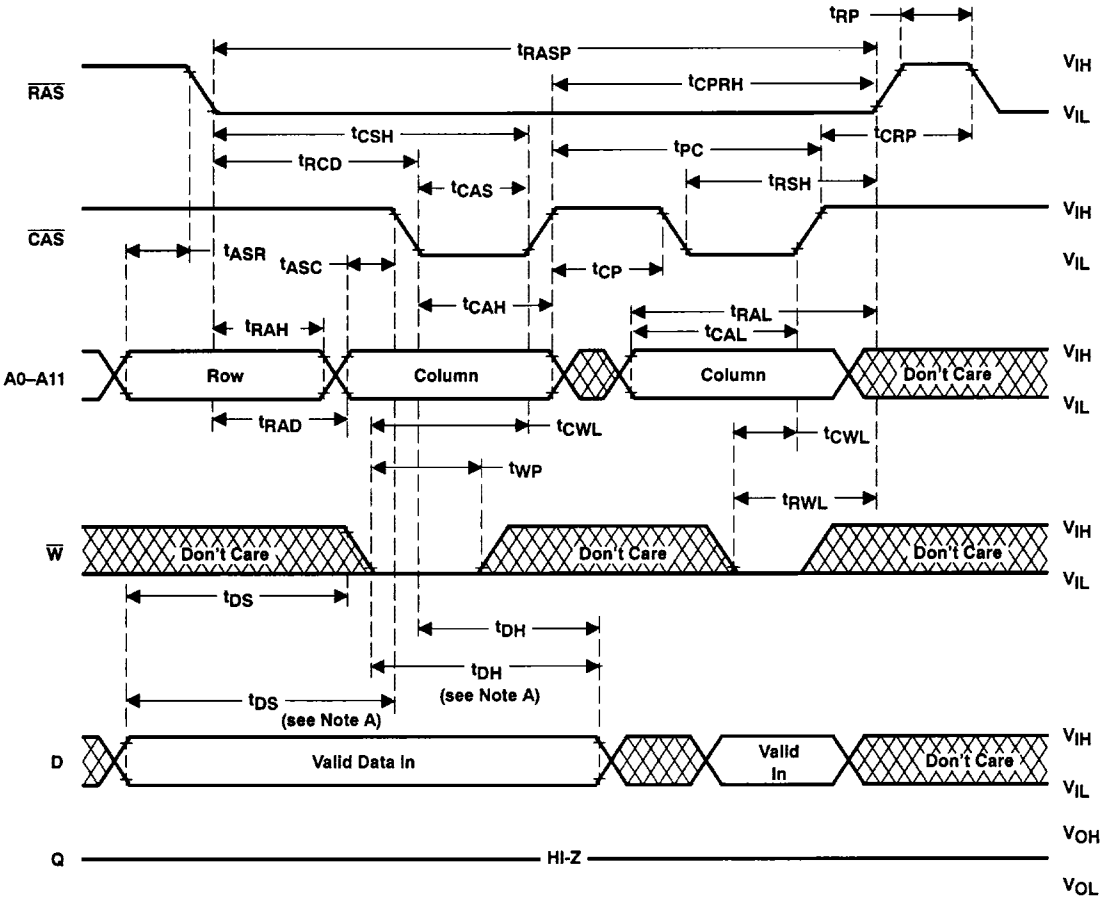
PARAMETER MEASUREMENT INFORMATION



NOTES: A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.
B: Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

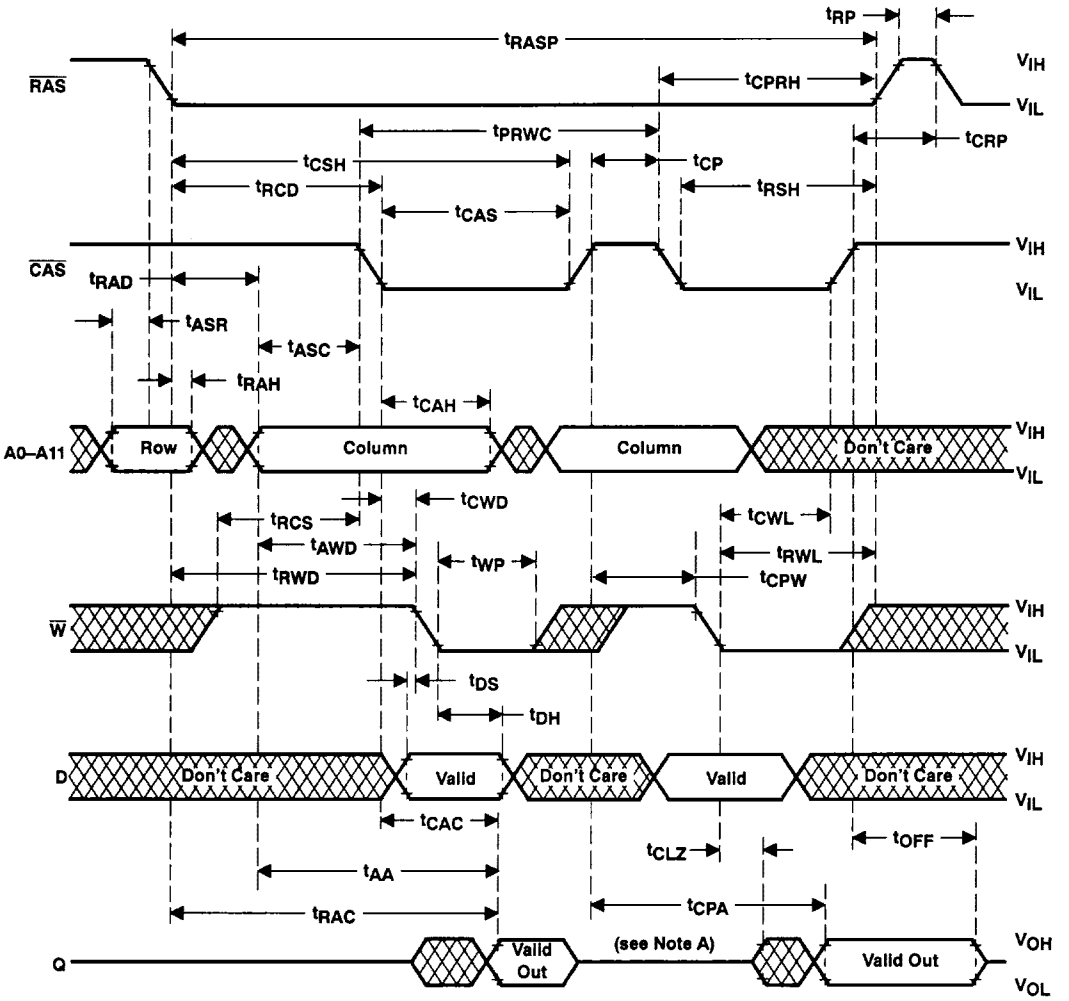
PARAMETER MEASUREMENT INFORMATION



NOTES: A: Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B: A read cycle or a read-write cycle can be intermixed with write cycle as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

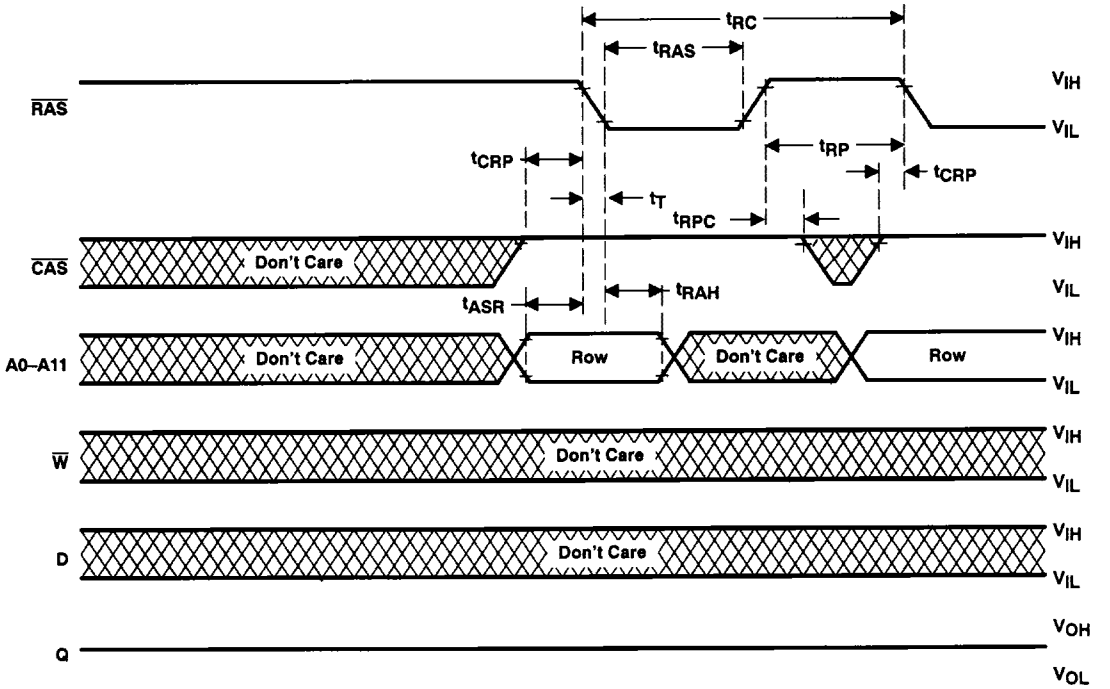


Figure 9. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

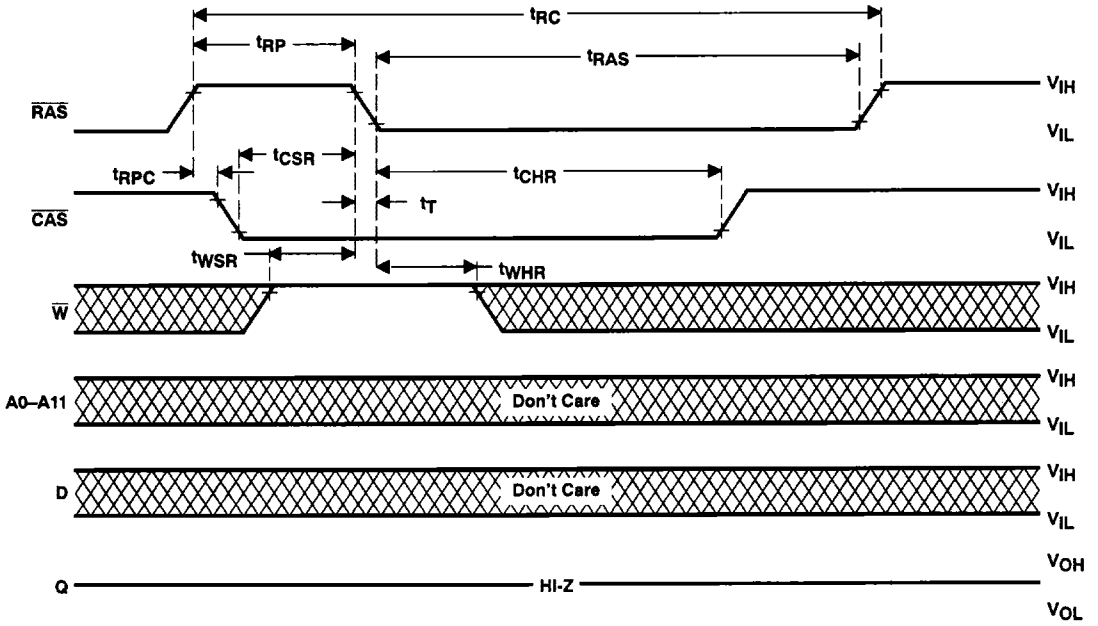


Figure 10. Automatic ($\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

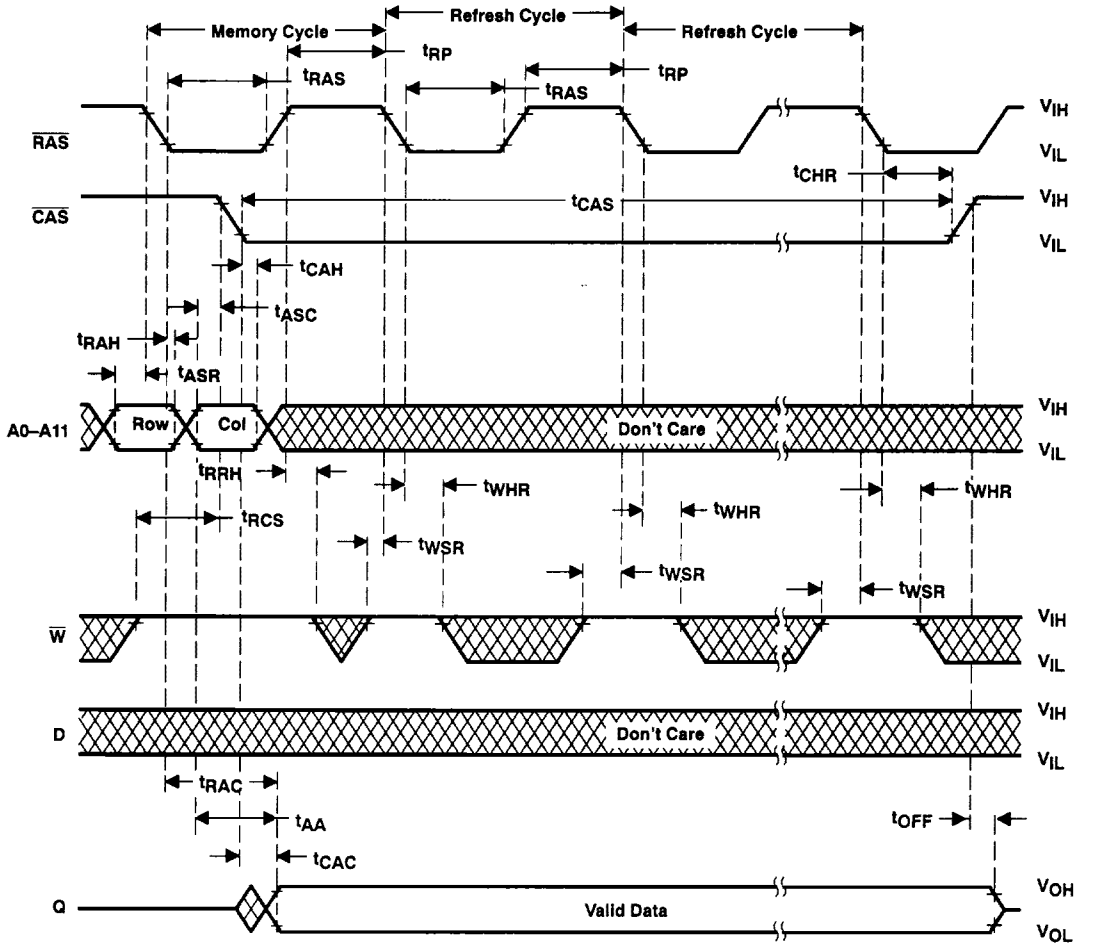


Figure 11. Hidden Refresh Cycle (Read)