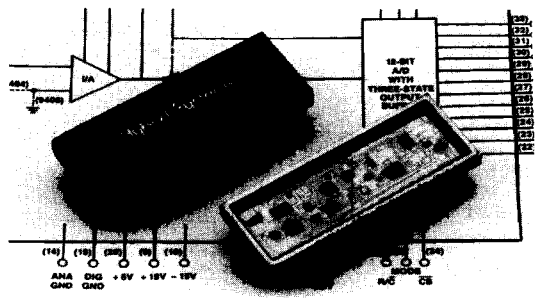
8-CHANNEL, 12-BIT DATA ACQUISITION SYSTEM (DAS)

FEATURES

- Complete 12-bit DAS
  - 8-channel multiplexer
  - Instrumentation amp with programmable gain
  - Sample/hold circuit
  - 12-bit A/D
  - 3-state output buffer
- 40 pin DIP
- 35 kHz throughput
- Low power



DESCRIPTION

The HS9408 is a compact, single-package solution to multichannel acquisition applications. This device is a complete data acquisition systeem which includes input multiplexing, instrumentation amplifier with programmable gain, sample-and-hold circuit, 12-bit A/D converter and control logic. Accuracy and linearity are specified for the complete system from analog input to digital output. The need for ordinary component specifications such as instrumentation amp linearity, gain accuracy, and sample-hold pedestal error are eliminated, as they are guaranteed in system specifications.

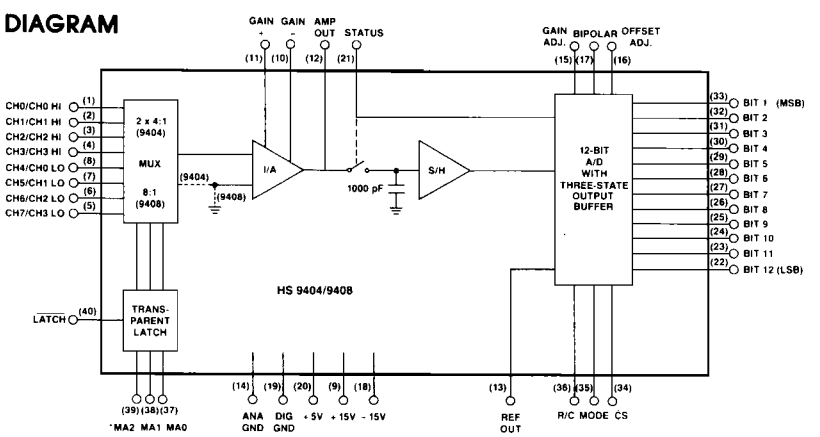
The HS9408 features overvoltage input protection (to ±35V) and the instrumentation amplifier provides gain ranges of 1 to 100*. The gain range is selected through the use of a single external resistor and allows a variable input range of ±100mV to ±10V. Expansion to fifteen single-ended inputs is easily accomplished with two additional ICs.

Total system linearity is specified as ±½ LSB at 25°C and ±¾ LSB is guaranteed over the miltary operating temperature range. System throughput rates of up to 35KHz can be achieved, while a tri-state output buffer permits easy interface with a microprocessor bus.

The HS9408 operates from ±15V and +5V supplies with a total power dissipation of 650mW. It is offered in 40-pin ceramic packages and is specified for operation over the commercial and military temperature ranges. Parts screened to MIL-STD-883 Class B or S are available.

*Gain can be set to higher values, but operation to 12-bit accuracy is not guaranteed.

FUNCTIONAL DIAGRAM



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SPECIFICATIONS

(Typical @ +25°C and nominal power supplies unless otherwise specified)

ANALOG INPUTS

Number of Inputs	
HS 9408	8 Single-Ended
Input Voltage Range[3]	
Unipolar	0 to +10V
Bipolar	±10V or ±5V[1]
Common Mode Voltage Range	±10V
CMRR[2]	
G = 1 @ 200 Hz, Vcm = 20 Vpp	90 dB
Input Bias Current	
+25°C	±15 nA typ, ±100 nA max
−55°C to +125°C	±200 nA (max)
Input Resistance	$10^{12}\Omega$ typ
Input Capacitance	
OFF Channel	5 pF
ON Channel	10 pF
Gain Equation (A_V)	$\frac{20K}{R_G} + 1$

DIGITAL INPUTS (t_{MIN} to t_{MAX})

Logic Levels	
Logic "1"	4.0V min.
Logic "0"	0.8V max.
Logic Loading	1 LSTTL load max

STATIC PERFORMANCE[3]

Integral Nonlinearity[5] (K)	±½ LSB over temperature
(T)	±¾ LSB over temperature
(S,J)	± 1 LSB over temperature
Differential Nonlinearity (T,K)	±1 LSB over temperature
(S,J)	±2 LSB over temperature
No Missing Codes (T,K)	12 bits over temperature
(S,J)	11 bits over temperature
Unipolar Offset Error[3,4]	±0.05% max
Bipolar Minus Full Scale Error[3,4]	±0.05% typ, ±0.1% max
Gain Error[4]	±0.1% typ, ±0.3% max
Channel to Channel Offset Voltage	1 mV max

DYNAMIC PERFORMANCE

Throughput Rate:	
Gain = 1	35 kHz
Gain = 10	28 kHz
Gain = 100	15 kHz
System Acquisition Time (20V step, 0.01%) to A/D Input	3.5 μ sec typ, 10 μ sec max[3]
A/D Conversion Time	20 μ sec typ, 25 μ sec max
S/H Feedthrough Attenuation	90 dB
MUX Crosstalk Attenuation (off isolation)	68 dB
t Settling, MUX IN to AMP OUT (0.01%)	
Gain = 1	2.5 μ sec
Gain = 10	10 μ sec
Gain = 100	40 μ sec
Slew Rate, AMP OUT	13V/μsec
Adjacent Channel Coupling Error[7] (V_{IN} = 20 Vp-p sine wave)	−78 dB @ 40 kHz −90 dB @ 0.5 kHz

DRIFT CHARACTERISTICS

Integral Nonlinearity	±2 ppm/°C
Differential Nonlinearity	±2 ppm/°C
Unipolar Offset[6]	±10 ppm/°C
Bipolar Zero[6]	±10 ppm/°C
Gain[6]	±25 ppm/°C

DIGITAL OUTPUTS

Logic Levels	
Logic "1"	2.4V min
Logic "0"	0.4V max
Leakage	±5μA typ.
Logic Coding	
Unipolar Range	Straight binary
Bipolar Range	Offset binary

POWER SUPPLIES

Power Supply Range	±15V, ±5% 5V, ±5%
PSRR (all supplies)	0.002%/% typ, 0.005%/% max
Current Drain	
+15V	22 mA
−15V	18 mA
+5V	10 mA
Power Dissipation	650 mW

TEMPERATURE RANGE

Operating (J,K)	0°C to +70°C
Operating (S,T)	−55°C to +125°C
Storage	−65°C to +150°C

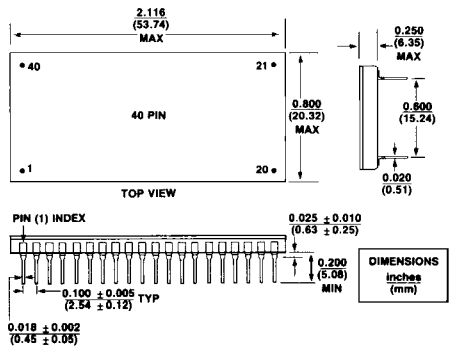
PACKAGE

Weight	15 grams

NOTES:

1. Input range selected at factory.
3. Unity gain configured.
4. Adjustable to zero; see application notes.
5. End point definition.
6. Gain and offset drift specifications as stated in data sheet are maximum (average) limits over the given temperature range, tested at temperature end points.
7. For best performance above 1 kHz, connect package lid to analog ground.

PACKAGE OUTLINE



NOTE: Initial commercial offerings will be in ceramic with future offerings in plastic.

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	CH0/CH0 HI	40	$\overline{\text{LATCH}}$
2	CH1/CH1 HI	39	MA2*
3	CH2/CH2 HI	38	MA1
4	CH3/CH3 HI	37	MA0
5	CH7/CH3 LO	36	R/$\overline{\text{C}}$
6	CH6/CH2 LO	35	MODE
7	CH5/CH1 LO	34	$\overline{\text{CS}}$
8	CH4/CH0 LO	33	BIT 1 (MSB)
9	+15V	32	BIT 2
10	GAIN (−)	31	BIT 3
11	GAIN (+)	30	BIT 4
12	AMP OUT	29	BIT 5
13	REF OUT	28	BIT 6
14	ANALOG GND	27	BIT 7
15	GAIN ADJ	26	BIT 8
16	OFFSET ADJ	25	BIT 9
17	BIPOLAR	24	BIT 10
18	−15V	23	BIT 11
19	DIGITAL GND	22	BIT 12 (LSB)
20	+5V	21	STATUS

*HS 9408 only.

ABSOLUTE MAXIMUM RATINGS (HS 9404/HS 9408)

+15V (+V_{DD})	+16.5V
−15V (−V_{DD})	−16.5V
+5V (+V_{CC})	+7V
Analog GND to Digital GND	±0.5V
Digital Inputs to Digital GND	+5.5V max −0.5V min
Analog Inputs to Analog GND	
Pins 1 through 8	±35V
Pins 10, 11, 15, 16, 17	±V_{DD}
Amp Out to Analog or Digital GND	Indefinite short circuit
REF OUT to Analog or Digital GND	Indefinite short circuit
to ±V_{DD}	100 ms short circuit
Voltage on Digital Ouputs in Tri-State Mode	+V_{CC} +0.5V max −0.5V min
Lead Temperature, Soldering	300°C, 10 sec

APPLICATIONS INFORMATION

CONTROL FUNCTIONS

The HS 9408 contains control functions necessary to provide for microprocessor interface. All control functions are defined in Tables 1, 2, and 3.

FUNCTION	DEFINITION	FUNCTION
R/$\overline{C}$	Read/Convert	1. ↓ initiates conversion 2. High (1) initiates read along with $\overline{CS}$ low
$\overline{CS}$	Chip Select	1. High (1) disconnects data bus 2. Low (0) connects data bus, must be low for conversion to start
$\overline{Latch}$	Latch	1. High (1) transparent 2. Low (0) MUX address latched
MA0 MA1 MA2*	Multiplexer Address	Select Channels (see MUX Logic Table 3)
MODE	$\overline{12\text{-bit}}$/8-bit	1. High (1) indicates 8-bit conversion 2. Low (0) indicates 12-bit conversion

*HS 9408 only

Table 1. Defining the Control Functions

CONTROL INPUTS R/$\overline{C}$	CONTROL INPUTS $\overline{CS}$	OPERATION
↓	0	Initiates conversion
1	1	Output goes to high impedance state
1	0	Initiates read

Table 2. Truth Table — Control Inputs

MUX ADDRESS INPUTS MA2*	MA1	MA0	CHANNEL SELECTED HS 9404	HS 9408
0	0	0	CH0 HI/CH0 LOW	CH0
0	0	1	CH1 HI/CH1 LOW	CH1
0	1	0	CH2 HI/CH2 LOW	CH2
0	1	1	CH3 HI/CH3 LOW	CH3
1	0	0	—	CH4
1	0	1	—	CH5
1	1	0	—	CH6
1	1	1	—	CH7

NOTES:
*Applies to HS 9408 only. $\overline{Latch}$ high allows MUX address to MUX.
$\overline{Latch}$ low latches the address present during low edge and keeps that channel selected.

Table 3. Truth Table — Multiplexer Address

TIMING

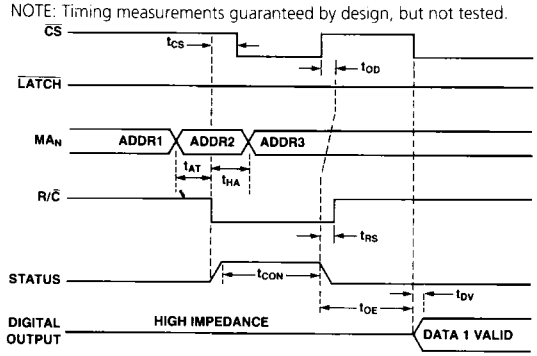
The timing diagram in Figure 1 shows how the HS 9408 works when controlled by a microprocessor. The normal sequence of events is as follows:

1. The input signal is acquired by the MUX, AMP and S/H (track mode) after the MUX address is changed.
2. A conversion is initiated by the R/$\overline{C}$ control line going to logic "0". Concurrent with this event, the status line goes to logic "1" to indicate the A/D is "busy". When the A/D is "busy", the S/H is in the hold mode.
3. The A/D indicates completion of the conversion by returning the status line to logic "0".
4. Data is placed on the output bus when the R/C control line is set to logic "1" and when the CS line is set to logic "0".

Reference Figure 1 for timing constraints of various operations.

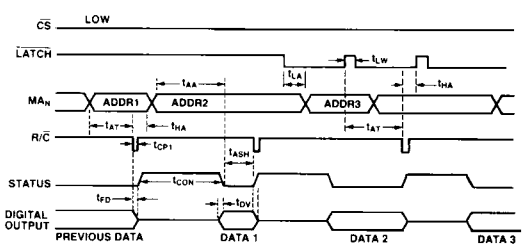
Figure 2 shows the timing requirements for stand-alone operation. The major difference between stand-alone and bus compatible operation is the use of the $\overline{CS}$ control line. Since stand-alone operation does not require the output data to arrive at a specified time, the $\overline{CS}$ line is kept at logic "0". This presents output data immediately after conversion is complete. Reference Figure 2 for timing constraints of various operations.

NOTE: Timing measurements guaranteed by design, but not tested.



t_{CS} – CHIP SELECT DELAY TIME – 100 nsec MAX.
t_{OD} – OUTPUT DISABLE DELAY AFTER ↓ OF STATUS – 35 nsec MAX.
t_{AT} – TOTAL ACQUISITION TIME OF MUX, AMP, S/H (TRACK MODE) – SEE SPECIFICATIONS.
t_{HA} – S/H HOLD APERTURE TIME – 500 nsec. (MINIMUM TIME BEFORE SWITCHING MUX ADDRESS)
t_{RS} – READ SETUP TIME – 0 nsec MIN.
t_{OE} – OUTPUT ENABLE SETUP TIME – 0 nsec MIN.
t_{DV} – DATA VALID TIME – 250 nsec.
t_{CON} – CONVERSION TIME OF A/D – 25 μsec (12 BITS) MAX
19 μsec (8 BITS) MAX

Figure 1. Timing for Bus Compatible DAS



t_{AT} – TOTAL ACQUISITION TIME OF MUX, AMP, S/H (TRACK MODE) – THIS IS THE TIME FROM CHANGING THE ADDRESS TO STARTING A NEW CONVERSION. SEE SPECIFICATIONS.
t_{CP1} – NEGATIVE CONVERT PULSE WIDTH – 50 nsec MIN., 1 μsec MAX.
t_{FD} – OUTPUT FLOAT DELAY TIME – 150 nsec.
t_{CON} – CONVERSION TIME OF A/D – 25 μsec MAX.
t_{HA} – S/H HOLD APERTURE TIME – 500 nsec.
t_{AA} – MUX AND AMP ACQUISITION TIME – SEE SPECIFICATIONS.
t_{ASH} – S/H ACQUISITION TIME – 7 μsec TYP., 10 μsec. MAX..
t_{DV} – DATA VALID TIME – 1000 nsec MAX, 250 nsec MIN.
t_{LA} – $\overline{LATCH}$ TO ADDRESS CHANGE TIME – 30 nsec.
t_{LW} – LATCH PULSE WIDTH – 80 nsec MIN.

Figure 2. Timing for Stand-Alone Operation

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OFFSET AND GAIN CONNECTIONS

The DAS is normally used with external offset and gain calibration potentiometers. However, if maximum accuracy is not required, they may be omitted. The offset control has a range of about ±20 LSB, and the gain control has a range of about ±13 LSB.

Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate instruments. The voltage source used as a signal input must be very stable. It also should be capable of being set to within 1/10 LSB at both ends of its range.

The DAS's offset and gain adjustments are independent of each other if the offset adjustment is made first. To minimize transition noise at the gain and offset pins, a 1 μF decoupling capacitor should be connected as shown on the diagram of Figure 3.

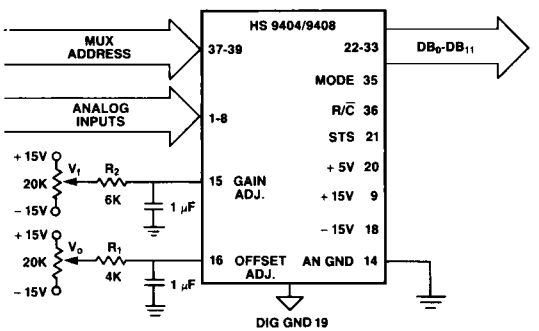


Figure 3. Gain and Offset Input Connections

OFFSET ADJUSTMENT PROCEDURE

1. For unipolar ranges:
   a) Set input voltage precisely to + 1/2 LSB.
   b) Adjust zero control until converter is switching from 000000000000 to 000000000001.
2. For bipolar ranges:
   a) Set input voltage precisely to 1/2 LSB above −FS.
   b) Adjust zero control until converter is switching from 000000000000 to 000000000001.

GAIN ADJUSTMENT PROCEDURE

1. Set input voltage precisely to 1/2 LSB less than "all bits on" value. Note that this is 1-1/2 LSB less than nominal full scale.
2. Adjust gain control until converter is switching from 111111111110 to 111111111111.

GAIN ADJUSTMENT PROCEDURE (continued)

Table 4 summarizes the offset and gain adjustment procedure and shows the proper input test voltages used in calibrating the DAS.

Input Voltage Range	Adjustment	Input Voltage	Adjust input to point where converter is just on the verge of switching between the two codes shown.[1]
0 to +10V	OFFSET	1.22mV	0000 0000 0000
	GAIN	9.9963V	1111 1111 1110
±5V	OFFSET	−4.9988V	0000 0000 0000
	GAIN	4.9963V	1111 1111 1110
±10V	OFFSET	−9.9976V	0000 0000 0000
	GAIN	9.9927V	1111 1111 1110

[1]Codes shown are natural binary for unipolar input ranges and offset binary for bipolar ranges.
0 = transition between logic "1" and logic "0".

Table 4. Calibration Data

Note: For bipolar operation, OFFSET adjust sets −full scale (or all zeros out code), not 0V in (midscale code).

The offset and gain adjustments at pins 16 and 15 only affect the A/D converter. The offset adjustment as shown should have enough range to compensate for any internal errors. If the internal amplifier is used at greater than unity gain, a gain adjustment should be added to the R_G circuit of the instrumentation amplifier. Note: If the gain and offset pins are not being used, they should be left floating.

GROUNDING CONSIDERATIONS

To insure maximum accuracy, the HS 9404/HS 9408s have a separate analog and digital ground; these two grounds must be routed properly to prevent DC and transient errors.

DC errors can be caused by current flowing through a run resistance between the system ground reference and the DAS ground reference. (One mA through 2.5Ω will cause an LSB of error.) The best way to prevent this type of error is to connect the digital and analog grounds very close to the HS 9408 and use this point as the system ground. This can be done as a so-called "star ground" as shown in Figure 5a or as shown in Figure 5b. In Figure 5a, the single common ground reference insures no ground current or ground loop errors. The circuit of Figure 5b sends all digital currents to the digital supply reference thereby preventing any digital current flow through a common ground supply return.

APPLICATIONS INFORMATION (continued)

GROUNDING CONSIDERATIONS (continued)

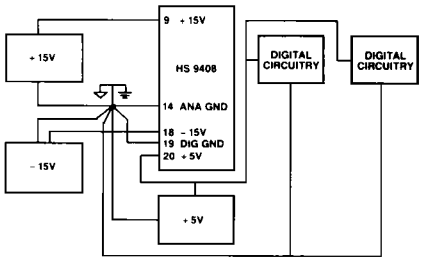


Figure 5a.

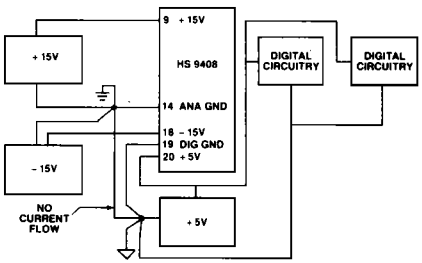


Figure 5b.

Since all ground currents are returned to their respective power supplies, no current flows through the connection between analog and digital ground; this causes both ground points to be at the same potential. If possible, a ground plane should be placed underneath the package to reduce noise pickup. If this is not the case, do not run any digital lines underneath the package. The HS 9408 Series has been layed out such that the analog section is on pins 1 through 20 and the digital section is on pins 21 through 40. To get 12-bit accuracy, the PC board should adhere to the same general layout rules.

To minimize transient-caused errors, decoupling capacitors are recommended between all supplies and their respective grounds. The HS 9408 has three 0.01µF ceramic bypass capacitors inside, so an external 10µF for each supply should be all that is required.

INSTRUMENTATION AMPLIFIER & ANALOG FRONT END

The HS 9408 has a full instrumentation amplifier with high impedance differential inputs and resistor programmable gain. The output of the amplifier is available for driving other analog circuitry or accessing the signal after amplification. Be aware that any loading in excess of 2 K ohms in parallel with 10 pF will adversely affect output voltage swing and settling time.

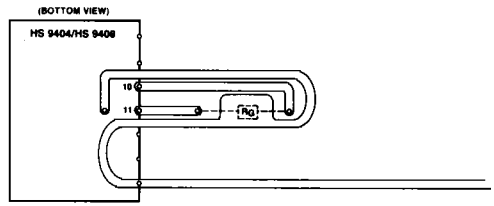
The formulas for calculating gain and the gain resistor are as follows:

$$A_V = \frac{20K}{R_G} + 1 \qquad R_G = \frac{20K}{A_V - 1}$$

Some typical values are as follows:

GAIN	1	5	10	50	100
R_G	infinite	5.000 KΩ	2.222 KΩ	408.2Ω	202.0Ω

Special care must be exercised when operating at high gains (>20) to avoid coupling error signals into the relatively high impedance GAIN (−) and GAIN (+) pins. The gain set resistor should be placed as close to the HS 9408 package as possible and the connections should be guarded with a quiet, low impedance signal trace such as analog ground, REF OUT, + 15V or AMP OUT. The use of a ground plane is preferred. To minimize gain errors due to temperature, a low drift (low temperature coefficient of resistance) resistor should be used for R_G with a TCR < 25 ppm/°C over the required temperature range.



Reference output current capability decreases as temperature increases. If REF OUT must supply more than ± 1 mA above 70°C, an external current buffer is recommended.

If the circuit is to be used at or near its maximum throughput rate, care must be used to prevent dynamic errors due to source impedance at the multiplexer inputs. If a low-pass anti-alias filter is used at the analog inputs (Figure 6a), it is suggested that a buffer be used (Figure 6b) to eliminate charge-transfer errors between C_{FILTER} and $C_{MUX,AMP}$ (Figure 6c).

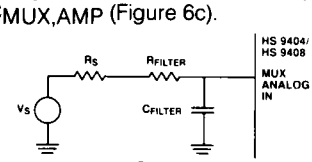


Figure 6a. (not recommended)

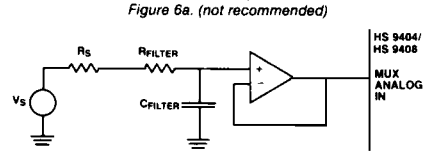


Figure 6b. (recommended)

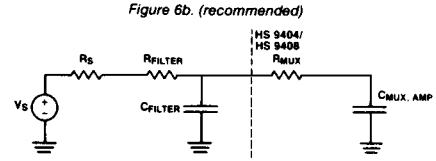


Figure 6c. (equivalent circuit of 6a)

The multiplexer used on the military processed devices is made with dielectrically isolated CMOS analog switches. They can withstand a continuous voltage of 10 volts greater than either supply and transient spikes of several hundred volts. This can eliminate the need for complex protection. The commercial devices use a multiplexer which can withstand voltages no greater than V_{SUPPLY}[4]. Thus, for commercial devices, make sure that power is applied to the device before or at the same time analog voltages appear at the MUX. This will save the device from destruction.

APPLICATIONS INFORMATION (continued)

UNIPOLAR/BIPOLAR CONFIGURATION

The HS 9408 - 2 are 20 volt range units which must be operated in bipolar configuration to give a ± 10V input signal range (for unity gain amplification). The HS 9408 - 1 are 10 volt range units which can be operated in unipolar or bipolar modes.

To connect for bipolar operation, short pin 17 to pin 13. For unipolar operation, short pin 17 to analog ground.

Noise performance is improved in bipolar mode if pin 17 is decoupled to analog ground with a 0.01 μF ceramic capacitor. (This value may be inadequate at + 125°C, causing the reference to oscillate.)

INPUT EXPANSION

The DAS is configured with either an 8-channel single-ended or 4-channel differential input. This was done to optimize package size and cost. In the event the user wishes to increase the number of input channels, examples of input expansion are shown in Figures 7a and 7b.

ADDR2	ADDR1	ADDR0	CHANNEL OUT
0	0	0	NONE
0	0	1	± IN1
0	1	0	± IN2
0	1	1	± IN3
1	0	0	± IN4
1	0	1	± IN5
1	1	0	± IN6
1	1	1	± IN7

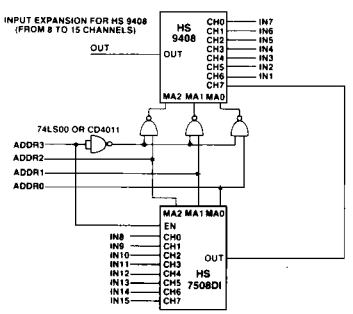


Figure 7a

ADDR3	2	1	0	CHANNEL OUT
0	0	0	0	NONE
0	0	0	1	IN1
0	0	1	0	IN2
0	0	1	1	IN3
0	1	0	0	IN4
0	1	0	1	IN5
0	1	1	0	IN6
0	1	1	1	IN7
1	0	0	0	IN8
1	0	0	1	IN9
1	0	1	0	IN10
1	0	1	1	IN11
1	1	0	0	IN12
1	1	0	1	IN13
1	1	1	0	IN14
1	1	1	1	IN15

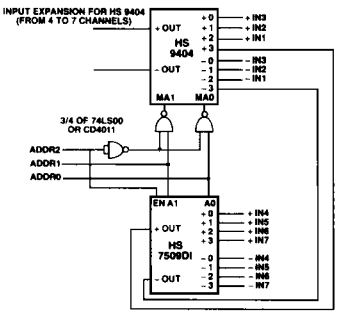
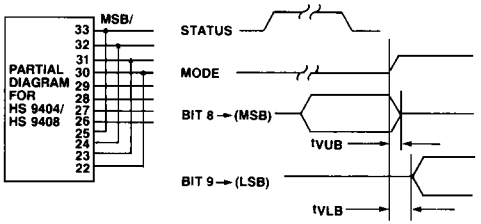


Figure 7b

To allow the HS 9408 to be used with an 8-bit bus, Figure 8 should be utilized.



tVUB = TIME FOR UPPER BITS TO GO TO HIGH IMPEDANCE – 125ns
tVLB = TIME FOR LOWER BITS TO REACH VALID STATE – 250ns

Figure 8. 8-Bit Bus Read Mode — 12-Bit Conversion

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Devices should never be plugged in under power and the PC board the device is in should be handled with caution. Unused digital inputs should never exceed the logic supply by 0.5 volts or go below ground by 0.5 volts. Thus, when powering up these devices, all supplys should come on at the same time. If not, a logic "1" on an unpowered device can destroy the digital inputs.

ORDERING INFORMATION

MODEL NUMBER	INTEGRAL LINEARITY	INPUT RANGE(S)	TEMPERATURE RANGE	SCREENING
HS 940X-J1	± 1 LSB	± 5V, 0 to + 10V	0°C to + 70°C	
HS 940X-J2	± 1 LSB	± 10V	0°C to + 70°C	
HS 940X-K1	± ½ LSB	± 5V, 0 to + 10V	0°C to + 70°C	
HS 940X-K2	± ½ LSB	± 10V	0°C to + 70°C	
HS 940X-S/B-1	± 1 LSB	± 5V, 0 to + 10V	– 55°C to + 125°C	883 Rev. C
HS 940X-S/B-2	± 1 LSB	± 10V	– 55°C to + 125°C	883 Rev. C
HS 940X-T/B-1	± ½ LSB	± 5V, 0 to + 10V	– 55°C to + 125°C	883 Rev. C
HS 940X-T/B-2	± ½ LSB	± 10V	– 55°C to + 125°C	883 Rev. C