

Am9581

Floppy/Hard Disk Data Separator ADVANCED INFORMATION

2

DISTINCTIVE CHARACTERISTICS

- Complete on-chip Phase-Locked-Loop (PLL)
- On-chip MFM/FM Encoder/Decoder
- Supports: 4 to 16Mbits/sec MFM data rates for Hard Disks
125 to 500Kbits/sec Single Density (FM) and
250K to 1Mbits/sec Double Density (MFM) for
Floppy Disks
- On-chip Write Pre-compensation
- On-chip Address Mark Generator/Detector
- Provides Clock extracted from the input data for Run-Length-Limited codes

GENERAL DESCRIPTION

The Am9581 Floppy/Hard Disk Data Separator (DDS) is a single-chip solution to several functions associated with reading and writing information to disk drive memory systems. The Am9581 is divided into three sections: read, write, and control.

The read section contains an on-board Phase-Locked-Loop (PLL) to provide a clock signal that tracks the FM/MFM serial data read off the disk. This data is then fed into the MFM/FM decoder to be converted into NRZ data. Also in this section is the Address Mark Detector for both floppy and hard disks.

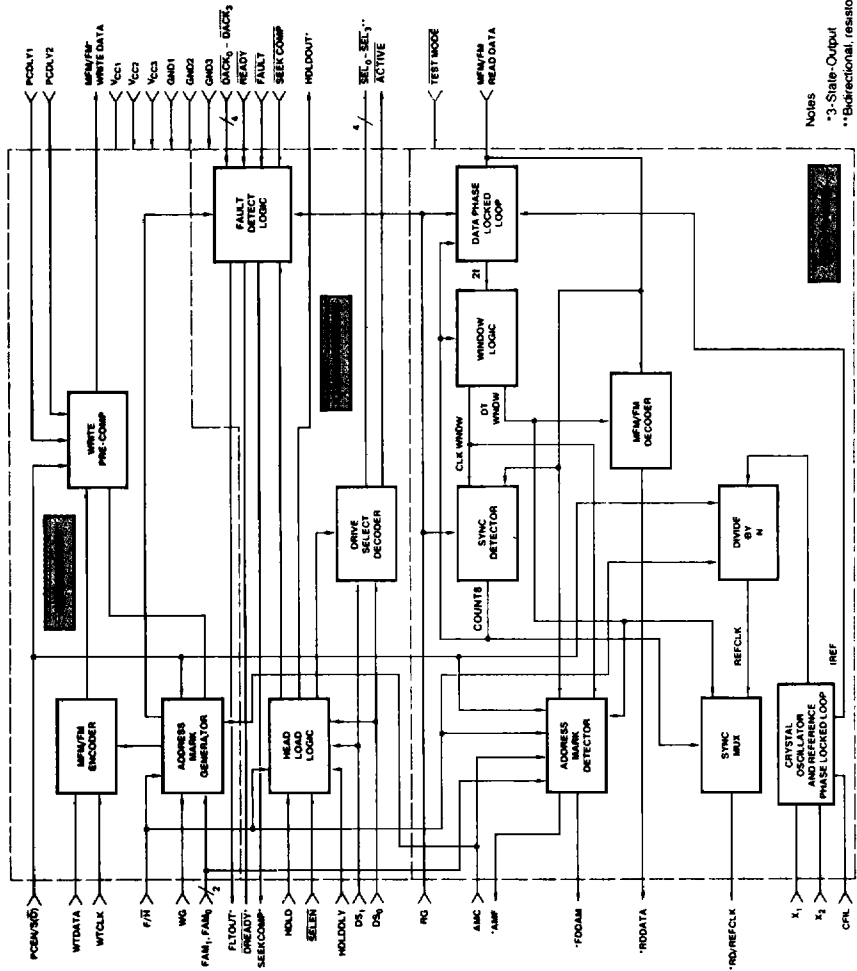
The write section contains an encoder to serialize NRZ data and its reference clock into a single bit stream of data

(MFM or FM) to store on the disk. Also in the write section are the Address Mark Generation and the Write Pre-compensation sections. Each sector on a disk contains several Address Marks. These enable the controller to identify sector types, sector numbers and data fields. The Write Pre-compensation section is used to overcome the problem of bit shifting caused by the method of storage on the media.

The control section handles mainly the drive select and also the head loading logic for floppy disks.

Used in conjunction with the Am9580 Hard Disk Controller (HDC), the chip set provides the total solution for ST-506 and ST-412 disk interface.

Block Diagram

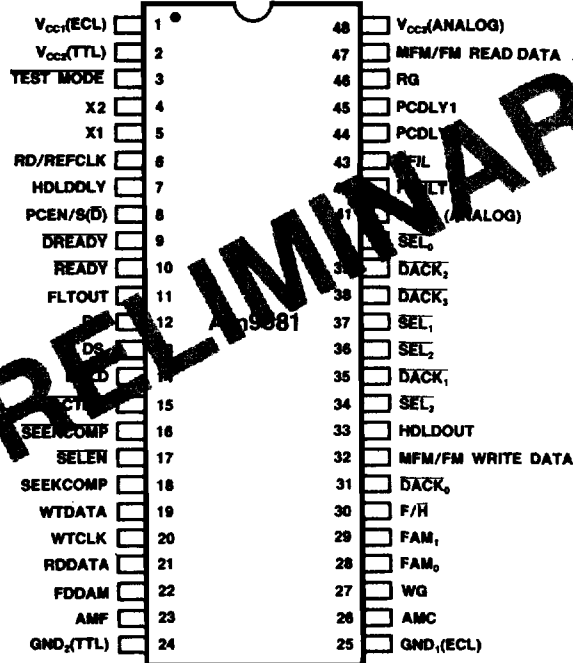


Notes
 * 3-State-Output
 ** Bidirectional, resistor pull up
 BD004052

Figure 1.
 Notes: * 3-State output.
 ** Bidirectional, resistor pull-up.

**CONNECTION DIAGRAM
Top View**

48-Pin

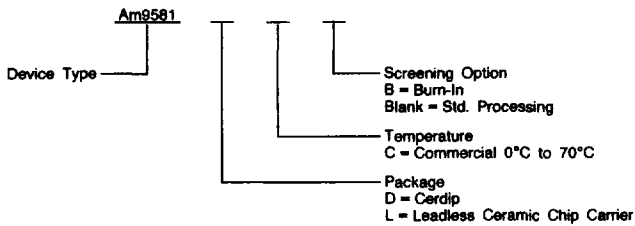


CD005631

Figure 2.

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations	
Am9581	DC (48 leads), LC (52 LCC)

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, check for newly released valid combinations and/or obtain additional data on AMD's standard military grade product.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
WRITE SECTION			
8	PCEN/S(\bar{D})	I	Pre-Compensation Enable/Single/Double Density. This pin has two functions which are multiplexed. When a drive is selected (SELEN going from HIGH to LOW), the logic level on PCEN/S(\bar{D}) is stored internally. A HIGH causes single density operation. A LOW causes double density operation. During a Write operation, a HIGH causes data pre-compensation to take place; otherwise, the data is uncompensated. If single density has been selected when SELEN goes LOW, then PCEN has no effect and the data is always uncompensated.
45, 44	PCDLY1, PCKLY2	I	Pre-Compensation Delay. The ratio of resistors (R_{PC1} , R_{PC2}) connected between PCDLY1 and PCKLY2 pins and V_{CC} sets the pre-compensation delay. The range of pre-compensation delay can be set by the user from 1% to 20% of the bit cell time with an accuracy of $\pm 5\%$ of the chosen value or 1ns, whichever is greater using 1% resistors. The minimum precomp delay that can be set is 2ns.
19	WTDATA	I	Write Data. NRZ data is applied to this input pin for FM or MFM encoding.
20	WTCLK	I	Write Clock. Write Clock is used to synchronize the NRZ write data for magnetic recording. This pin is normally connected to the RD/REFCLK output pin. The user should note that the NRZ input data must meet set-up and hold requirements to the write clock. Skew may be compensated by connecting the write clock to the delayed RD/REFCLK.
27	WG	I	Write Gate. When HIGH, this line enables the WRITE CHANNEL so that writing data onto the disk is made possible. When both WG and RG (Read Gate) are HIGH, a fault condition is generated causing the FLTOUT line to go HIGH.
29, 28	FAM ₁ , FAM ₀	I	Floppy Address Mark Select Bits. These two input bits are used to select the desired Address Mark related to floppies. These bits are further qualified by F/H (Floppy/Hard Disk input select bit) and S/ \bar{D} inputs. These lines are also used to set up the chip for use with RLL codes as shown in Table 1.
30	F/H	I	Floppy/Hard Disk Select. When this pin is tied HIGH, the DDS chip is selected for use with single or double density floppies. When tied LOW, the DDS is selected for hard disks. This input line is also used to select the Address Marks for floppies or hard disks. The selection criteria are listed in Table 1.
32	MFM/FM WRITE DATA	O	Write Data (3-State). Encoded output data used for the actual recording process. MFM format is used for most hard disk and double density floppies, and FM is used for single density floppies. This line is 3-stated when none of the drives connected to the DDS is selected.
READ SECTION			
46	RG	I	Read Gate. A HIGH on this pin enables the READ CHANNEL so that processing of the read back data using the data Phase-Locked-Loop (PLL) can proceed. If both RG and WG are active, a fault condition is generated, causing FLTOUT to go HIGH.
47	MFM/FM READ DATA	I	Read Data. The input to this pin is the MFM/FM encoded information read back from the disk. The Data Separator chip separates the clock and the data information from this MFM/FM data and restores it to the original NRZ format.
5, 4	X ₁ , X ₂	I	Reference Frequency. These two input pins are for connections to an external crystal. An external TTL level clock source can be used instead and tied to the X ₁ pin with X ₂ grounded. The frequency of the crystal to be used for various modes of operation is shown in Table 1. The XTAL frequency is divided down internally to produce the necessary 1f and 2f frequencies. (The 2f reference clock is used internally only for FM encoding.)
26	AMC	I	Address Mark Control. This control input line is used to generate and write the Address Marks during a WRITE operation (with WG) and detect the Address Marks during a READ operation (with RG).
23	AMF	O	Address Mark Found (3-State). Becomes active in response to an active AMC to indicate that the selected type of Address Marks specified in Table 1 have been found during a read and that an Address Mark of appropriate type has been written during a write. The line is 3-stated when none of the drives connected to the DDS is selected.
22	FDDAM	O	Floppy Deleted Data Address Mark (3-State). For single density floppies, this output pin indicates the detection of a deleted Data Address Mark. During Read operations, this status signal is generated by the Am9581 only when a request is made by the HDC. For MFM hard disks and double density floppies, this pin will always be LOW when the DDS is selected. This pin is 3-stated when none of the drives connected to DDS is selected. In RLL hard disk mode, this pin is used to output 2f clock synchronous with RDDATA.
21	RDDATA	O	NRZ Read Data (3-State). This line contains the binary NRZ data decoded from the MFM/FM READ DATA. In RLL mode, the input data on the MFM/FM READ DATA pin is passed directly out to the RDDATA output without any decoding taking place.
6	RD/REFCLK	O	Read/Reference Clock (3-State). Read/Reference clock is synchronously multiplexed such that during a READ operation, the clock source is the RDCLK which is derived from the MFM/FM READ DATA bit stream. When not doing a valid READ operation, the clock source is derived from the input to pins X ₁ and X ₂ . The switching from RDCLK to REFCLK is a glitch-free operation. The pin is 3-stated when none of the drives connected to DDS is selected. For RLL hard disks, this pin always outputs REFCLK.
43	CFIL	I	Filter Capacitor. The filter capacitor for the reference PLL is connected between this pin and ground.
CONTROL SECTION			
14	HDLD	I	Head Load. This input pin is applicable to floppies only and is used for controlling the head loading (when HIGH) and unloading (when LOW) mechanism.

Pin Description (Cont.)

Pin No.	Name	I/O	Description															
33	HDLDOOUT	O	Head Load to Drive (3-State). This is the Head Load signal to the floppy drive. When HDLD from the controller chip goes HIGH, HDLDOOUT goes HIGH immediately. When HDLD goes LOW, there is a delay (set by HDLDDLY) before HDLDOOUT goes LOW. Refer to the timing diagram of Figure 3 for the different cases involving the HDLDOOUT signal.															
7	HDLDDLY	I	Head Load Delay. A resistor R_x connected between this input pin and V_{CC} , and a capacitor C_x connected between this input pin and ground establish a time delay (selected by user) associated with the unloading of the head in floppies. This time delay is necessary so that a drive may be deselected and selected again without unloading and reloading the head. The user may set the time delay from a minimum of 5ms to a maximum of 500ms with a maximum tolerance of 0.5ms or $\pm 5\%$, whichever is larger.															
17	SELEN	I	Select Enable. An active LOW signal to this pin enables the drive specified by the drive select bits DS_1 , DS_0 . The falling edge of SELEN and the status of the PCEN/S(D) pin determine single- or double-density operation for floppies.															
13, 12	DS_0 , DS_1	I	Drive Select. These two pins specify the selection of up to four drives, as indicated below: <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>DS_1</th> <th>DS_0</th> <th>SEL PIN ACTIVATED</th> </tr> </thead> <tbody> <tr> <td>LOW</td> <td>LOW</td> <td>SEL_0</td> </tr> <tr> <td>LOW</td> <td>HIGH</td> <td>SEL_1</td> </tr> <tr> <td>HIGH</td> <td>LOW</td> <td>SEL_2</td> </tr> <tr> <td>HIGH</td> <td>HIGH</td> <td>SEL_3</td> </tr> </tbody> </table>	DS_1	DS_0	SEL PIN ACTIVATED	LOW	LOW	SEL_0	LOW	HIGH	SEL_1	HIGH	LOW	SEL_2	HIGH	HIGH	SEL_3
DS_1	DS_0	SEL PIN ACTIVATED																
LOW	LOW	SEL_0																
LOW	HIGH	SEL_1																
HIGH	LOW	SEL_2																
HIGH	HIGH	SEL_3																
40, 37, 36, 34	$SEL_0 - SEL_3$	O	Select $_{0,3}$ (Resistor Pull-Up). These four output lines are the decoded DS_1 , DS_0 bits used to select up to four drives. When a particular SEL pin is grounded, the DDS will not acknowledge a request for this drive from the HDC (all interface lines to the HDC will be tri-stated). In a typical floppy/Winchester disk drive system with 2 DDS's each attached to 2 drives, the two remaining SEL lines are grounded. In the example on page 17, one DDS interfaces with drives 2 and 3 and has SEL_0 and SEL_1 grounded. Grounding the 2 SEL lines prevents this DDS from acknowledging requests for drives 0 and 1.															
31, 35, 39, 38	$DACK_0 - DACK_3$	I	Drive Acknowledge (Schmitt Trigger Inputs). These input pins reflect the response of an individual drive, acknowledging that it has been selected. Therefore, these inputs are used with the $SEL_0 - SEL_3$ status to test whether the drive that acknowledged is the one being selected; otherwise, a fault condition will be detected.															
10	READY	I	Ready (Schmitt Trigger Input). This input pin indicates that the drive selected is ready to READ, WRITE, or SEEK (access a track).															
9	DREADY	O	Drive Ready (3-State). This status output pin is used to indicate that the selected drive is ready to READ, WRITE or SEEK. When a fault condition is sensed by the F/HDDS, this line is set LOW so that the controller can detect the fault by sensing FLTOUT. The line is 3-stated if none of the drives connected to F/HDDS are selected.															
42	FAULT	I	Fault (Schmitt Trigger). This pin indicates a fault condition when selecting a drive or in the drive itself. An active FAULT is considered only after the Drive Acknowledge bit corresponding to the drive selected is active LOW.															
11	FLTOUT	O	Fault Out (3-State). This output pin is a status output of the fault detection logic. The fault conditions detected are: <ol style="list-style-type: none"> WG and RG both active. Active FAULT from the selected drive. Unselected drives acknowledging drive selection. More than one drive acknowledge in response to a drive selection. The pin is 3-stated when none of the drives connected to F/HDDS is selected.															
16	SEEKCOMP	I	Seek Complete (Schmitt Trigger). This input line indicates that a SEEK operation has successfully been completed and that the head has settled on the desired track. This signal is generated by the drive.															
18	SEEKCOMP	O	Seek Complete (3-State). This status output line is the same as SEEKCOMP for Hard Disk mode. In Floppy mode this output is driven by the Head Load Delay logic (see Detailed Description for details). The line is 3-stated if none of the drives connected to F/HDDS is selected.															
3	TEST MODE	I	This line is used to test the chip logic independent of the PLL.															
15	ACTIVE	O	(TTL) Control for external buffers, if used. This status output pin is used to indicate that none of the drives is selected and all of the control output pins are in tristate.															
25, 24, 41	$GND_1 - GND_3$		Ground.															
1, 2, 48	$VCC_1 - VCC_3$		Power Supply +5V.															

DETAILED DESCRIPTION

The Am9581 simplified block diagram shown in Figure 1 is divided into three sections - (1) the CONTROL section, (2) the WRITE section, and (3) the READ section. The WRITE section and the READ sections are independent of each other and under the supervision of the CONTROL section. The functions of each section are described below.

Control Section

This section consists of the HEAD LOAD LOGIC, DRIVE SELECT DECODER, and the FAULT DETECT LOGIC. The HEAD LOAD LOGIC is enabled only if the DDS is to be used in floppy disk drives. The HEAD LOAD LOGIC block controls the loading and unloading of the floppy disk drive head as specified in the timing diagram of Figure 3. Each of the three operations is described below.

Normal Operation

The controller selects a drive by asserting \overline{SELEN} LOW, causing one of the \overline{SEL}_{0-3} lines to be asserted. Once the drive is selected, the controller can request the DDS to load the head by asserting HDLD. The DDS responds with HDLDOUT going HIGH and asserts SEEKCOMP after a time delay (t_{HDLDLY}) set by the resistor R_X and the capacitor C_X at the HDLDLY pin. This time delay set by the user is to accommodate the setting time associated with the head loading and unloading; t_{HDLDLY} can be calculated as $(1.1 R_X C_X) \pm 5\%$.

To deselect the drive, the controller drives \overline{SELEN} HIGH and HDLD LOW. The actual deselection of the drive and the unloading of the head do not occur until after t_{HDLDLY} .

Same Drive Reselected

The selection of the drive and the loading of the head is the same as described in the normal operation. However, if the same drive (DRIVE 0) is deselected and selected again within the time interval defined by t_{HDLDLY} , then the head can remain loaded (HDLDOUT remaining HIGH). In this case, a different track can be assessed while the head remains loaded.

Different Drive Selected

When a drive (DRIVE 0 for example) is deselected and then a different drive (DRIVE 1) is selected during the time interval t_{HDLDLY} , HDLDOUT will remain HIGH. This means that the head of the newly selected drive will be loaded automatically as shown in Figure 3.

Hard disk drives do not have head loading/unloading mechanisms since the heads are basically floating when the drive is running. (When a hard disk drive is not running, the heads are in contact with the disk in a specified area called the landing zone.) Each time a different track is to be accessed, a hard disk drive is said to be in SEEK mode. When the desired track is found, the drive issues an active SEEKCOMP. This status is indicated to the controller by the Am9581 as an active SEEKCOMP.

Write Section

FM/MFM Encoding

The serial NRZ data pattern is transformed into pulses that occur in a time window specified as the bit cell time. The bit cell time is derived from a very stable reference frequency which can be labeled as the WTCLK. The encoding process takes place during a write operation - i.e., WG is HIGH and RG is LOW. The result of the encoding process is the transformation of the NRZ data and its reference clock into a single bit stream consisting of a CLOCK and/or a DATA pulse for each bit cell depending upon the NRZ value within the bit cell time.

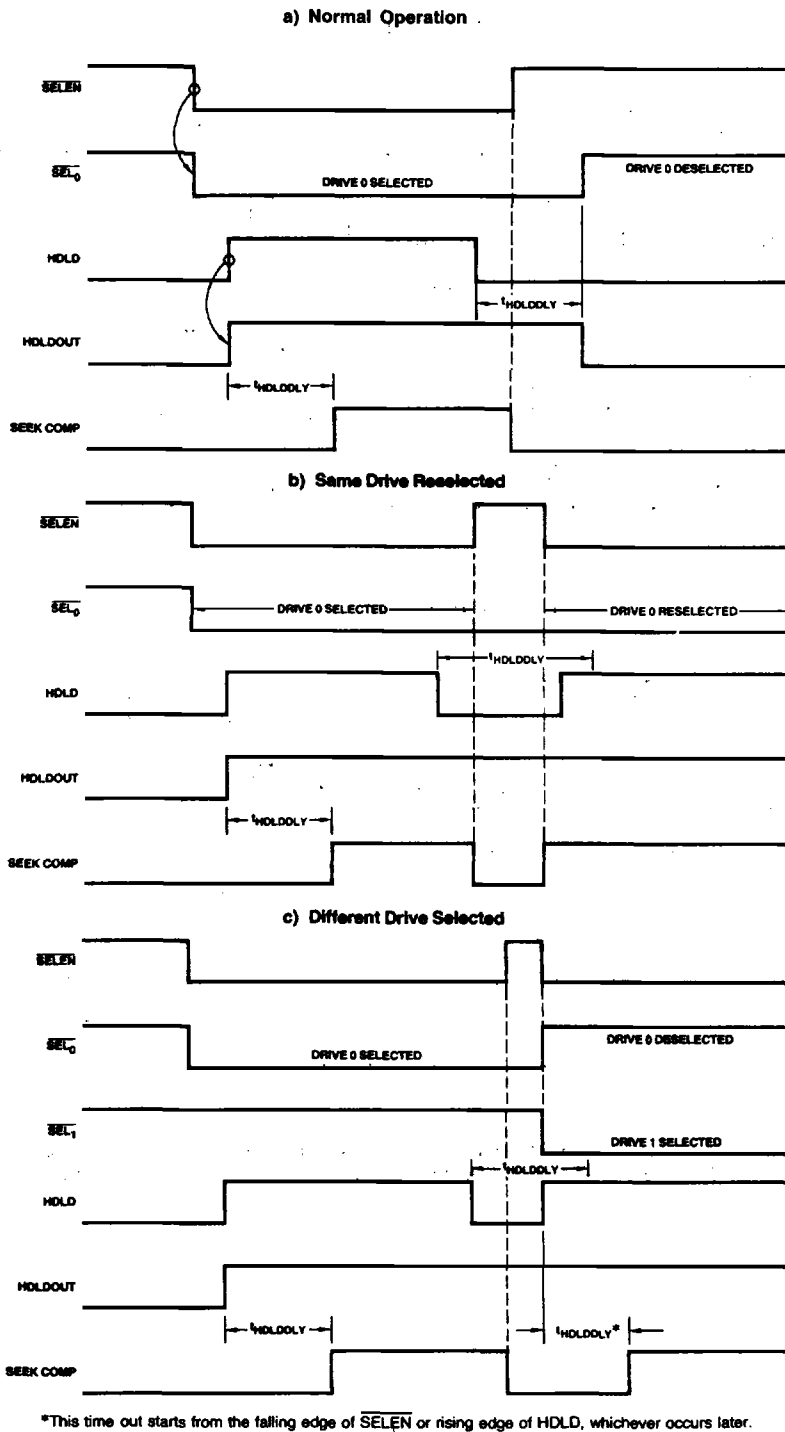
For FM encoding, a CLOCK pulse is always inserted at the beginning of the bit cell. When NRZ data is "1" during the bit cell time, a DATA pulse is inserted in the middle of the bit cell; otherwise, no DATA pulse is inserted. Therefore, for FM encoding, a CLOCK pulse and a DATA pulse can both be present within the bit cell time (which is $4\mu s$ for single density floppies running at 250 Kbit/sec).

In MFM encoding, when the NRZ data is "1" during the bit cell time, a data pulse is inserted in the middle of the bit cell. If the NRZ data is "0" during the bit cell time, no data pulse is inserted. However, unlike FM, the clock pulses are not automatically inserted at the beginning of each bit cell. The clock pulses are inserted at the beginning of a bit cell if and only if the NRZ data is "0" during the current bit cell as well as the previous bit cell. Otherwise, no clock pulses are written (see Figure 4). Therefore, in MFM, only a CLOCK pulse or a DATA pulse can be present within the bit cell time (which is $2\mu s$ for a 500Kbit/sec double density floppy and 200ns for a 5Mbit/sec hard disk drive). FM and MFM encoding are shown in Figure 4.

Address Mark Generation

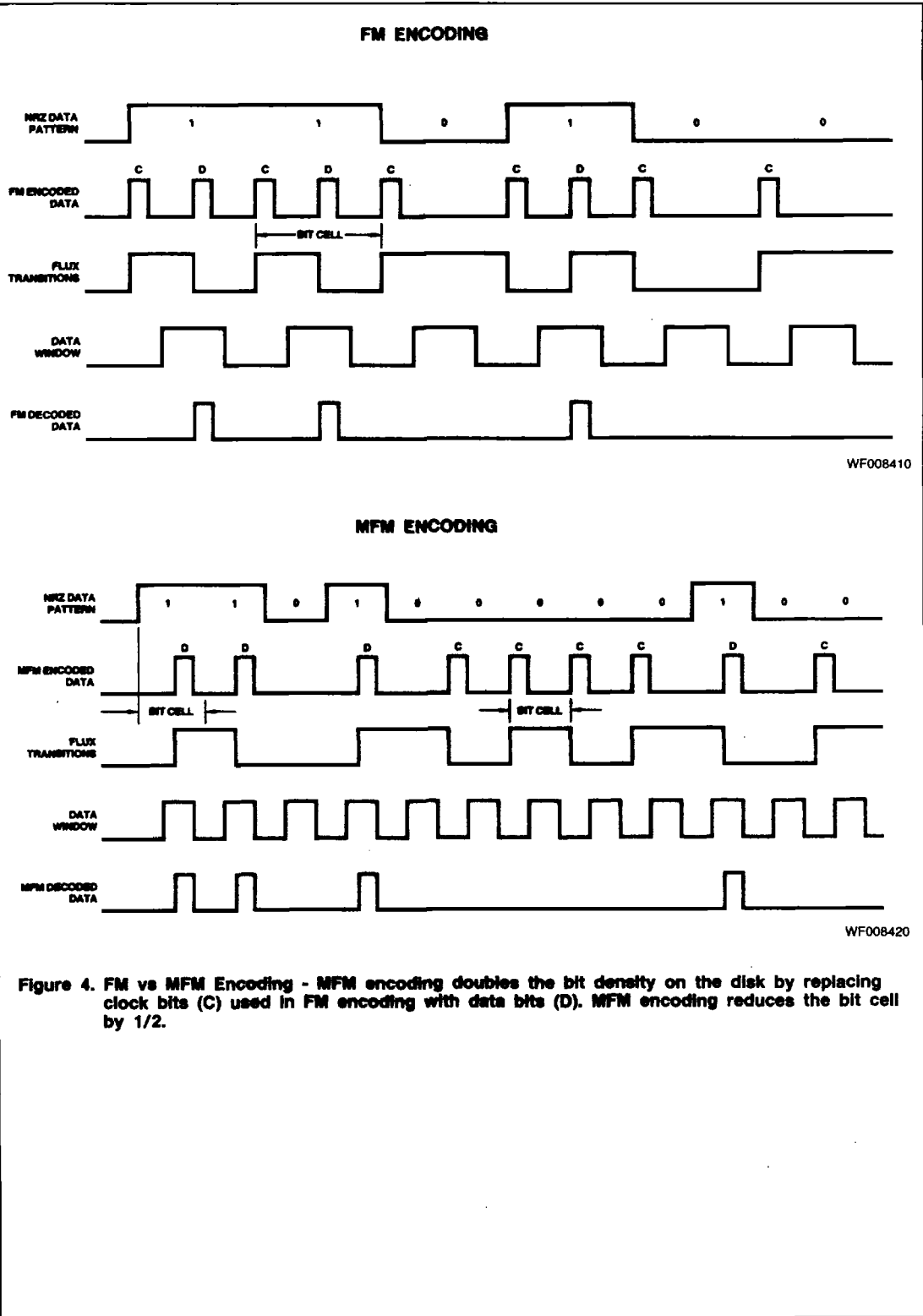
Each sector on the disk contains several Address Marks. These enable the controller to identify sector types, sector numbers, and data fields. So that the Address Marks are unique and always distinguishable from all possible data patterns, the encoding rules (either for FM or MFM) are deliberately violated when an Address Mark is written. This is done by deleting some of the clock bits in the encoded clock/data pattern. When a sector is read back from the disk, these missing clocks are identified, and then the controller is assured that correct synchronization has taken place. The DDS will generate all the standard IBM Address Marks for floppy (IBM format) and Winchester (ST506/SA1000 formats). AMC (ADDRESS MARK CONTROL) is sampled on the rising edge of WTCLK when a WRITE operation is taking place. An Address Mark is then inserted, AMF (ADDRESS MARK FOUND) is brought HIGH in acknowledgement.

The type of Address Mark generated is dependent on FAM_0 , FAM_1 , and the operating mode, i.e., floppy or hard, and single or double density. The type of Address Mark selected is listed in Table 1.



WF008391

Figure 3. Floppy Timing Sequence



The different Address Marks listed below are formed by combinations of the Hexadecimal Data and Clock Patterns.

SINGLE DENSITY FLOPPY

TYPE	Data Pattern	Clock Pattern	Number of Bytes
IXAM	FC	D7	1
IDAM	FE	C7	1
DAM	FB	C7	1
DDAM	F8	C7	1

DOUBLE DENSITY FLOPPY*

TYPE	Data Pattern	Clock Pattern	Number of Bytes
IXAM	C2	14	3
DAM and IDAM	A1	0A	3

HARD DISK*

TYPE	Data Pattern	Clock Pattern	Number of Bytes
DAM and IDAM	A1	0A	1

*Note: The ID Address Marks and Data Address mark for double density floppy and hard disks are normally qualified by an extra byte following the Address Mark. However, these extra bytes are normally encoded (no missing clocks), which the controller can easily detect during a READ operation.

Write Pre-Compensation

Bit shifting is a phenomenon caused by the flux changes stored on the disk interacting with each other. Its effect is to make nearby flux changes move away from each other, creating a timing uncertainty which can cause errors when data is read. This phenomenon is much worse on the inside tracks of a disk because the flux changes are closer together. To overcome this data interaction, the WRITE DATA stream is pre-compensated; i.e., the direction of each bit shift is anticipated and the bit is moved in the other direction by the Am9581 before being written. When PCEN is HIGH, pre-compensation is enabled and each bit will be made either EARLY, NOMINAL, or LATE, depending on its interaction with its neighbors. (In FM mode PCEN has no effect.) The amount of time shift between NOMINAL and LATE is set by two external resistors on the PCDLY pins. The pre-compensation is shown in Figure 5.

For RLL codes, NRZ to RLL encoding, write pre-compensation and address mark detection have to be performed by an external circuit.

Read Section

The read section of Am9581 consists of a data Phase-Locked-Loop (PLL), Window Logic, Sync Field Detector, Address Mark Detector, MFM/FM Decoder, Synchronized Multiplexer, crystal controlled oscillator, a reference PLL, and a divide by N counter as shown in Figure 1.

Data Phase-Locked-Loop (PLL)

The main function of the data PLL is to provide a clock signal (shown as 2f in Figure 1) that closely tracks the FM/MFM serial data read off the disk. The 2f signal is then used by the window logic to generate clock and data windows.

When the chip is in the write mode (WG active), the data PLL is synchronized to the REFCLK derived from the XTAL oscillator and the reference PLL. When the data is read from the disk (RG active), the data PLL is locked to the data stream from the disk.

The Window Logic

The main function of the window logic is to generate clock and data windows using the 2f signal provided by the data PLL. When the Read Gate (RG) is asserted, the window logic assigns clock and data windows arbitrarily.

The Sync Field Detector

The sync field detector looks for the sync field consisting of 8 consecutive pulses in clock windows. When this pattern is detected, the COUNT 8 signal is activated, freezing the window polarity. If the sync pattern is not found, the window logic flips the window polarities so that the sync detector can continue to look for the sync pattern. The apparent sync field ending is seen as a pulse in the data window. This action arms an address mark time out; i.e., after 8 bit cells (or 24 for double density floppy) an address mark must be found or the state machine is reset back to the lowest level of search - looking for 8 apparent zeros.

Address Mark Detector

The detection of various address marks for floppies and hard disks is performed by this section. The type of address mark to be detected is determined by the signals S/D, F/H, FAM₀ and FAM₁ as shown in Table 1. In response to an active AMC, AMF will be asserted to indicate that the desired address mark has been found during a read, or an appropriate address mark has been written during a write. FDDAM is asserted in the FM floppy mode upon detection of a floppy deleted data address mark during a read.

MFM/FM Decoder

The MFM/FM decoder converts the incoming MFM/FM data to NRZ data. If an MFM/FM pulse occurs in a data window, the NRZ data is decoded as a "1." If no pulse occurs in the data window, the NRZ data is decoded as a "0."

SYNC MUX

The SYNC MUX is a synchronized multiplexer that outputs either the REFCLK derived from the XTAL oscillator and the reference PLL or the RDCLK derived from disk data. The multiplexer outputs REFCLK while writing and also while reading until a sync field has been detected. Once the sync is detected, it switches over to RDCLK without any glitches. For RLL hard disks, the output is always REFCLK.

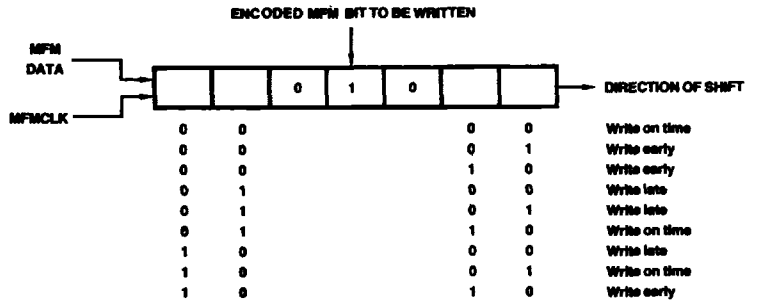
XTAL Oscillator, Reference PLL and Divide by N Counter

The XTAL oscillator, the reference PLL and the divide by N counter provide REFCLK to the SYNC MUX. The clock is also used in the data PLL to prevent VCO from drifting off from the center of its tuning range while it is not reading data off the disk. The appropriate divide ratio is selected internally as shown in Table 1.

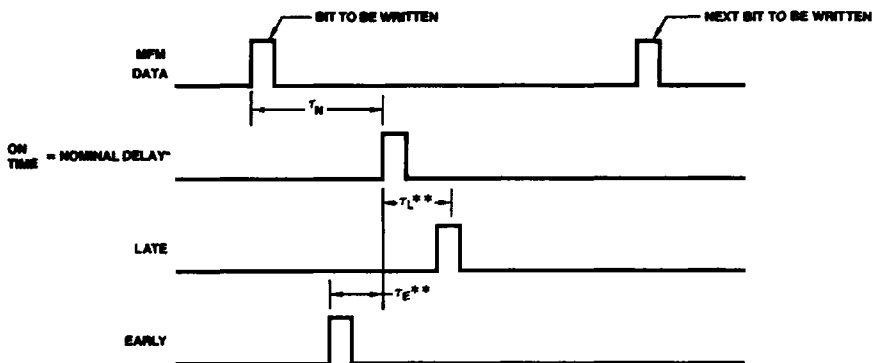
WRITE PRE-COMPENSATION

Pre-compensation is for the MFM case only. FM does not require pre-compensation. The bit to be written is shifted early

or late with respect to a nominal delay. The nominal delay is selected when data is to be written on time. Action to be taken is made by examining a 7-bit register.



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Figure 5.

*Nominal delay = τ_N
 ** $\tau_L = \tau_E = 1\% - 20\%$ bit cell time

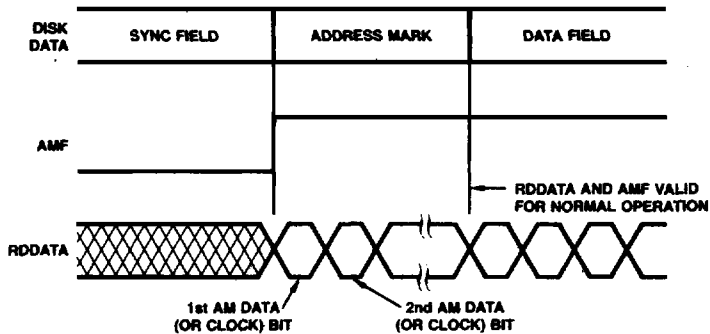
TABLE 1.

F/H	PCEN/S(D)	FAM ₁	FAM ₀	Address Mark Selected	Mode	XTAL FREQ
1	1	0	0	Index (IXAM)	FM Floppy	
1	1	0	1	ID (IDAM)	FM Floppy	
1	1	1	0	Data (DAM)	FM Floppy	32 x Bit Rate FREQ
1	1	1	1	Deleted Data (DDAM)	FM Floppy	
1	0	0	0	Index (IXAM)	MFM Floppy	
1	0	1	0	ID or Data	MFM Floppy	16 x Bit Rate FREQ
0	X	0	0	Normal A1 Address Mark	MFM Hard Disk	Bit Rate FREQ
0	X	1	1	Any Apparent Address Mark	Dump Clock** - Hard Disk	Bit Rate FREQ
0	X	1	0	None	RLL Hard Disk	Code Rate FREQ*
0	X	0	1	Any Apparent Address Mark	Dump Data - Hard Disk	Bit Rate FREQ
1	0	0	1	Any Apparent Address Mark	Dump Data - Floppy Disk	16 x Bit Rate FREQ
1	0	1	1	Any Apparent Address Mark	Dump Clock - Floppy Disk	16 x Bit Rate FREQ

*Code Rate Frequency = "2f" frequency of PLL.

**Dump is a mode whereby data (or clock) is passed to the HDC on an apparent START of Address Mark (end of apparent SYNC field). This is to enable the recovery of sectors which could not otherwise be read due to corruption of the Address Mark.

DUMP MODE



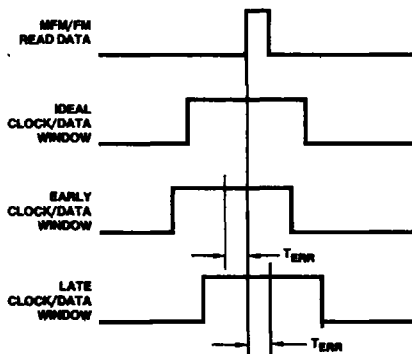
WF008480

TABLE 2. DATA PHASE LOCKED-LOOP SPECIFICATIONS

Supply Voltage	+5V = 10%
Operating Temperature Range	0 to 70°C (Plastic DIP)
Acquisition Time*	16x1/f _D seconds MAX
Capture Range*	±6% of f _D MIN
Decode Window Error*	±2.5ns or ±2% of 1/f _D , MAX whichever larger

*f_D = bit rate frequency

TABLE 3.



WF008490

DECODE WINDOW ERROR

*Note: f_D = bit rate frequency

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 to +150°C
Supply Voltage to Ground	
Potential Continuous	-0.5 to +7.0V
DC Voltage Applied to Outputs	
for High Output State	-0.5V to +V _{CC}
DC Input Voltage	-0.5 to +7.0V
DC Output Current into Outputs	30mA
DC Input Current	-30 to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Am9581**ELECTRICAL CHARACTERISTICS**

The following conditions apply unless otherwise specified:

COM'L T_A = 0 to +70°C V_{CC} = 5.0V ± 10% (MIN = 4.50V, MAX = 5.50V)

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V _{OH}	Output HIGH Voltage	V _{CC} = MIN, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -1mA (Note 6)	2.4			Volts
V _{OL}	Output LOW Voltage	V _{CC} = MIN, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 4mA (Mil), 8mA (Com'l) (Note 6) I _{OL} = 48mA (Note 5)			0.5	Volts
V _{IH}	Input HIGH Level	Guaranteed Input HIGH Voltage for All Inputs, Note 7		2.0			Volts
V _{IL}	Input LOW Level	Guaranteed Input LOW Voltage for All Inputs, Note 7				0.8	Volts
V _I	Input Clamp Voltage	V _{CC} = MIN, I _{IN} = -18mA				-1.2	Volts
I _{IL}	Input LOW Current	V _{CC} = MAX, V _{IN} = 0.5V	(Note 7)			-0.4	mA
I _{IH}	Input HIGH Current	V _{CC} = MAX, V _{IN} = 2.4V	(Note 7)			20	μA
I _I	Input HIGH Current	V _{CC} = MAX, V _{IN} = 5.5V	(Note 7)			1.0	mA
I _O	Off-State (High-Impedance) Output Current	V _{CC} = MAX	V _O = 0.4V V _O = 2.4V			-50 50	μA
I _{SC}	Output Short Circuit Current (Note 3)	V _{CC} = MAX	(Note 6)	-15		-50	mA
I _{CC}	Power Supply Current (Note 4)	V _{CC} = MAX	0 to +70°C		TBD	TBD	mA
V _{t+}	Positive Going Threshold Voltage		Note 8		1.6		Volts
V _{t-}	Negative Going Threshold Voltage		Note 8		0.8		Volts
V _H	Hysteresis		Note 8		0.8		Volts

- Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
 2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
 4. All tristate outputs are in the high-impedance state.
 5. SEL₀ - SEL₃ outputs only. These have resistor-pullups.
 6. All outputs except SEL₀ - SEL₃.
 7. Logic inputs. (Does not include X₁, X₂, PCDLY1, PCDLY2, CFIL, HDLDDLY, $\overline{\text{DACK}}_0$ - $\overline{\text{DACK}}_3$, READY, FAULT, SEEKCOMP.)
 8. Schmitt-trigger inputs only ($\overline{\text{DACK}}_0$ - $\overline{\text{DACK}}_3$, READY, FAULT, SEEKCOMP).

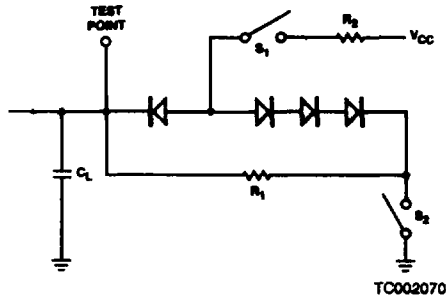
OPERATING RANGES

Part Number	T _A	V _{CC}	V _{SS}
Am9581 DC	0°C to 70°C	5V ± 10%	0V
Am9581 LC	0°C to 70°C	5V ± 10%	0V

Operating ranges define those limits over which the functionality of the device is guaranteed.

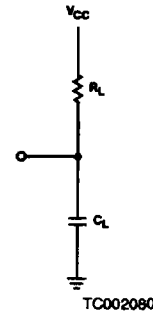
SWITCHING CHARACTERISTICS

THREE-STATE OUTPUTS



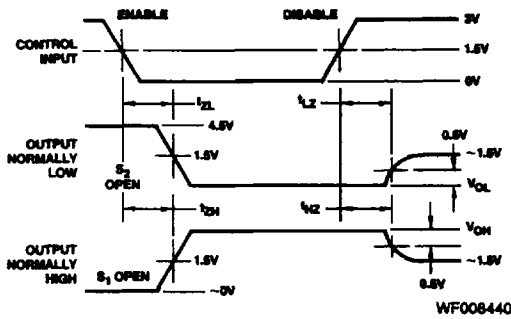
C_L , R_1 , R_2 to be determined.
All diodes 1N916 or 1N3064.

$\overline{SEL}_0 - \overline{SEL}_3$ OUTPUTS



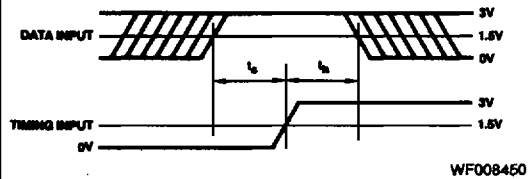
R_L , C_L to be determined.

ENABLE AND DISABLE TIMES

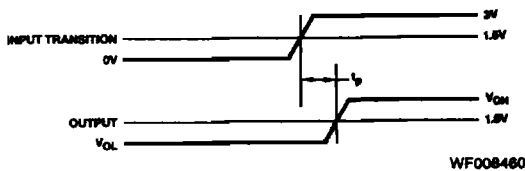


Notes: 1. Diagram shown for input control Enable-Low and input control Disable-High.
2. S_1 and S_2 of load circuit are closed except where shown.

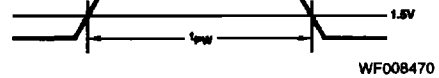
SET-UP AND HOLD TIME MEASUREMENTS



PROPAGATION DELAY MEASUREMENTS



PULSE WIDTH MEASUREMENTS



Am9581 DDS READ/WRITE SECTION TIMING

No.	Parameters	Description	Min	Typ	Max	Units
READ						
1	t _{RRH}	RD/REFCLK HIGH Time*		0.5T		ns
2	t _{RRL}	RD/REFCLK LOW Time*		0.5T		ns
3	t _{RRC}	RD/REFCLK Cycle Time*		T		ns
4	t _{RGDW}	RG ↓ to RG ↑ DWELL Time*		2T		ns
5	t _{RRAMF}	RD/REFCLK ↑ to AMF ↓ Delay		10		ns
6	t _{AMCAMFL}	AMC ↓ to AMF ↓ Delay		25		ns
7	t _{RRRD}	RD/REFCLK ↑ to Read Data Delay		15		ns
8	t _{FAMSU}	Valid FAM to AMC ↑ Set-up		20		ns
9	t _{FAMH}	AMC ↑ to Valid FAM Hold		0		ns
10	t _{FDDAMD}	RD/REFCLK ↑ to Valid FDDAM Delay		15		ns
WRITE						
11	t _{WCH}	WTCLK HIGH Time*		0.5T		ns
12	t _{WCL}	WTCLK LOW Time*		0.5T		ns
13	t _{WCC}	WTCLK Cycle Time*		T		ns
14	t _{RGWGDW}	RG ↓ to WG ↑ DWELL*		2T		ns
15	t _{WGDW}	WG ↓ to WG ↑ DWELL*		2T		ns
16	t _{AMCWC}	AMC ↓ to WTCLK ↑ Set-up		20		ns
17	t _{AMCDW}	AMC ↓ to AMC ↑ DWELL*		2T		ns
18	t _{AMFWC}	WTCLK ↑ to AMF Delay		20		ns
19	t _{AMCAMFL}	AMC ↓ to AMF ↓ Delay		25		ns
20	t _{WDSU}	WTDATA to WTCLK ↑ Set-up		20		ns
21	t _{WDH}	WTCLK ↑ to WTDATA Hold		0		ns
22	t _{FAMSU}	Valid FAM to AMC ↑ Set-up		20		ns
23	t _{FAMH}	AMC ↑ to Valid FAM Hold		0		ns
24	t _{X1D}	X ₁ to RD/REF CLK Delay			TBD	ns
25	t _{WGHWC}	WG ↑ to WTCLK ↑ Set-up		20		ns
26	t _{WGLWC}	WG ↓ to WTCLK ↑ Hold		20		ns
27	t _{PCWCSU}	PCEN to WTCLK ↑ Set-up		-1T		ns
28**	t _{PCWCH}	PCEN to WTCLK ↑ Hold		6T		ns

* T = 1/Nominal Data Rate.

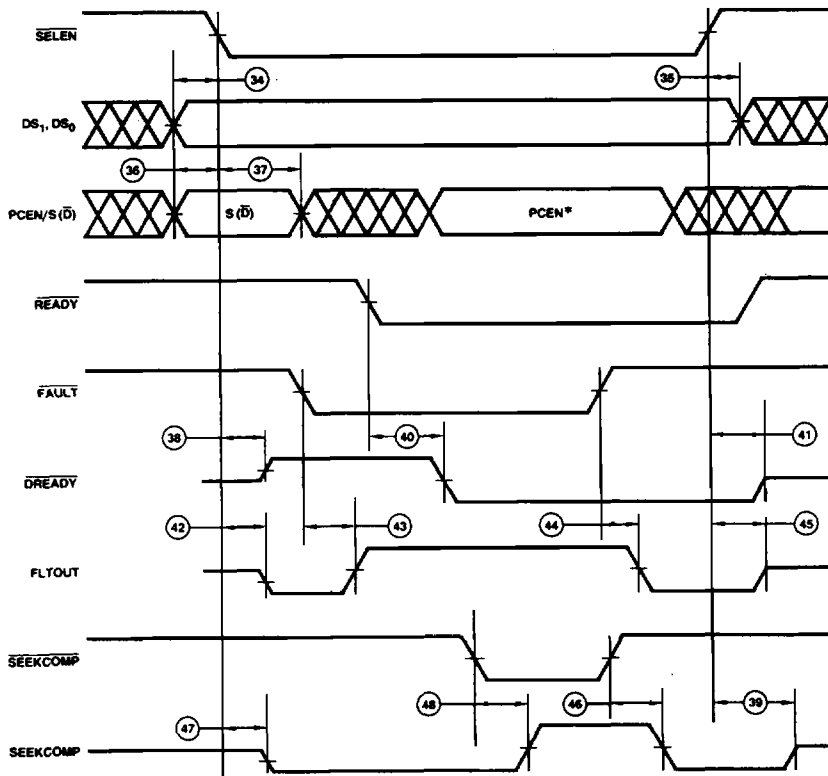
** If the data pattern remaining in the write pipeline after WG goes LOW does not need pre-compensation, PCEN can go LOW at the same time as WG.

Am9581 DDS SELECT TIMING

No.	Parameters	Description	Min	Typ	Max	Units
30	t _{SELSU}	SEL to SELEN ↓ Set-up		0		ns
31	t _{SEHH}	SEL ↑ to SELEN ↑ Hold		0		ns
32	t _{SELD}	SELEN ↓ to SEL ↓ Delay		50		ns
33	t _{SEHD}	SELEN ↑ to SEL ↑ Delay		50		ns

Am9581 DDS CONTROL SECTION TIMING

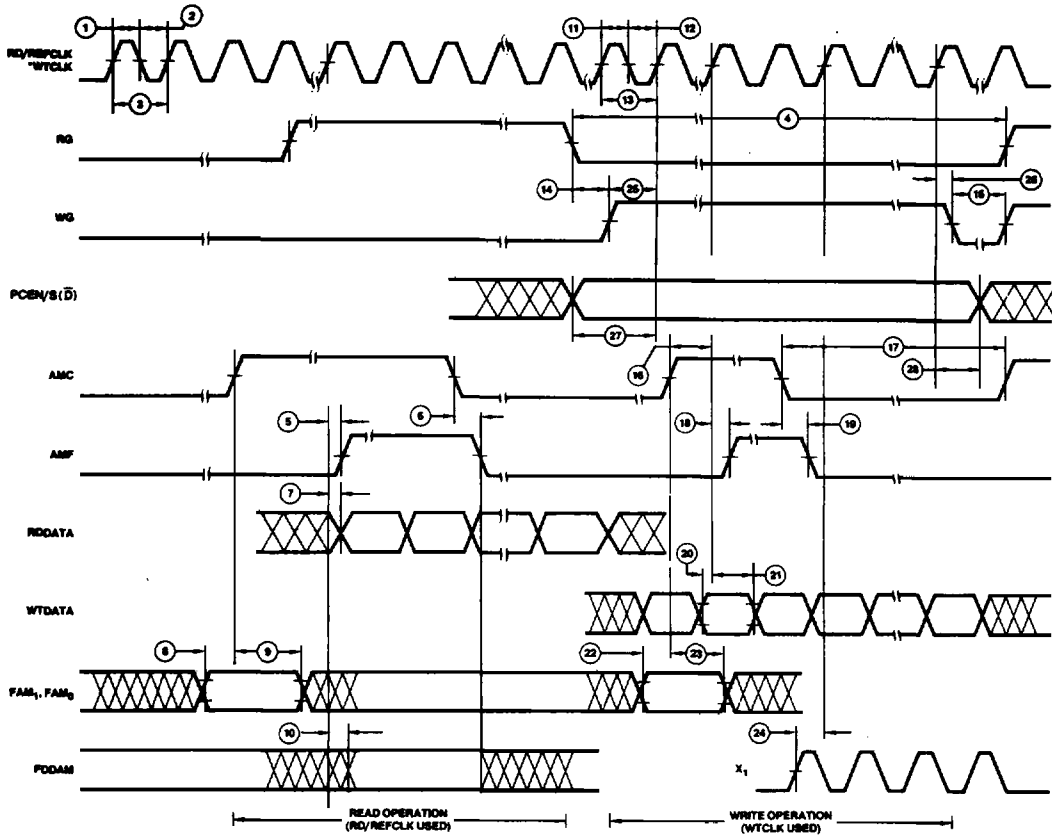
No.	Parameters	Description	Min	Typ	Max	Units
34	t _{DSSU}	DS Valid to SELEN LOW Set-up		20		ns
35	t _{DSH}	SELEN HIGH to DS Valid Hold		5		ns
36	t _{S/DSU}	S/ \bar{D} to SELEN LOW Set-up		20		ns
37	t _{S/DH}	SELEN LOW to S/ \bar{D} Hold		20		ns
38	t _{SEDR}	SELEN LOW to \bar{D} READY HIGH		50		ns
39	t _{SESCZ}	SELEN HIGH to SEEKCOMP High-Z		50		ns
40	t _{DRD}	READY LOW to \bar{D} READY LOW Delay		15		ns
41	t _{SEDRZ}	SELEN HIGH to \bar{D} READY High-Z		50		ns
42	t _{SEFL}	SELEN LOW to FLTOUT LOW Delay		50		ns
43	t _{FLFHD}	FAULT LOW to FLTOUT HIGH Delay		10		ns
44	t _{FFD}	FAULT HIGH to FLTOUT LOW Delay		10		ns
45	t _{SEFZ}	SELEN HIGH to FLTOUT High-Z		50		ns
46	t _{SCLD}	SEEKCOMP HIGH to SEEKCOMP LOW Delay		10		ns
47	t _{SCD}	SELEN LOW to SEEKCOMP LOW		50		ns
48	t _{SCHD}	SEEKCOMP LOW to SEEKCOMP HIGH Delay		10		ns



WF008432

*See WRITE section for PCEN timing requirements.

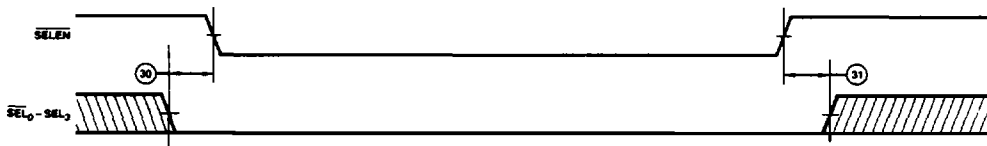
Am9581 DDS READ/WRITE SECTION TIMING



WF008502

*Note: During write operation, WTCLK is used which could be asynchronous relative to the RD/REFCLK.

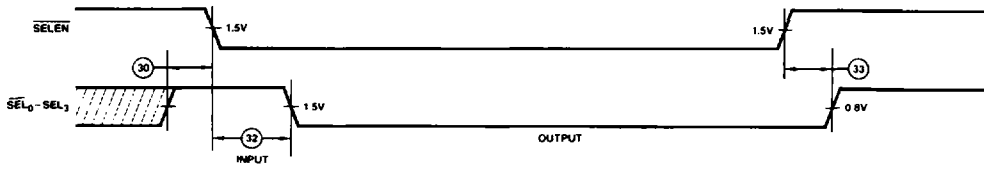
DDS NOT SELECTED



WF008510

Here a SEL line is used as an input and is held LOW. Whenever the HDC addresses the drive corresponding to this SEL pin, the DDS will tri-state all its output lines on the HDC interface.

DDS SELECTED

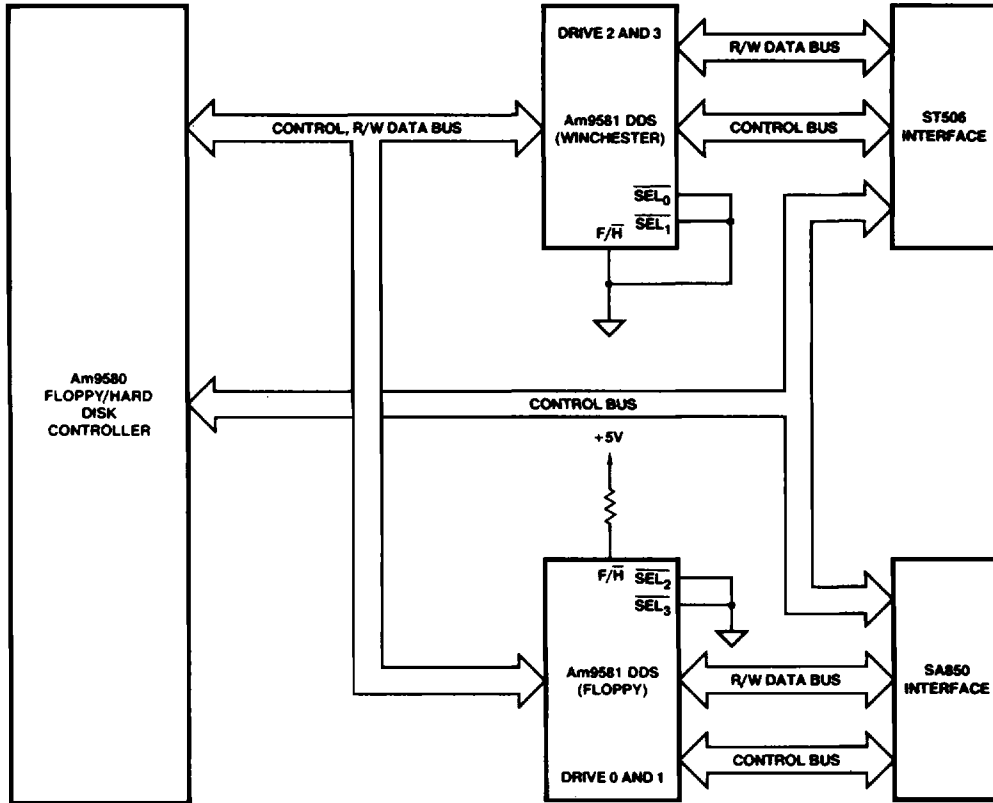


WF008520

Here the DDS causes the \overline{SEL} output corresponding to the drive selected to go LOW.

TYPICAL FLOPPY/WINCHESTER DISK DRIVE SYSTEM

2



AF003280