

## MSM3732 AS/RS

32,768-BIT DYNAMIC RANDOM ACCESS MEMORY

### GENERAL DESCRIPTION

The Oki MSM3732H/L is a fully decoded, dynamic NMOS random access memory organized as 32,768 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM3732 to be housed in a standard 16 pin DIP.

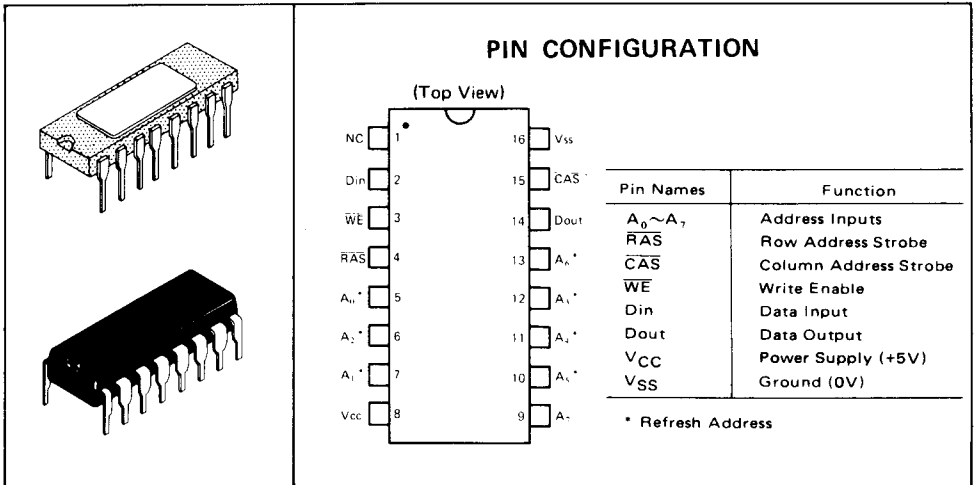
The MSM3732 is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

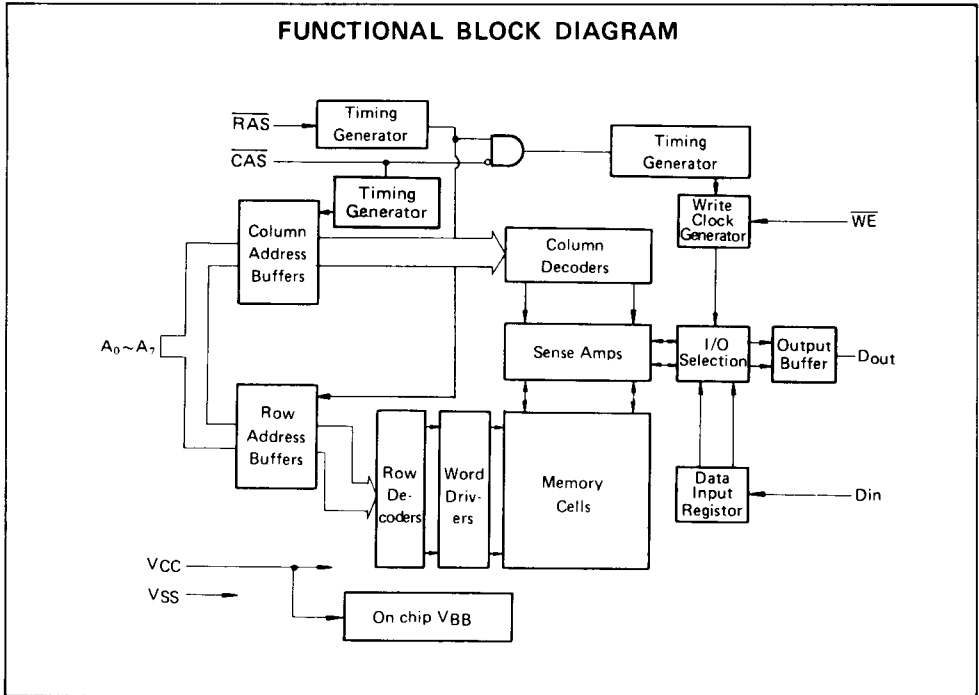
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

### FEATURES

- 32,768 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  - 150 ns max (MSM3732H/L-15)
  - 200 ns max (MSM3732H/L-20)
- Cycle time,
  - 270 ns min (MSM3732H/L-15)
  - 330 ns min (MSM3732H/L-20)
- Low power: 248 mW active, 28 mW max standby
- Single +5V Supply,  $\pm 10\%$  tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated"  $\overline{\text{CAS}}$
- 128 refresh cycles/2 ms
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write,  $\overline{\text{RAS}}$ -only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance

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### ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-1 to +7	V
Voltage on $V_{CC}$ supply relative to $V_{SS}$	$V_{CC}$	-1 to +7	V
Operating temperature	$T_{opr}$	0 to 70	°C
Storage temperature	$T_{stg}$	-55 to +150	°C
Power dissipation	$P_D$	1.0	W
Short circuit output current		50	mA

**Note:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

(Referenced to  $V_{SS}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature 0°C to +70°C
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V	
	$V_{SS}$	0	0	0	V	
Input High Voltage, all inputs	$V_{IH}$	2.4		6.5	V	
Input Low Voltage, all inputs	$V_{IL}$	-1.0		0.8	V	

## DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
Operating Current* Average power supply current ( $\overline{RAS}$ , $\overline{CAS}$ cycling; $t_{RC} = \text{min.}$ )	$I_{CC1}$		45	mA	
Standby Current Power supply current ( $\overline{RAS} = \overline{CAS} = V_{IH}$ )	$I_{CC2}$		5.0	mA	
Refresh Current* Average power supply current ( $\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$ ; $t_{RC} = \text{min.}$ )	$I_{CC3}$		35	mA	
Page Mode Current* Average power supply current ( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ cycling; $t_{PC} = \text{min.}$ )	$I_{CC4}$		42	mA	
Input Leakage Current Input leakage current, any input ( $0V \leq V_{IN} \leq 5.5V$ , all other pins not under test = $0V$ )	$I_{LI}$	-10	10	$\mu A$	
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$ )	$I_{LO}$	-10	10	$\mu A$	
Output Levels Output high voltage ( $I_{OH} = -5 \text{ mA}$ ) Output low voltage ( $I_{OL} = 4.2 \text{ mA}$ )	$V_{OH}$ $V_{OL}$	2.4	0.4	V V	

**Note\*:** ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

## CAPACITANCE

( $T_a = 25^\circ C$ ,  $f = 1 \text{ MHz}$ )

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance ( $A_0 \sim A_7$ , $D_{IN}$ )	$C_{IN1}$	4.5	5	pF
Input Capacitance ( $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ )	$C_{IN2}$	7	10	pF
Output Capacitance ( $D_{OUT}$ )	$C_{OUT}$	5	7	pF

Capacitance measured with Boonton Meter.

## AC CHARACTERISTICS

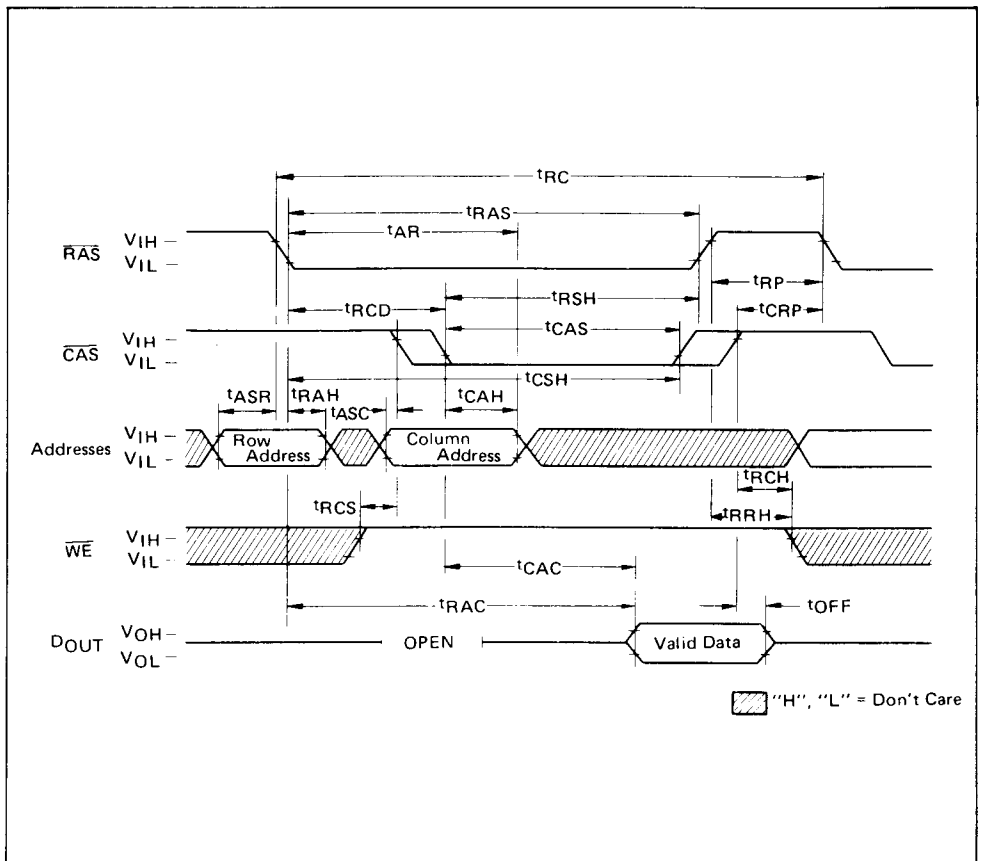
(Recommended operating conditions unless otherwise noted.)

Note 1,2,3

Parameter	Symbol	Units	MSM3732-15		MSM3732-20		Note
			Min.	Max.	Min.	Max.	
Refresh period	tREF	ms		2		2	
Random read or write cycle time	tRC	ns	270		330		
Read-write cycle time	tRWC	ns	270		330		
Page mode cycle time	tPC	ns	170		225		
Access time from RAS	tRAC	ns		150		200	4, 6
Access time from CAS	tCAC	ns		100		135	5, 6
Output buffer turn-off delay	tOFF	ns	0	40	0	50	
Transition time	tT	ns	3	35	3	50	
RAS precharge time	tRP	ns	100		120		
RAS pulse width	tRAS	ns	150	10,000	200	10,000	
RAS hold time	tRSH	ns	100		135		
CAS precharge time	tCP	ns	60		80		
CAS pulse width	tCAS	ns	100	10,000	135	10,000	
CAS hold time	tCSH	ns	150		200		
RAS to CAS delay time	tRCD	ns	25	50	30	65	7
CAS to RAS precharge time	tCRP	ns	0		0		
Row Address set-up time	tASR	ns	0		0		
Row Address hold time	tRAH	ns	15		20		
Column Address set-up time	tASC	ns	0		0		
Column Address hold time	tCAH	ns	45		55		
Column Address hold time referenced to RAS	tAR	ns	95		120		
Read command set-up time	tRCS	ns	0		0		
Read command hold time	tRCH	ns	0		0		
Write command set-up time	tWCS	ns	-10		-10		8
Write command hold time	tWCH	ns	45		55		
Write command hold time referenced to RAS	tWCR	ns	95		120		
Write command pulse width	tWP	ns	45		55		
Write command to RAS lead time	tRWL	ns	45		55		
Write command to CAS lead time	tCWL	ns	45		55		
Data-in set-up time	tDS	ns	0		0		
Data-in hold time	tDH	ns	45		55		
Data-in hold time referenced to RAS	tDHR	ns	95		120		
CAS to WE delay	tCWD	ns	60		80		8
RAS to WE delay	tRWD	ns	110		145		8
Read command hold time referenced to RAS	tRRH	ns	20		25		

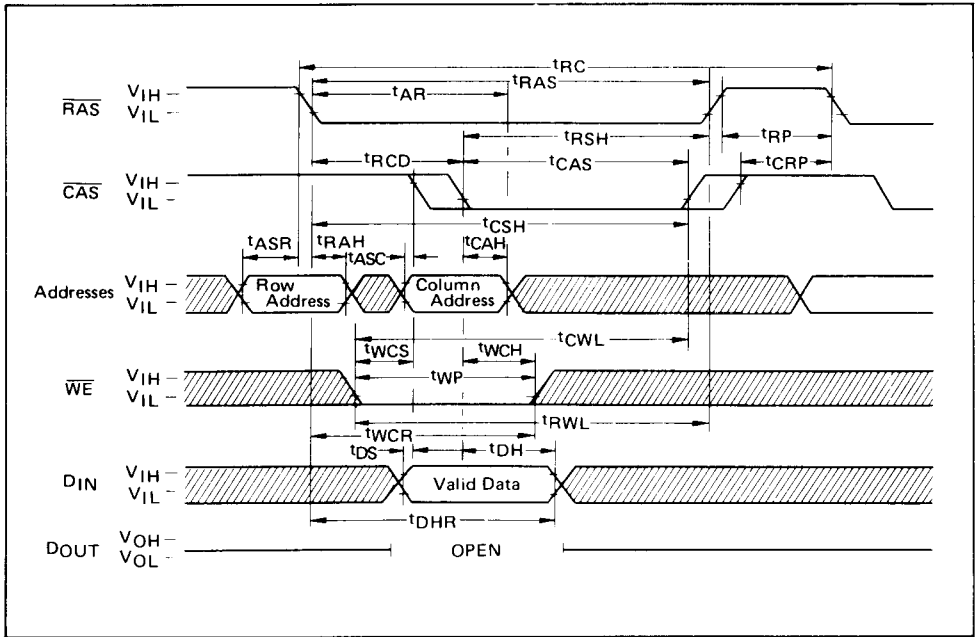
- NOTES:**
- 1) An initial pause of 100  $\mu$ s is required after power-up followed by any 8  $\overline{\text{RAS}}$  cycles (Examples;  $\overline{\text{RAS}}$  only) before proper device operation is achieved.
  - 2) AC measurements assume  $t_T = 5$  ns.
  - 3)  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
  - 4) Assumes that  $t_{RCD} < t_{RCD}(\text{max.})$ .  
If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds the value shown.
  - 5) Assumes that  $t_{RCD} < t_{RCD}(\text{max.})$
  - 6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
  - 7) Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
  - 8)  $t_{WCS}$ ,  $t_{CWD}$  and  $t_{RWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{CWD} \geq t_{CWD}(\text{min.})$  and  $t_{RWD} > t_{RWD}(\text{min.})$  the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

### READ CYCLE TIMING

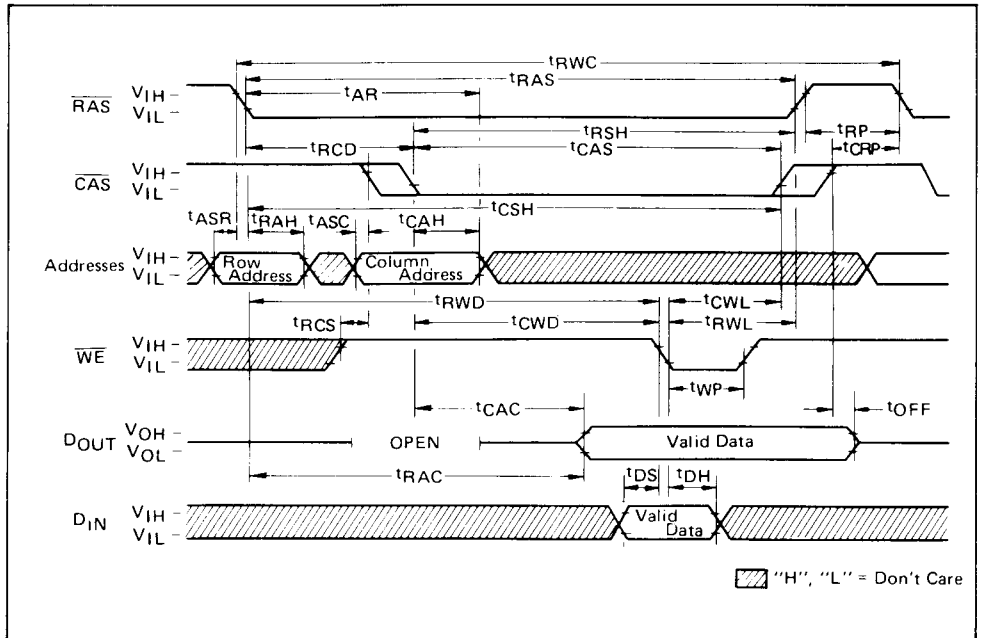


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**WRITE CYCLE TIMING**  
(EARLY WRITE)

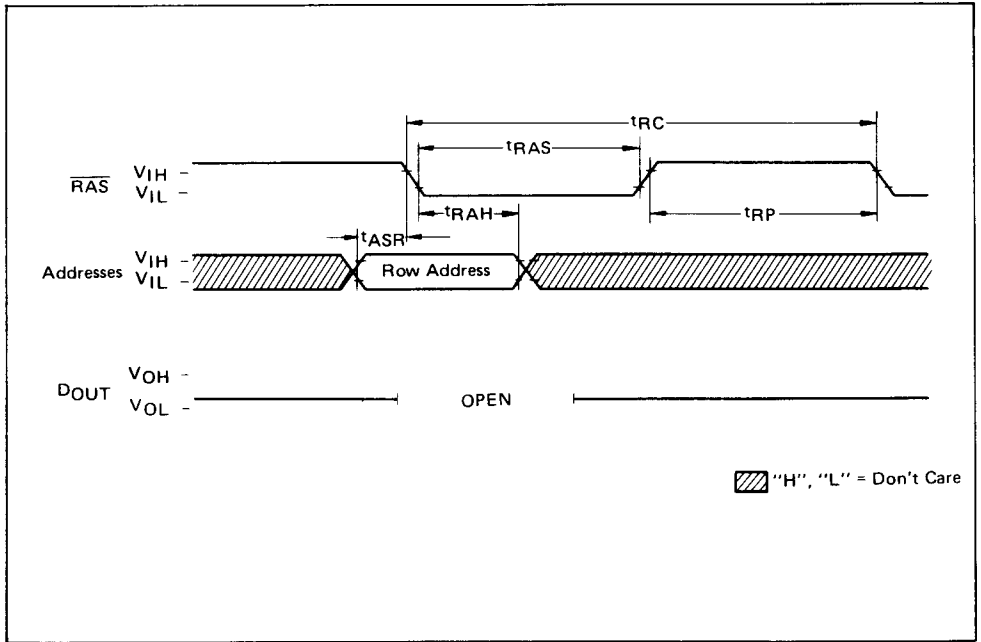


**READ-WRITE/READ-MODIFY-WRITE CYCLE**



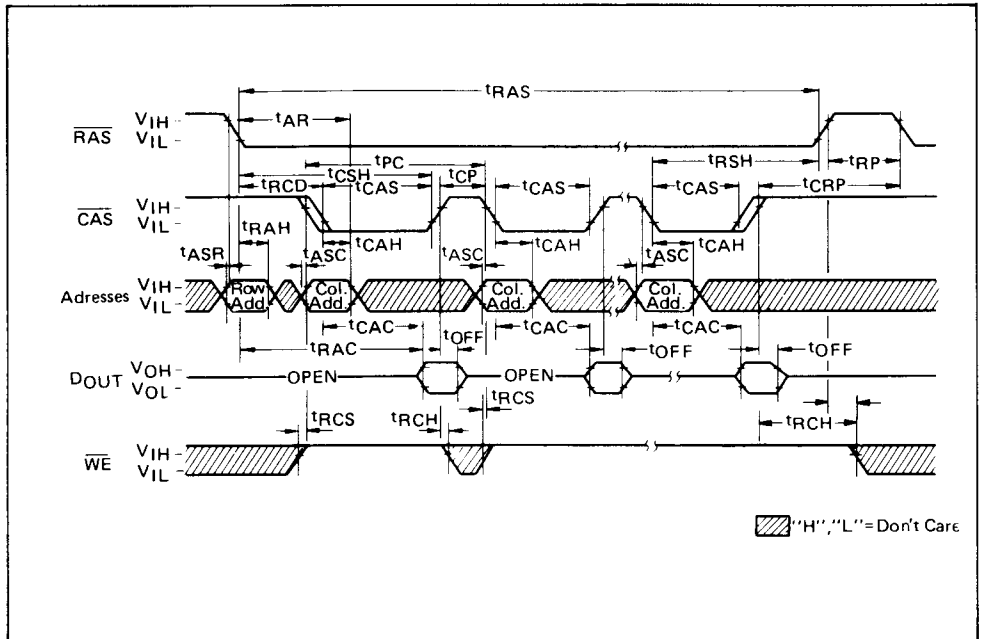
### RAS ONLY REFRESH TIMING

(CAS: V<sub>IH</sub>,  $\overline{WE}$  & D<sub>I/N</sub>: Don't care)



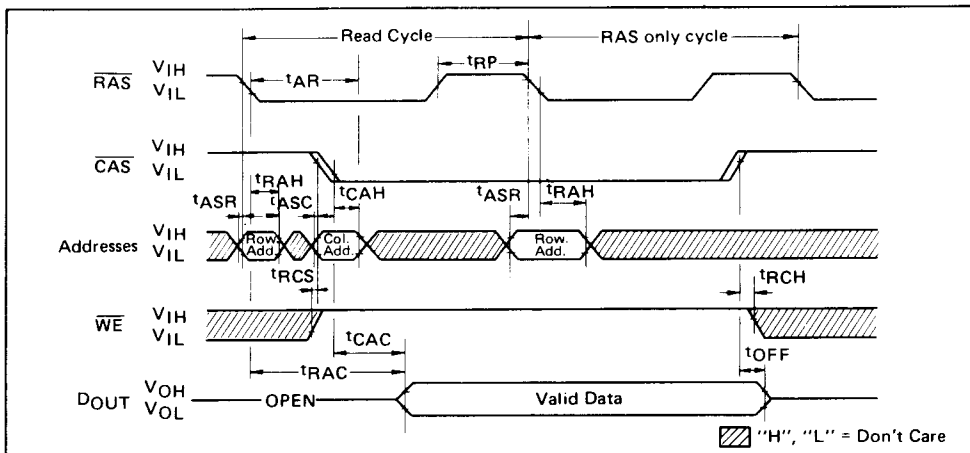
### PAGE MODE READ CYCLE

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## HIDDEN REFRESH



### DESCRIPTION

#### Address Inputs:

A total of fifteen binary input address bits are required to decode any 1 of 32,768 storage cell locations within the MSM3732. Eight row-address bits are established on the input pins ( $A_0 \sim A_7$ ) and latched with the Row Address Strobe ( $\overline{RAS}$ ). The seven column-address bits ( $A_8$  through  $A_{14}$ ) are established on the input pins and latched with the Column Address Strobe ( $\overline{CAS}$ ). All input addresses must be stable on or before the falling edge of  $\overline{RAS}$ .  $\overline{CAS}$  is internally inhibited (or "gated") by  $\overline{RAS}$  to permit triggering of  $\overline{CAS}$  as soon as the Row Address Hold Time ( $t_{RAH}$ ) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses. One Column Address ( $A_7$ ) has to be fixed at logic "0" (low level) for MSM3732L, and at logic "1" (high level) for MSM3732H.

#### Write Enable:

The read mode or write mode is selected with the  $\overline{WE}$  input. A logic high (1) on  $\overline{WE}$  dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

#### Data Input:

Data is written into the MSM3732 during a write or read-write cycle. The last falling edge of  $\overline{WE}$  or  $\overline{CAS}$  is a strobe for the Data In ( $D_{IN}$ ) register. In a write cycle, if  $\overline{WE}$  is brought low (write mode) before  $\overline{CAS}$ ,  $D_{IN}$  is strobed by  $\overline{CAS}$ , and the set-up and hold times are referenced to  $\overline{CAS}$ . In a read-write cycle,  $\overline{WE}$  will be delayed until  $\overline{CAS}$  has made its negative transition. Thus  $D_{IN}$  is strobed by  $\overline{WE}$ , and set-up and hold times are referenced to  $\overline{WE}$ .

#### Data Output:

The output buffer is three-state TTL compatible with

a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until  $\overline{CAS}$  is brought low. In a read cycle, or read-write cycle, the output is valid after  $t_{RAC}$  from transition of  $\overline{RAS}$  when  $t_{RCD}$  (max.) is satisfied, or after  $t_{CAC}$  from transition of  $\overline{CAS}$  when the transition occurs after  $t_{RCD}$  (max.). Data remain valid until  $\overline{CAS}$  is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

#### Page Mode:

Page-mode operation permits strobing the row-address into the MSM3732 while maintaining  $\overline{RAS}$  at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of  $\overline{RAS}$  is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

#### Refresh:

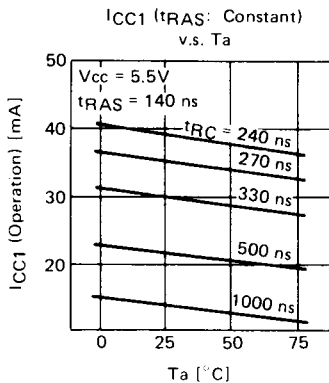
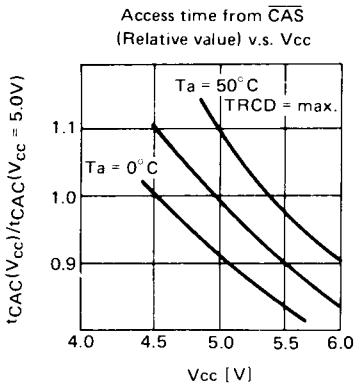
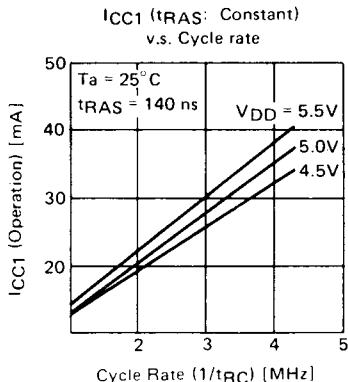
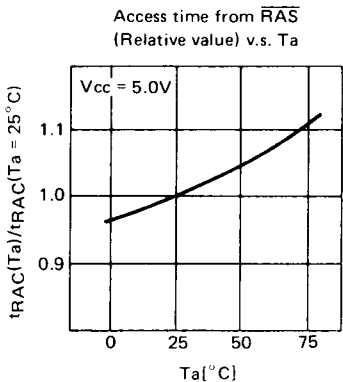
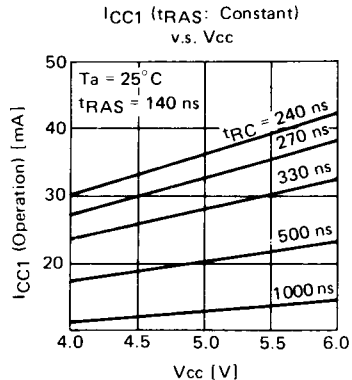
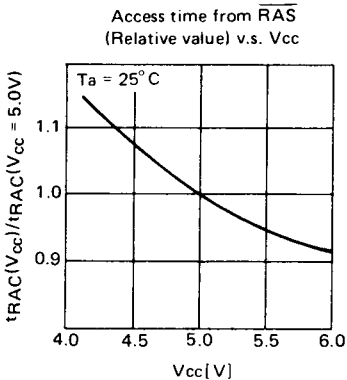
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ( $A_0 \sim A_6$ ) at least every two milliseconds. During refresh, either  $V_{IL}$  or  $V_{IH}$  is permitted for  $A_7$ .  $\overline{RAS}$  only refresh avoids any output during refresh because the output buffer is in the high impedance state unless  $\overline{CAS}$  is brought low. Strobing each of 128 row-addresses with  $\overline{RAS}$  will cause all bits in each row to be refreshed. Further  $\overline{RAS}$ -only refresh results in a substantial reduction in power dissipation.

#### Hidden Refresh:

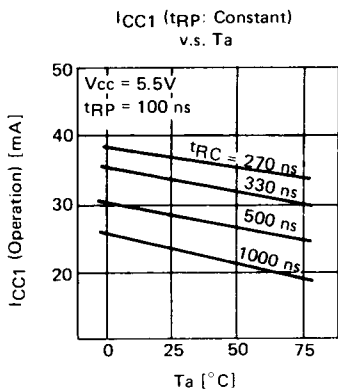
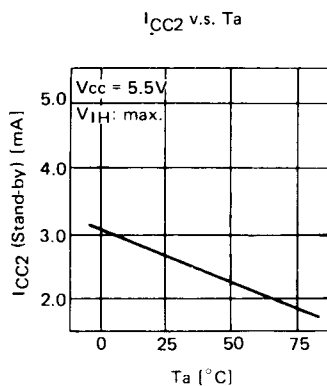
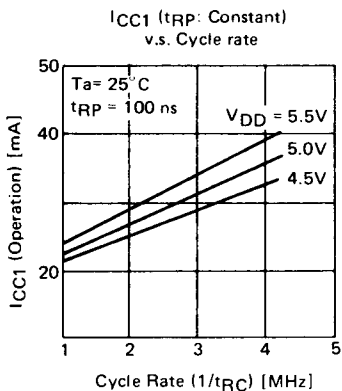
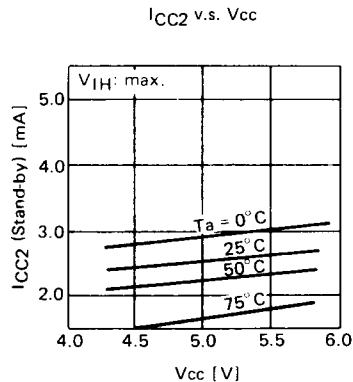
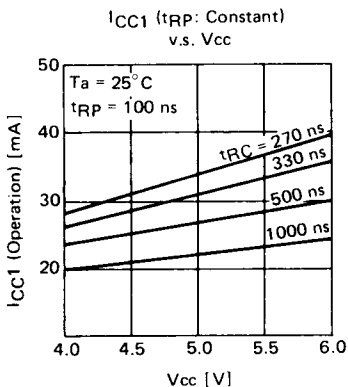
$\overline{RAS}$  ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding  $\overline{CAS}$  as  $V_{IL}$  from a previous memory read cycle.

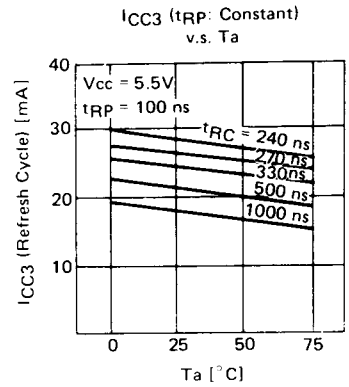
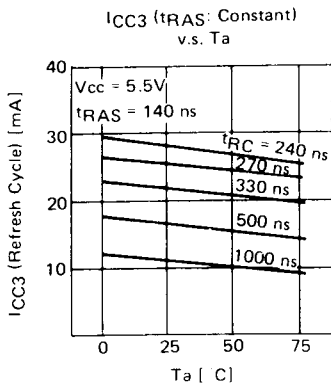
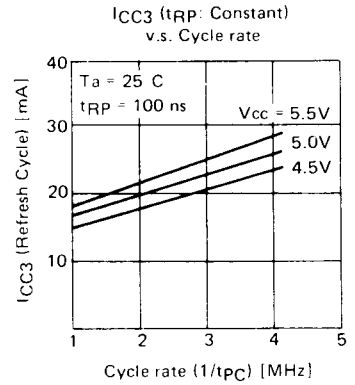
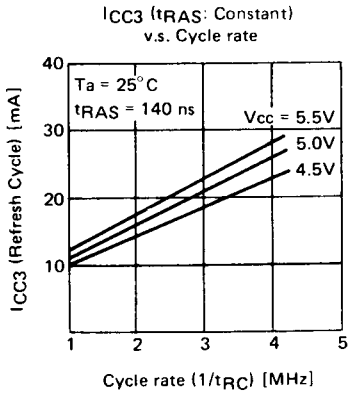
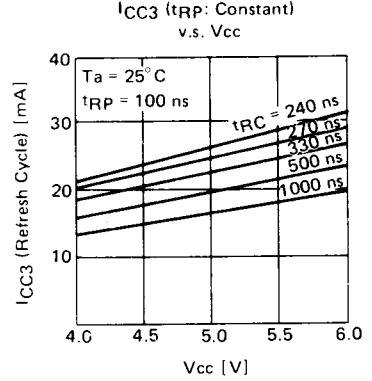
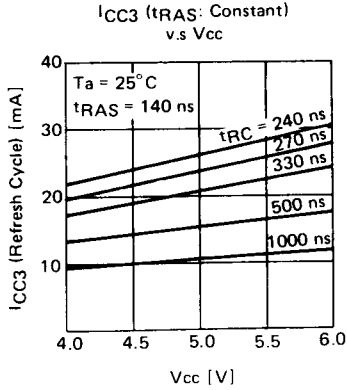
TYPICAL CHARACTERISTICS

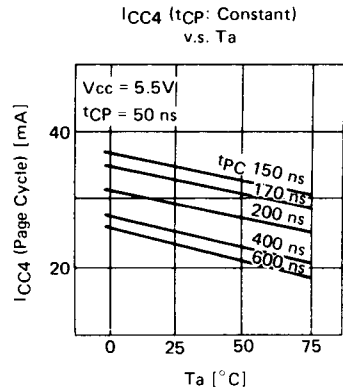
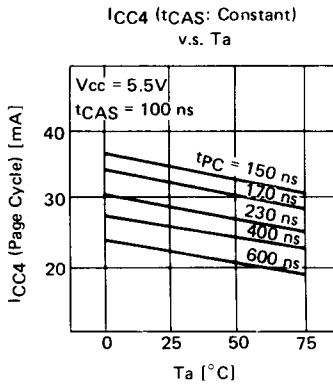
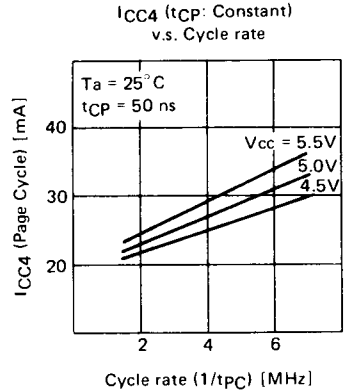
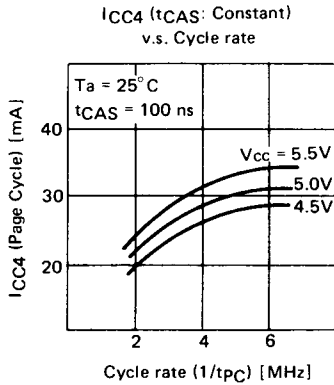
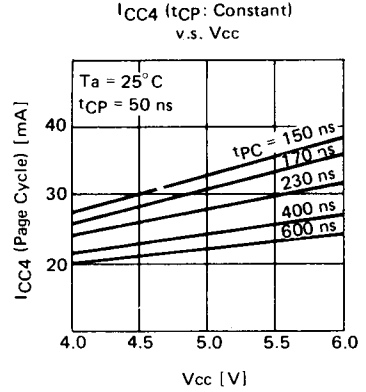
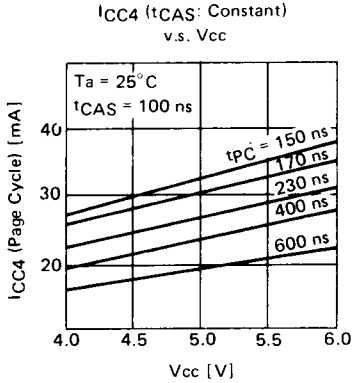


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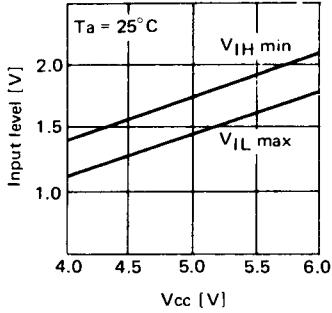
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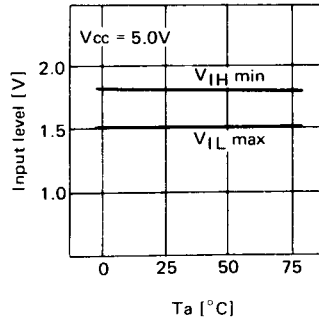


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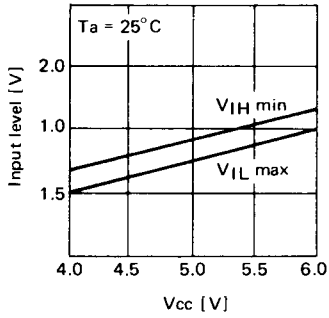
Address Input  
v.s. Vcc



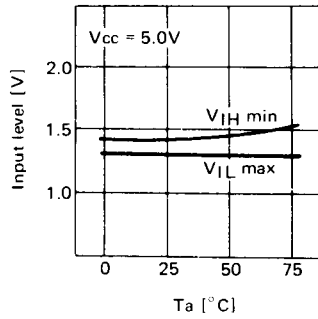
Address Input  
v.s. Ta



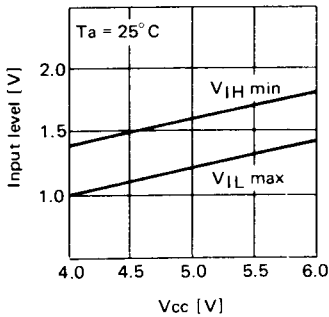
Data Input  
v.s. Vcc



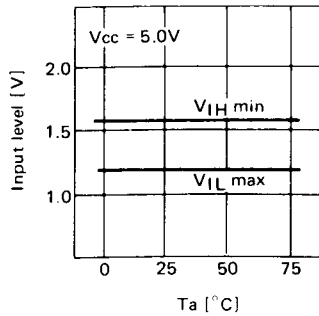
Data Input  
v.s. Ta

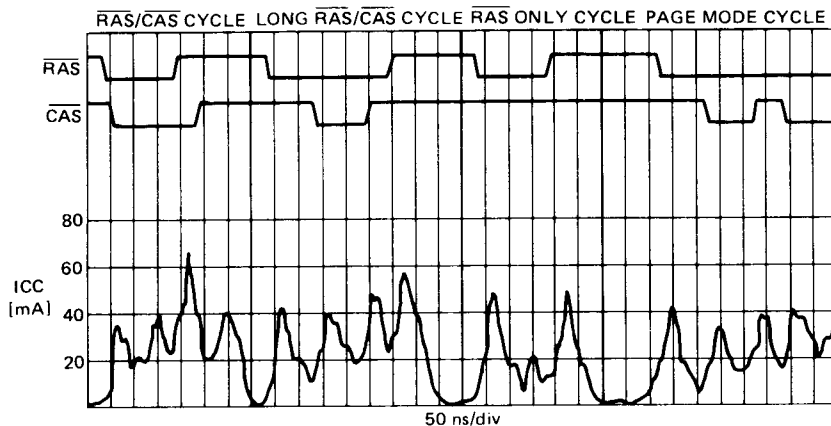


Clock Input  
v.s. Vcc



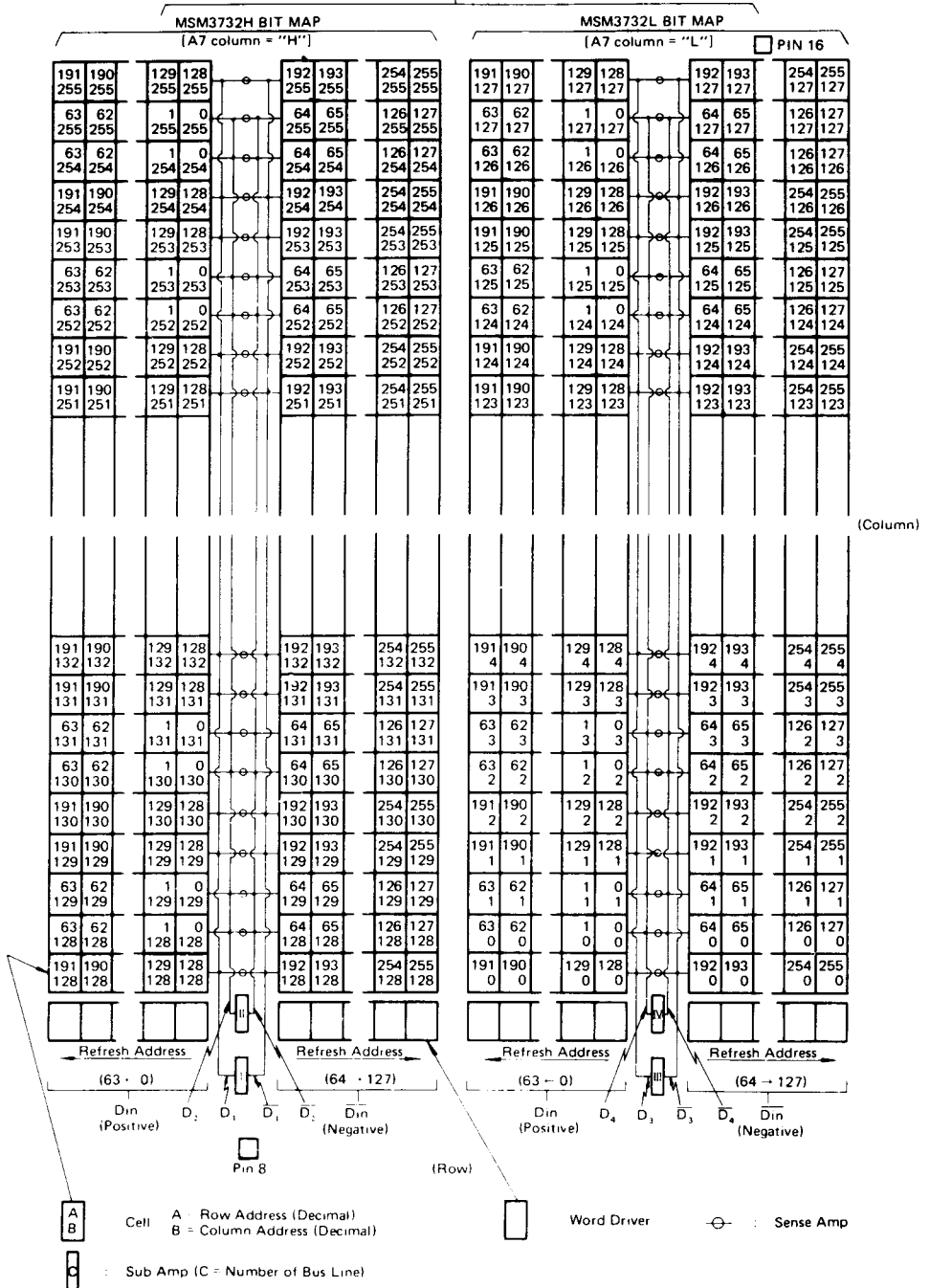
Clock Input  
v.s. Ta





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MSM3732 Bit MAP (Physical-Decimal)



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