Integrated Device Technology, Inc.

BUS-MATCHING BIDIRECTIONAL FIFO 512 x 18-BIT – 1,024 x 9-BIT 1,024 x 18-BIT – 2,048 x 9-BIT

IDT72510
IDT72520

FEATURES:

- Two side-by-side FIFO memory arrays for bidirectional data transfers
- 512 x 18-Bit – 1,024 x 9-Bit (IDT72510)
- 1,024 x 18-Bit – 2,048 x 9-Bit (IDT72520)
- 18-bit data bus on Port A side and 9-bit data bus on Port B side
- Can be configured for 18-to-9-bit, 36-to-9-bit, or 36-to-18-bit communication
- Fast 25ns access time
- Fully programmable standard microprocessor interface
- Built-in bypass path for direct data transfer between two ports
- Two fixed flags, Empty and Full, for both the A-to-B and the B-to-A FIFO
- Two programmable flags, Almost-Empty and Almost-Full for each FIFO
- Programmable flag offset can be set to any depth in the FIFO
- Any of the eight internal flags can be assigned to four external flag pins
- Flexible reread/rewrite capabilities.
- On-chip parity checking and generation
- Standard DMA control pins for data exchange with peripherals
- IDT72510 and IDT72520 available in the the 52-pin PLCC package
- Industrial temperature range (–40°C to +85°C) is available

DESCRIPTION:

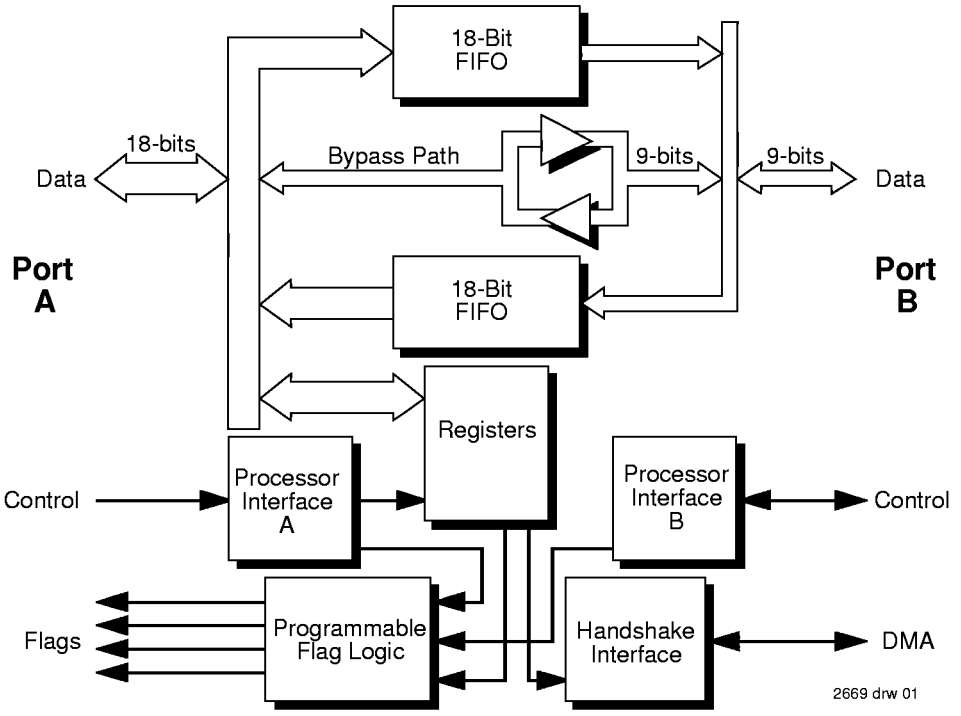
The IDT72510 and IDT72520 are highly integrated first-in, first-out memories that enhance processor-to-processor and processor-to-peripheral communications. IDT BiFIFOs integrate two side-by-side memory arrays for data transfers in two directions.

The BiFIFOs have two ports, A and B, that both have standard microprocessor interfaces. All BiFIFO operations are controlled from the 18-bit wide Port A. The BiFIFOs incorporate bus matching logic to convert the 18-bit wide memory data paths to the 9-bit wide Port B data bus. The BiFIFOs have a bypass path that allows the device connected to Port A to pass messages directly to the Port B device.

Ten registers are accessible through Port A, a Command Register, a Status Register, and eight Configuration Registers.

The IDT BiFIFOs have programmable flags. Each FIFO memory array has four internal flags, Empty, Almost-Empty, Almost-Full and Full, for a total of eight internal flags. The Almost-Empty and Almost-Full flag offsets can be set to any

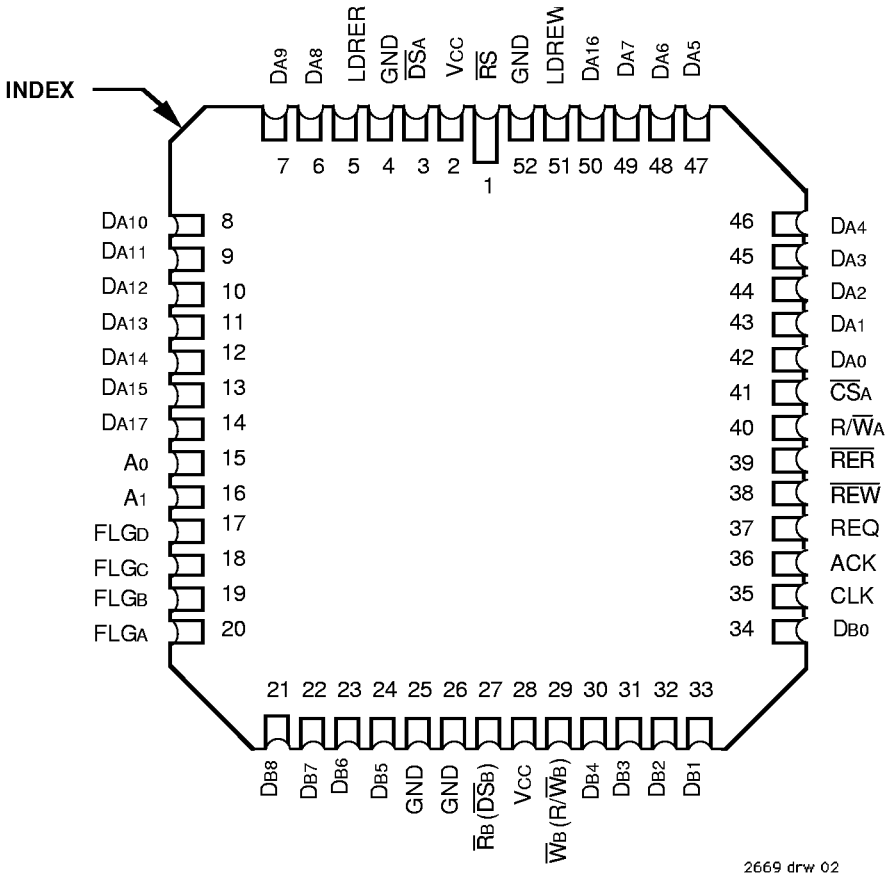
SIMPLIFIED BLOCK DIAGRAM



depth through the Configuration Registers. These eight internal flags can be assigned to any of four external flag pins (FLGA-FLGD) through one Configuration Register.

Port B has parity, reread/rewrite and DMA functions. Parity generation and checking can be done by the BiFIFO on data passing through Port B. The Reread and Rewrite controls will read or write Port B data blocks multiple times. The BiFIFOs have three pins, REQ, ACK and CLK, to control DMA transfers from Port B devices.

PIN CONFIGURATION



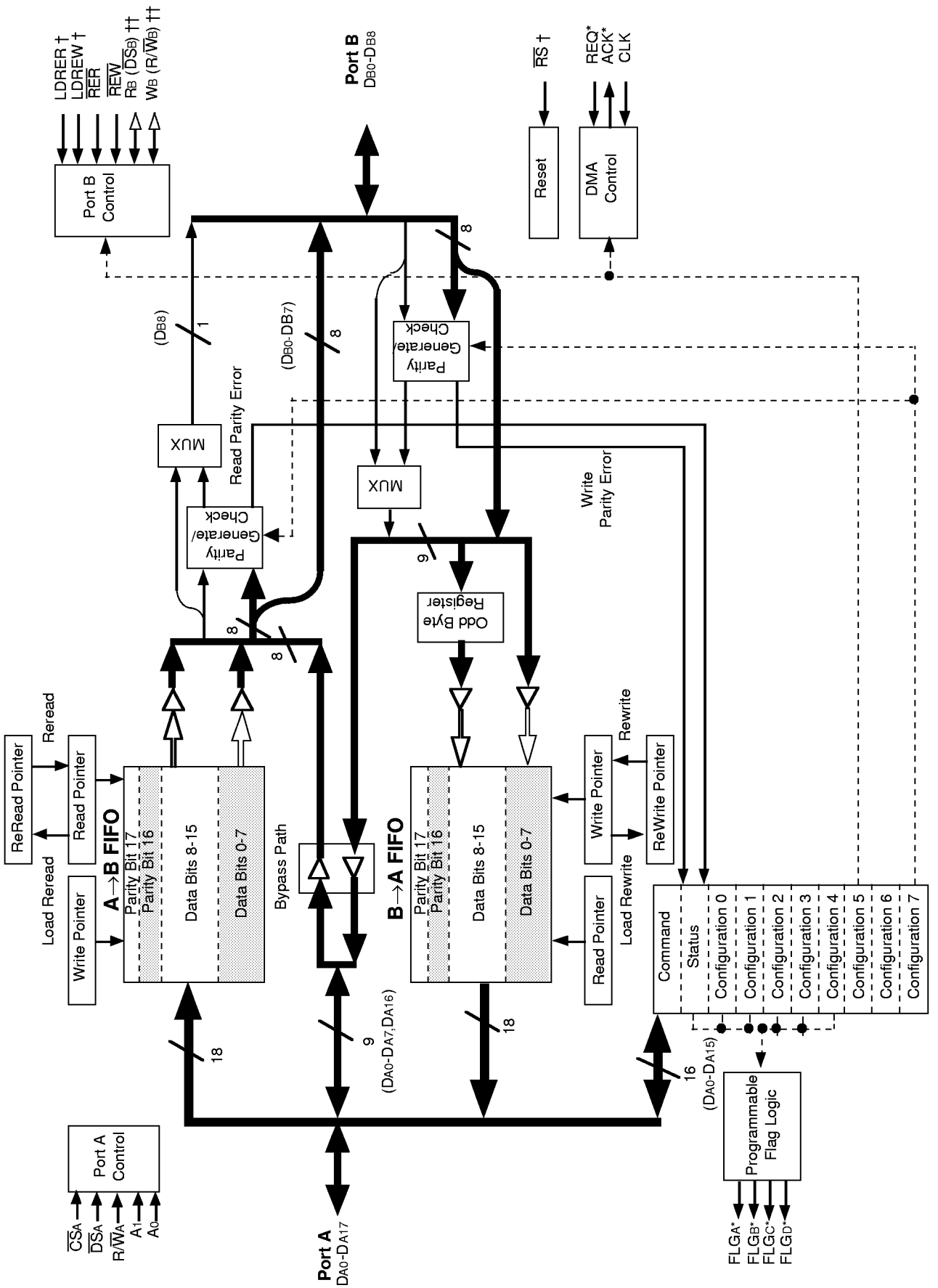
PLCC (J52-1, order code: J)
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
DA0-DA15	Data A	I/O	Data inputs and outputs for 16 bits of the 18-bit Port A bus.
DA16-DA17	Parity A	I/O	DA16 is the parity bit for DA0-DA7. DA17 is the parity bit for DA8-DA15. DA16 and DA17 can be used as two extra data bits if the parity generate function is disabled.
$\overline{CS}$A	Chip Select A	I	Port A is accessed when Chip Select A is LOW.
$\overline{DS}$A	Data Strobe A	I	Data is written into Port A on the rising edge of Data Strobe when Chip Select is LOW. Data is read out of Port A on the falling edge of Data Strobe when Chip Select is LOW.
R/$\overline{W}$A	Read/Write A	I	This pin controls the read or write direction of Port A. When $\overline{CS}$A is LOW and R/$\overline{W}$A is HIGH, data is read from Port A on the falling edge of $\overline{DS}$A. When $\overline{CS}$A is LOW and R/$\overline{W}$A is LOW, data is written into Port A on the rising edge of $\overline{DS}$A.
A0, A1	Addresses	I	When Chip Select A is asserted, A0, A1, and Read/Write A are used to select one of six internal resources.
DB0-DB7	Data B	I / O	Data inputs and outputs for 8 bits of the 9-bit Port B bus.
DB8	Parity B	I / O	DB8 is the parity bit for DB0-DB7. DB8 can be used as a data bit if the parity generate function is disabled.
$\overline{R}$B ($\overline{DS}$B)	Read B	I or O	If Port B is programmed to processor mode, this pin functions as an input. If Port B is programmed to peripheral mode this pin functions as an output. This pin can function as part of an Intel-style interface ($\overline{R}$B) or as part of a Motorola-style interface ($\overline{DS}$B). As an Intel-style interface, data is read from Port B on a falling edge of $\overline{R}$B. As a Motorola-style interface, data is read on the falling edge of $\overline{DS}$B or written on the rising edge of $\overline{DS}$B through Port B. The Default is Intel-style processor mode ($\overline{R}$B as an input).
$\overline{W}$B (R/$\overline{W}$B)	Write B	I or O	If Port B is programmed to processor mode, this pin functions as an input. If Port B is programmed to peripheral mode this pin functions as an output. This pin can function as part of an Intel-style interface ($\overline{W}$B) or as part of a Motorola-style interface (R/$\overline{W}$B). As an Intel style interface, data is written to Port B on a rising edge of $\overline{W}$B. As a Motorola-style interface, data is read (R/$\overline{W}$B = HIGH) or written (R/$\overline{W}$B = LOW) to Port B in conjunction with a Data Strobe B falling or rising edge. The Default is Intel-style processor mode ($\overline{W}$B as input).
$\overline{RER}$	Reread	I	Loads A-to-B FIFO Read Pointer with the value of the Reread Pointer when LOW.
$\overline{REW}$	Rewrite	I	Loads B-to-A FIFO Write Pointer with the value of the Rewrite Pointer when LOW.
LDRER	Load Reread	I	Loads the Reread Pointer with the value of the A-to-B FIFO Read Pointer when HIGH. This signal is accessible through the Command Register.
LDREW	Load Rewrite	I	Loads the Rewrite Pointer with the value of the B-to-A FIFO Write Pointer when HIGH. This signal is accessible through the Command Register.
REQ	Request	I	When Port B is programmed in peripheral mode, asserting this pin begins a data transfer. Request can be programmed either active HIGH or active LOW.
ACK	Acknowledge	O	When Port B is programmed in peripheral mode, Acknowledge is asserted in response to a Request signal. This confirms that a data transfer may begin. Acknowledge can be programmed either active HIGH or active LOW.
CLK	Clock	I	This pin is used to generate timing for ACK, $\overline{R}$B, $\overline{W}$B, $\overline{DS}$B and R/$\overline{W}$B when Port B is in the peripheral mode.
FLGA-FLGD	Flags	O	These four outputs pins can be assigned to any one of the eight internal flags in the BiFIFO. Each of the two internal FIFOs (A-to-B and B-to-A) has four internal flags: Empty, Almost-Empty, Almost-Full, and Full. If parity checking is enabled, the FLGA pin can also be assigned as a parity error output.
$\overline{RS}$	Reset	I	A LOW on this pin will perform a reset of all BiFIFO functions. Software reset can be achieved through command register.
V_{CC}	Power		There are two +5V power pins on all four devices.
GND	Ground		There are four ground pins

2669 tbl 01

DETAILED BLOCK DIAGRAM



NOTES:
(*) Can be programmed either active high or active low in internal configuration registers.
(†) Accessible through internal registers.
(††) Can be programmed through an internal configuration register to be either an input or an output.

2669 drw 03

FUNCTIONAL DESCRIPTION

IDT's BiFIFO family is versatile for both multiprocessor and peripheral applications. Data can be sent through both FIFO memories concurrently, thus freeing both processors from laborious direct memory access (DMA) protocols and frequent interrupts.

Two full 18-bit wide FIFOs are integrated into the IDT BiFIFO, making simultaneous data exchange possible. Each FIFO is monitored by separate internal read and write pointers, so communication is not only bidirectional, it is also totally independent in each direction. The processor connected to Port A of the BiFIFO can send or receive messages directly to the Port B device using the BiFIFO's 9-bit bypass path.

The BiFIFOs can be used in three different bus configurations: 18 bits to 9 bits, 36 bits to 9 bits and 36 bits to 18 bits. One BiFIFO can be used for the 18- to 9-bit configuration, and two BiFIFOs are required for 36- to 9-bit or 36- to 18-bit configurations. Bits 11 and 12 of Configuration Register 5 determine the BiFIFO configuration (see Table 11 for Configuration Register 5 format).

The microprocessor or microcontroller connected to Port A controls all operations of the BiFIFOs. Thus, all Port A interface pins are inputs driven by the controlling processor. Port B can be programmed to interface either with a second processor or a peripheral device. When Port B is programmed in processor interface mode, the Port B interface pins are inputs driven by the second processor. If a peripheral device is connected to the BiFIFOs, Port B is programmed to peripheral interface mode and the interface pins are outputs.

18- to 9-bit Configurations

A single BiFIFO can be configured to connect an 18-bit processor to another 9-bit processor or a 9-bit peripheral. Bits 11 and 12 of Configuration Register 5 should be set to **00** for a stand-alone configuration. Figures 1 and 2 show the BiFIFO in 18- to 9-bit configurations for processor and peripheral interface modes respectively.

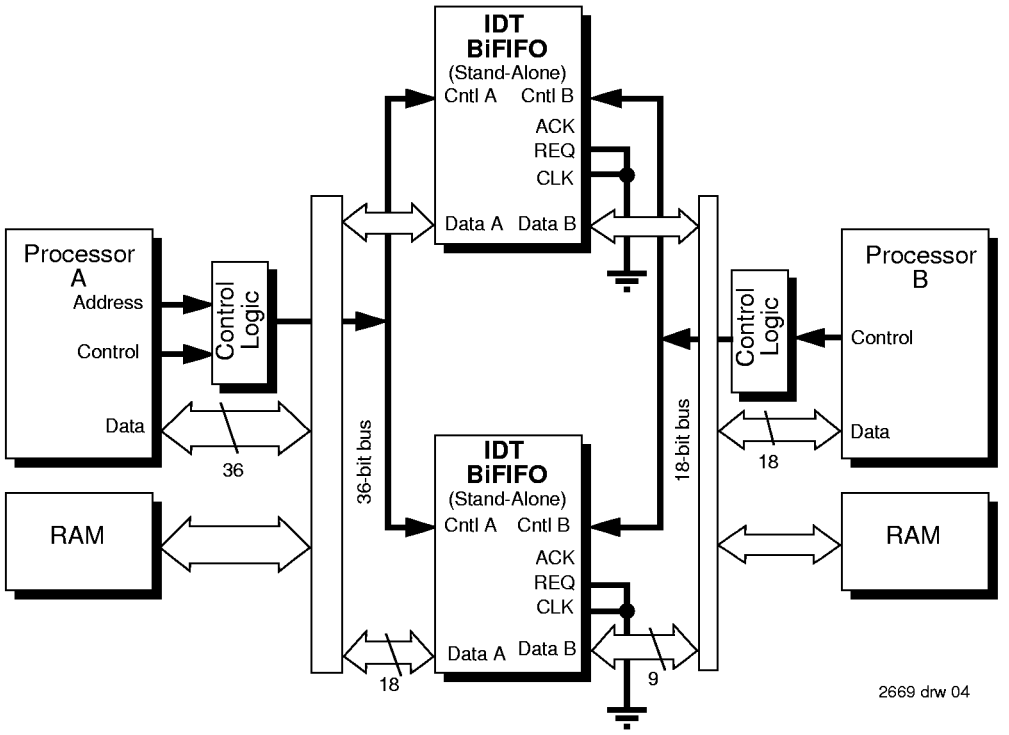
36- to 9-bit Configurations

Two BiFIFOs can be hooked together to create a 36-bit to 9-bit configuration. This means that a 36-bit processor can talk to a 9-bit processor or a 9-bit peripheral. Both BiFIFOs are programmed simultaneously through Port A by placing one command word on the most significant 16 data bits and one command word on the least significant 16 data bits (parity bits should be ignored).

One BiFIFO must be programmed as the master device and the other BiFIFO is the slave device. Bits 11 and 12 of Configuration Register 5 are set to **10** for the slave device and **11** for the master device. The first two 9-bit words on Port B are read from or written to the slave device and the next two 9-bit words go to the master device.

When both BiFIFOs are in peripheral interface mode, the Port B interface pins of the master device are outputs and this BiFIFO controls the bus. The Port B interface pins of the slave device are inputs driven by the master BiFIFO. Two BiFIFOs are connected in Figure 4 to create a 36- to 9-bit peripheral interface.

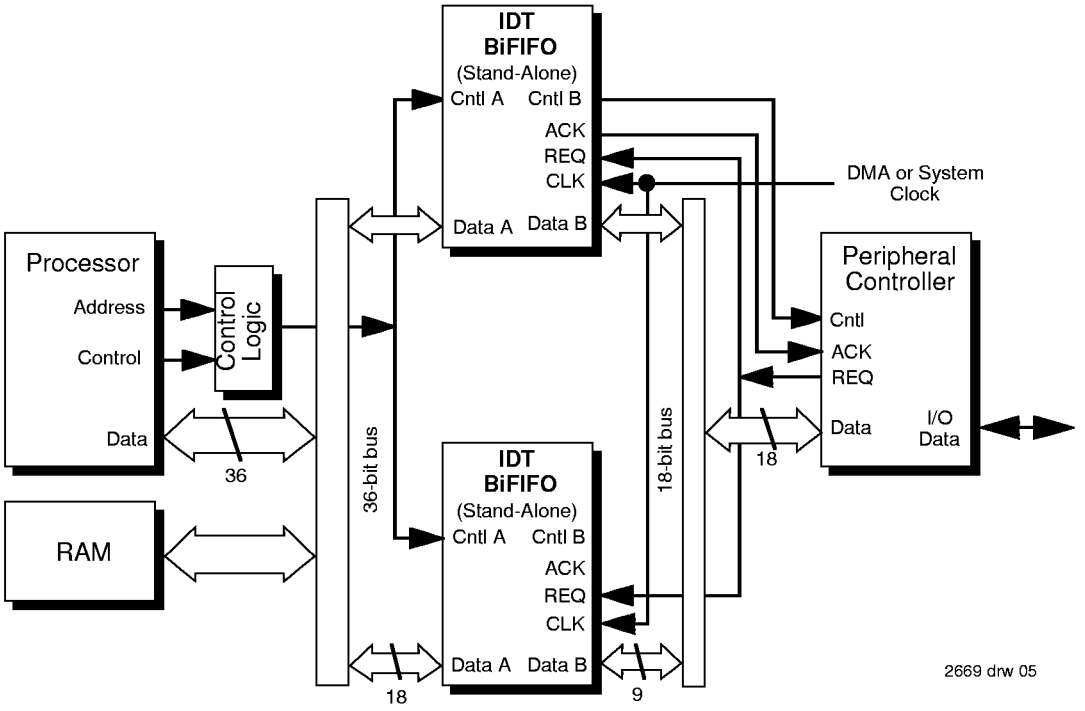
36-BIT PROCESSOR to 18-BIT PROCESSOR CONFIGURATION



NOTE:
1. Upper BiFIFO only is used in 18- to 9-bit configuration. Note that *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, R/$\overline{W}_A$ and $\overline{DS}_A$; *Cntl B* refers to R/$\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

Figure 1. 36- to 18-Bit Processor Interface Configuration

36-BIT PROCESSOR to 18-BIT PERIPHERAL CONFIGURATION



NOTE:

1. Upper BiFIFO only is used in 18- to 9-bit configuration. Note that *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, R/$\overline{W}_A$ and $\overline{DS}_A$; *Cntl B* refers to R/$\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

Figure 2. 36- to 18-Bit Peripheral Interface Configuration

The two BiFIFOs shown in Figure 3 are configured to connect a 36-bit processor to a 9-bit processor.

36- to 18-bit Configurations

In a 36- to 18-bit configuration, two BiFIFOs operate in parallel. Both BiFIFOs are programmed simultaneously, 16 data bits to each device with the 4 parity bits ignored.

Both BiFIFOs must be programmed into stand-alone mode for a 36-bit processor to communicate with an 18-bit processor or an 18-bit peripheral. This means that bits 11 and 12 of Configuration Register 5 must be set to **00**.

This configuration can be extended to wider bus widths (54- to 27-bits, 72- to 36-bits, ...) by adding more BiFIFOs to the configuration. Figures 1 and 2 show multiple BiFIFOs configured for processor and peripheral interface modes respectively.

Processor Interface Mode

When a microprocessor or microcontroller is connected to Port B, all BiFIFOs in the configuration must be programmed to processor interface mode. In this mode, all Port B interface controls are inputs. Both REQ and CLK pins should be pulled LOW to ensure that the set-up and hold time requirements for these pins are met during reset. Figures 1 and 3 show BiFIFOs in processor interface mode.

Peripheral Interface Mode

If Port B is connected to a peripheral controller, all BiFIFOs in the configuration must be programmed in the peripheral interface mode. To assure fixed high states for $\overline{R}_B$ and $\overline{W}_B$ before they are programmed into an output, both pins should be pulled-up to V_{CC} with 10K resistors.

If the BiFIFOs are in stand-alone configuration mode (18- to 9-bit, 36- to 18-bit, ...), then the Port B interface pins are all outputs. Of course, only one set of Port B interface pins should be used to control a single peripheral device, while the other interface pins are all ignored. Figure 2 shows stand-alone configuration BiFIFOs connected to a peripheral.

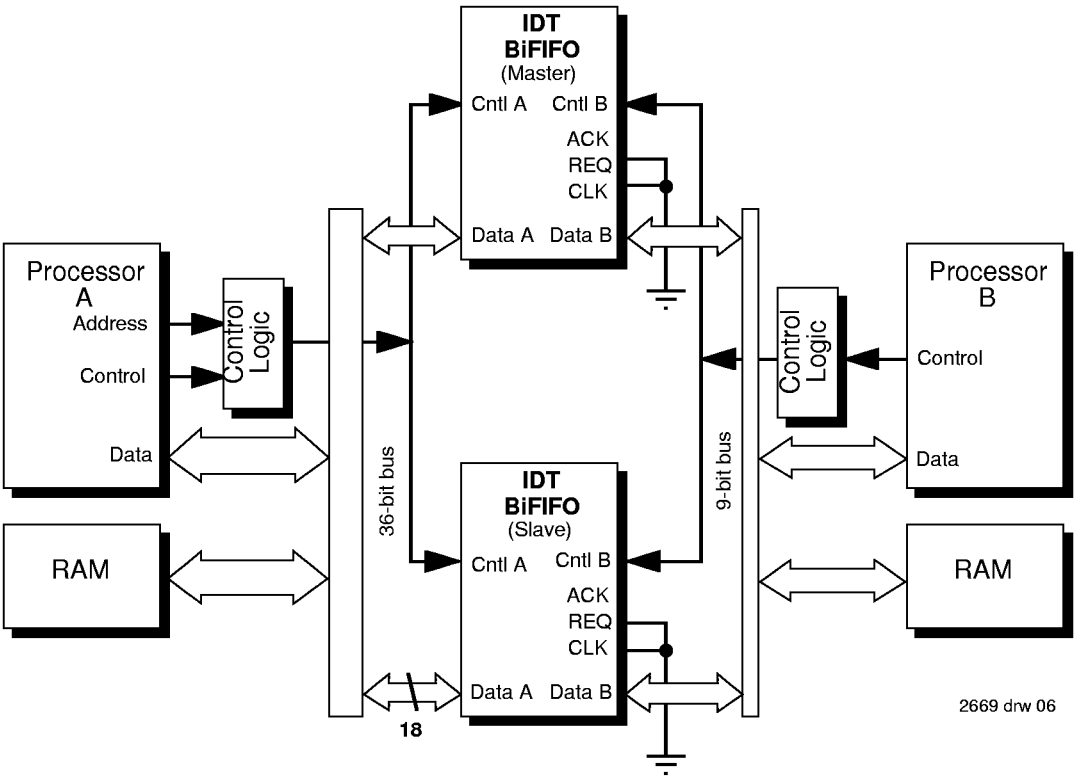
In a 36- to 9-bit configuration, the master device controls the bus. The Port B interface pins of the master device are outputs and the interface pins of the slave device are inputs. A 36- to 9-bit configuration of two BiFIFOs connected to a peripheral is shown in Figure 4.

Port A Interface

The BiFIFO is straightforward to use in microprocessor-based systems because each BiFIFO port has a standard microprocessor control set. Port A has access to six resources: the A→B FIFO, the B→A FIFO, the 9-bit direct data bus (bypass path), the configuration registers, status and command registers. The Port A Address and Read/Write pins determine the resource being accessed as shown in Table 1. Data Strobe is used to move data in and out of the BiFIFO.

When either of the internal FIFOs are accessed 18 bits of data are transferred across Port A. Since the bypass path is only 9 bits wide, the least significant byte with parity (D_{A0}-D_{A7}, D_{A16}) is used on Port A. All of the registers are 16 bits wide which means only the data bits (D_{A0}-D_{A15}) are passed by Port A.

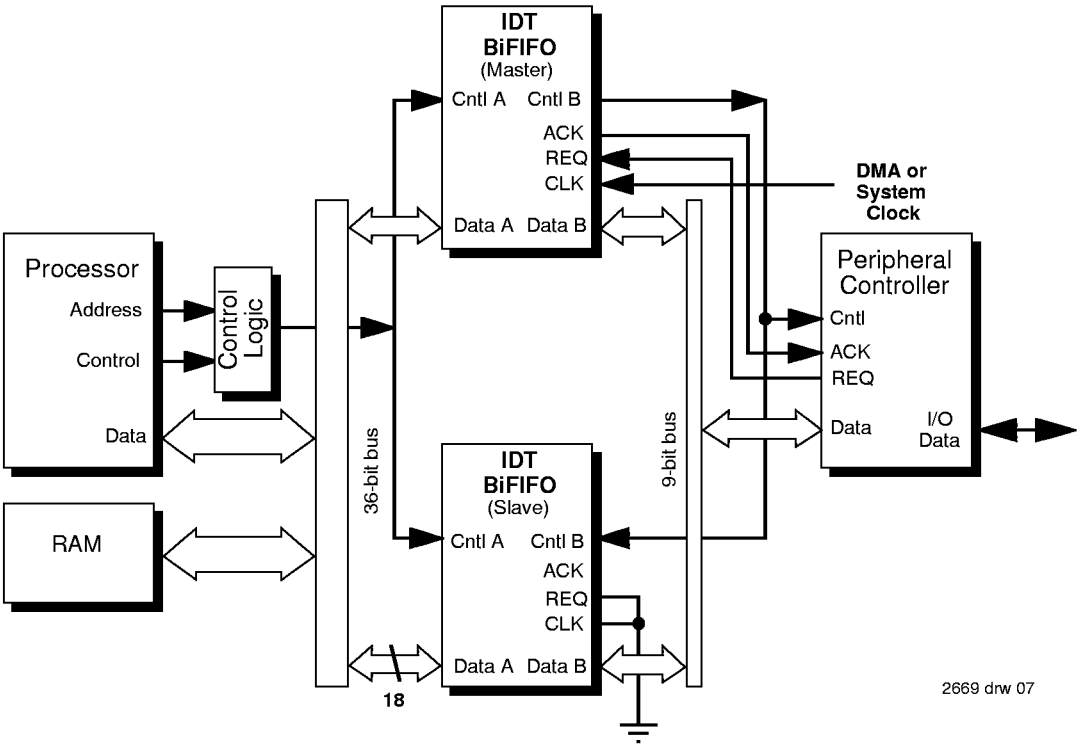
36-BIT PROCESSOR to 9-BIT PROCESSOR CONFIGURATION



NOTE:
1. *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, R/$\overline{W}_A$ and $\overline{DS}_A$; *Cntl B* refers to R/$\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

Figure 3. 36- to 9-Bit Processor Interface Configuration

36-BIT PROCESSOR to 9-BIT PERIPHERAL CONFIGURATION



NOTE:
1. *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, R/$\overline{W}_A$ and $\overline{DS}_A$; *Cntl B* refers to R/$\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

Figure 4. 36- to 9-Bit Peripheral Interface Configuration

PORT A RESOURCES

$\overline{CS}_A$	A_1	A_0	Read	Write
0	0	0	B→A FIFO	A→B FIFO
0	0	1	9-bit Bypass Path	9-bit Bypass Path
0	1	0	Configuration Registers	Configuration Registers
0	1	1	Status Register	Command Register
1	X	X	Disabled	Disabled

2669 tbl 03

Table 1. Accessing Port A Resources Using $\overline{CS}_A$, A_0, and A_1

Bypass Path

The bypass path acts as a bidirectional bus transceiver directly between Port A and Port B. The direct connection requires that the Port A interface pins are inputs and the Port B interface pins are outputs. The bypass path is 9 bits wide in an 18- to 9-bit configuration or in a 36- to 9-bit configuration. Only in the 36- to 18-bit configuration is the bypass path 18 bits wide.

During bypass operations, the BiFIFOs must be programmed into peripheral interface mode. Bit 10 of Configuration Register 5 (see Table 11) is set to **1** for peripheral interface mode. In a 36- to 9-bit configuration, both Port B data buses will be active. Data written into Port A will appear on both master and slave Port B buses concurrently. To avoid Port B bus contention, the data on D_{A0}-D_{A7} and D_{A16} of both BiFIFOs should be exactly the same. Data read from Port A will appear on pins D_{A0}-D_{A7} and D_{A16} of both BiFIFOs within the same 36-bit word.

Command Register

Ten registers are accessible through Port A, a Command Register, a Status Register, and eight Configuration Registers.

The Command Register is written by setting $\overline{CS}_A$ = 0, A_1 = 1, A_0 = 1. Commands written into the BiFIFO have a 4-bit opcode (bit 8 – bit 11) and a 3-bit operand (bit 0 – bit 2) as shown in Figure 5. The commands can be used to reset the BiFIFO, to select the Configuration Register, to perform intelligent reread/rewrite, to set the Port B DMA direction, to set the Status Register format, to modify the Port B Read and Write Pointers, and to clear Port B parity errors. The command opcodes are shown in Table 2.

The reset command initializes different portions of the BiFIFO depending on the command operand. Table 3 shows the reset command operands.

The Configuration Register address is set directly by the command operands shown in Table 4.

Intelligent reread/rewrite is performed by changing the Port B Read Pointer with the Reread Pointer or by changing the Port B Write Pointer with the Rewrite Pointer. No command operands are required to perform a reread/rewrite operation.

COMMAND OPERATIONS

Command Opcode	Function
0000	Reset BiFIFO (see Table 3)
0001	Select Configuration Register (see Table 4)
0010	Load Reread Pointer with Read Pointer Value
0011	Load Rewrite Pointer with Write Pointer Value
0100	Load Read Pointer with Reread Pointer Value
0101	Load Write Pointer with Rewrite Pointer Value
0110	Set DMA Transfer Direction (see Table 5)
0111	Set Status Register Format (see Table 6)
1000	Increment in byte for A→B FIFO Read Pointer (Port B)
1001	Increment in byte for B→A FIFO Write Pointer (Port B)
1010	Clear Write Parity Error Flag
1011	Clear Read Parity Error Flag

2669 tbl 04

Table 2. Functions Performed by Port A Commands

When Port B of the BiFIFO is in peripheral mode, the DMA direction is controlled by the Command Register. Table 5 shows the Port B read/write DMA direction operands.

The BiFIFO supports two Status Register formats. Status Register format 1 gives all the internal flag status, while Status Register format 0 provides the data in the Odd Byte Register. Table 6 gives the operands for selecting the appropriate Status Register format. See Table 8 for the details of the two Status Register formats.

Two commands are provided to increment the Port B Read and Write Pointers in case reread/rewrite is performed. Incrementing the pointers guarantees that pointers will be on a word boundary when an odd number of bytes is transmitted through Port B. No operands are required for these commands.

When parity check errors occur on Port B, a clear parity error command is needed to remove the parity error. There are no operands for these commands.

Reset

The IDT72510 and IDT72520 have a hardware reset pin ($\overline{RS}$) that resets all BiFIFO functions. A hardware reset requires the following four conditions: $\overline{R}_B$ and $\overline{W}_B$ must be HIGH, $\overline{RER}$ and $\overline{REW}$ must be HIGH, LDRER and LDREW must be LOW, and $\overline{DS}_A$ must be HIGH (Figure 9). After a hardware reset, the BiFIFO is in the following state: Configuration Registers 0-3 are **0000H**, Configuration Register 4 is set to **6420H**, and Configuration Registers 5 and 7 are **0000H**. Additionally, Status Register format 0 is selected, all the

COMMAND FORMAT

15			12	11	8	7			3	2	0
X	X	X	X	Command Opcode		X	X	X	X	X	Command Operand

2669 tbl 05

Figure 5. Format for Commands Written into Port A

RESET COMMAND FUNCTIONS

Reset Operands	Function
000	No Operation
001	Reset B→A FIFO (Read, Write, and Rewrite Pointers = 0)
010	Reset A→B FIFO (Read, Write, and Reread Pointers = 0)
011	Reset B→A and A→B FIFO
100	Reset Internal DMA Request Circuitry
101	No Operation
110	No Operation
111	Reset All

2669 tbl 06

Table 3. Reset Command Functions

pointers including the Reread and Rewrite Pointers are set to **0**, the odd byte register valid bit is cleared, the DMA direction is set to B→A write, the internal DMA request circuitry is cleared (set to its initial state), and all parity errors are cleared.

A software reset command can reset A→B pointers and the B→A pointers to **0** independently or together. The request (REQ) DMA circuitry can also be reset independently. A software Reset All command resets all the pointers, the DMA request circuitry, and sets all the Configuration Registers to their default condition. Note that a hardware reset is **NOT** the same as a software Reset All command. Table 7 shows the BiFIFO state after the different hardware and software resets.

SELECT CONFIGURATION REGISTER COMMAND FUNCTIONS

Operands	Function
000	Select Configuration Register 0
001	Select Configuration Register 1
010	Select Configuration Register 2
011	Select Configuration Register 3
100	Select Configuration Register 4
101	Select Configuration Register 5
110	Select Configuration Register 6
111	Select Configuration Register 7

2669 tbl 07

Table 4. Select Configuration Register Command Functions.

DMA DIRECTION COMMAND FUNCTIONS

Operands	Function
XX0	Write B→A FIFO
XX1	Read A→B FIFO

2669 tbl 08

Table 5. Set DMA Direction Command Functions. Command Only Operates in Peripheral Interface Mode

STATUS REGISTER FORMAT COMMAND FUNCTIONS

Operands	Function
XX0	Status Register Format 0
XX1	Status Register Format 1

2669 tbl 09

Table 6. Command Functions to Set the Status Register Format

STATE AFTER RESET

	Hardware Reset	Software Reset				
	($\overline{RS}$ asserted)	B→A (001)	A→B (010)	B→A and A→B (011)	Internal Request (100)	All (111)
Configuration Registers 0-3	0000H	—	—	—	—	0000H
Configuration Register 4	6420H	—	—	—	—	6420H
Configuration Register 5	0000H	—	—	—	—	0000H
Configuration Register 7	0000H	—	—	—	—	0000H
Status Register format	0	—	—	—	—	—
B→A Read, Write, Rewrite Pointers	0	0	—	0	—	0
A→B Read, Write, Reread Pointers	0	—	0	0	—	0
Odd byte register valid bit	clear	clear	—	clear	—	clear
DMA direction	B→A write	—	—	—	—	—
DMA internal request	clear	—	—	—	clear	clear
Parity errors	clear	—	—	—	—	—

2669 tbl 10

Table 7. The BiFIFO State After a Reset Command

Status Register

The Status Register reports the state of the programmable flags, the DMA read/write direction, the Odd Byte Register valid bit, and parity errors. The Status Register is read by setting $\overline{CS}_A$ = 0, A_1 = 1, A_0 = 1 (see Table 1).

There are two Status Register formats that are set by a Status Register format command. Format **0** stores the Odd Byte Register data in the lower eight bits of the Status Register, while format **1** reports the flag states and the DMA read/write direction in the lower eight bits. The upper eight bits are identical for both formats. The flag states, the parity errors, the Odd Byte Register valid bit, and the Status Register format are all in the upper eight bits of the Status Register. See Table 8 for both Status Register formats.

Configuration Registers

The eight Configuration Register formats are shown in Table 9. Configuration Registers 0-3 contain the programmable flag offsets for the Almost Empty and Almost Full flags. These offsets are set to **0** when a hardware reset or a software reset all is applied. Note that Table 9 shows that Configuration Registers 0-3 are 10 bits wide to accommodate the 1,024 locations in each FIFO memory of the IDT72520. Only 9 least significant bits are used for the 512 locations of the IDT72510; the most significant bit, bit 9, must be set to **0**.

Configuration Register 4 is used to assign the internal flags to the external flag pins (FLG_A-FLG_D). Each external flag pin is assigned an internal flag based on the four bit codes shown in Table 10. The default condition for Configuration Register 4 is **6420H** as shown in Table 7. The default flag assignments are: FLG_D is assigned B→A $\overline{Full}$, FLG_C is assigned B→A $\overline{Empty}$, FLG_B is assigned A→B $\overline{Full}$, FLG_A is assigned A→B $\overline{Empty}$.

Configuration Register 5 is a general control register. The format of Configuration Register 5 is shown in Table 11. Bit 0 sets the Intel-style interface ($\overline{R}_B$, $\overline{W}_B$) or Motorola-style interface ($\overline{DS}_B$, R/$\overline{W}_B$) for Port B. Bit 1 changes the byte order for data coming through Port B. Bits 2 and 3 redefine Full and Empty Flags for reread/rewrite data protection.

Bits 4-9 control the DMA interface and are only applicable in peripheral interface mode. In processor interface mode, these bits are don't care states. Bits 4 and 5 set the polarity of the DMA control pins REQ and ACK, respectively. An internal clock controls all DMA operations. This internal clock is derived from the external clock (CLK). Bit 9 determines the internal clock frequency: the internal clock = CLK or the internal clock = CLK divided by 2. Bit 8 sets whether $\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for either one or two internal clocks. Bits 6 and 7 set the number of internal clocks between REQ assertion and ACK assertion. The timing can be from 2 to 5 cycles as shown in Figure 17.

Bit 10 controls Port B processor or peripheral interface mode. In processor mode, the Port B control pins ($\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$, R/$\overline{W}_B$) are inputs and the DMA controls are ignored. In peripheral mode, the Port B control pins are outputs and the DMA controls are active.

Bits 11 and 12 set the width expansion mode. For 18- to 9-bit configurations or 36- to 18-bit configurations, the BiFIFO should be set in stand-alone mode. For a 36- to 9-bit configuration, one BiFIFO must be in slave mode and the other BiFIFO must be in master mode. The master BiFIFO allows the first two bytes transferred across Port B to go to the slave BiFIFO, then the next two bytes go to the master BiFIFO.

Configuration Register 7 controls the parity functions of Port B as shown in Table 12. Either parity generation or parity

STATUS REGISTER FORMAT 0

Bit	Signal
0	Odd Byte Register
1	
2	
3	
4	
5	
6	
7	
8	Valid Bit
9	Write Parity Error
10	Read Parity Error
11	Status Register Format = 0
12	A→B Full Flag
13	A→B Almost-Full Flag
14	B→A Empty Flag
15	B→A Almost-Empty Flag

2669 tbl 11

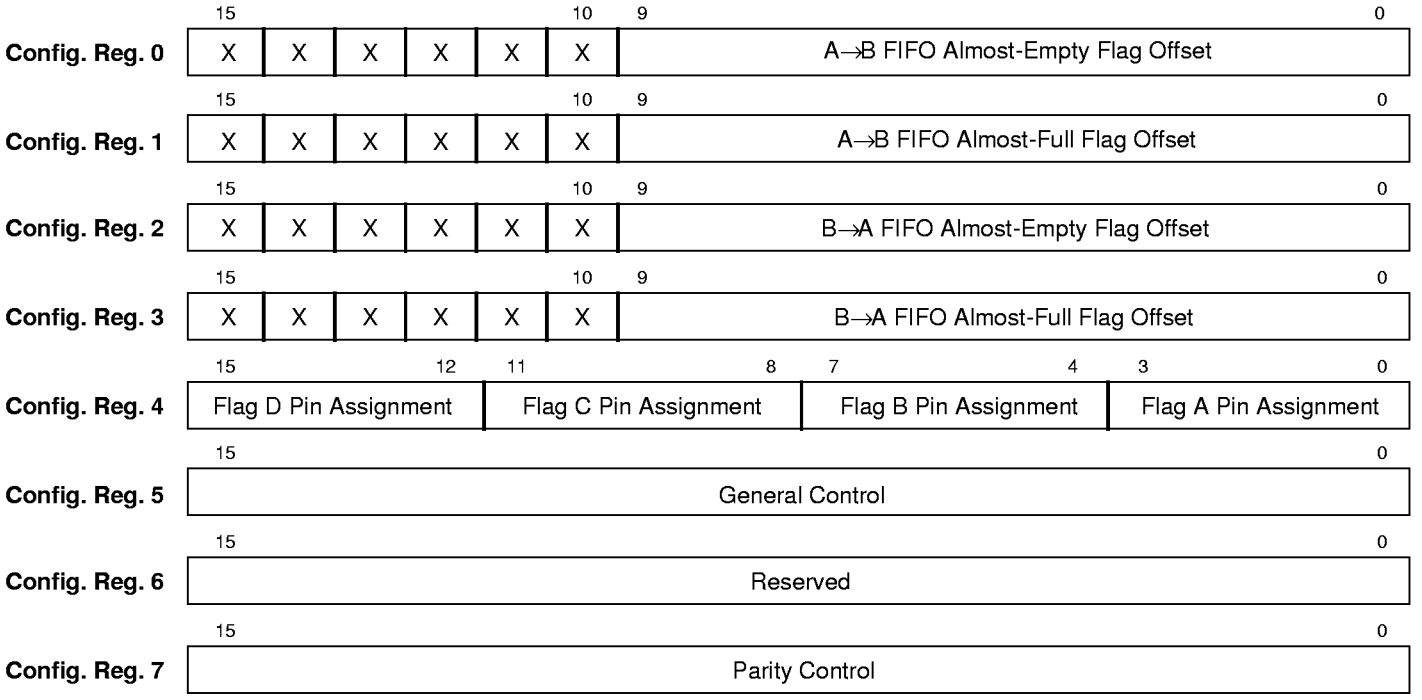
STATUS REGISTER FORMAT 1

Bit	Signal
0	Reserved
1	Reserved
2	Reserved
3	DMA Direction
4	A→B Empty Flag
5	A→B Almost-Empty Flag
6	B→A Full Flag
7	B→A Almost-Full Flag
8	Valid Bit
9	Write Parity Error
10	Read Parity Error
11	Status Register Format = 1
12	A→B Full Flag
13	A→B Almost-Full Flag
14	B→A Empty Flag
15	B→A Almost-Empty Flag

2669 tbl 12

Table 8. The Two Status Register Formats

CONFIGURATION REGISTER FORMATS



NOTE:

1. Bit 9 of Configuration Registers 0-3 must be set to 0 on the IDT72510.

2669 tbl 13

Table 9. The BiFIFO Configuration Register Formats

checking is enabled for data read and written through Port B. Bit 8 controls parity checking and generation for B→A write data. Bit 9 controls parity checking and generation for A→B read data. Bit 10 controls whether the parity is odd or even. Bit 11 is used to assign the internal parity checking error to the FLGA pin. When the parity error is assigned to FLGA, the Configuration Register 4 flag assignment for FLGA is ignored.

Programmable Flags

The IDT BiFIFO has eight internal flags; four of these flags have programmable offsets, the other four are empty or full. Associated with each FIFO memory array are four internal flags, Empty, Almost-Empty, Almost-Full and Full, for the total of eight internal flags. The Almost-Empty and Almost-Full offsets can be set to any depth through the Configuration Registers 0-3 (see Table 9). The offset (or depth) of FIFO RAM array is based on the unit of an 18-bit word. The flags are asserted at the depths shown in Table 13. After a hardware reset or a software reset all, the almost flag offsets are set to **0**. Even though the offsets are equivalent, the Empty and Almost-Empty flags have different timing which means that the flags are not coincident. Similarly, the Full and Almost-Full flags are not coincident because of timing.

These eight internal flags can be assigned to any of four external flag pins (FLGA-FLGD) through Configuration Register 4 (see Table 10). For the specific flag timings, see Figures 20-23.

The current state of all eight flags is available in the Status Register in Status Register format 1. In Status Register format 0, only four flags can be found in the Status Register (see Table 8).

EXTERNAL FLAG ASSIGNMENT CODES

Assignment Code	Internal Flag Assigned to Flag Pin
0000	A→B $\overline{\text{Empty}}$
0001	A→B $\overline{\text{Almost-Empty}}$
0010	A→B $\overline{\text{Full}}$
0011	A→B $\overline{\text{Almost-Full}}$
0100	B→A $\overline{\text{Empty}}$
0101	B→A $\overline{\text{Almost-Empty}}$
0110	B→A $\overline{\text{Full}}$
0111	B→A $\overline{\text{Almost-Full}}$
1000	A→B Empty
1001	A→B Almost-Empty
1010	A→B Full
1011	A→B Almost-Full
1100	B→A Empty
1101	B→A Almost-Empty
1110	B→A Full
1111	B→A Almost-Full

2669 tbl 14

Table 10. Configuration Register 4 Internal Flag Assignments to External Flag Pins.

Port B Interface

Port B also has parity, reread/rewrite and DMA functions. Port B can be configured to interface to either Intel-style ($\overline{R}_B$, $\overline{W}_B$) or Motorola-style ($\overline{DS}_B$, R/$\overline{W}_B$) devices in Configuration Register 5 (see Table 11). Port B can also be configured to talk to a processor or a peripheral device through Configuration Register 5. In processor interface mode, the Port B interface controls are inputs. In peripheral interface mode, the Port B interface controls are outputs. After a hardware reset or a software Reset All command, Port B defaults to an Intel-style processor interface; the controls are inputs.

Two 9-bit words are put together to create each 18-bit word stored in the internal FIFOs. The first 9-bit word written to Port B goes into the Odd Byte Register shown in the detailed block diagram. The Odd Byte Register valid bit (Bit 8) in the Status Register is **1** when this first 9-bit word is written. The data bits from Port B (D_{B0}-D_{B7}) are also stored in the lower 8 bits of the Status Register when Status Register format 0 is selected (see Table 8). The second write on Port B moves the 9-bits from Port B and the 9-bits in the Odd Byte Register into the B→A FIFO and advances the B→A Write Pointer. The Status Register valid bit is set to **0** after the second write.

When Port B reads data from the A→B FIFO, two buffers choose which 9 of the 18 memory bits are sent to Port B. These buffers alternate between the upper 9 bits (D_{A8}-D_{A15}, D_{A17}) and the lower 9 bits (D_{A0}-D_{A7}, D_{A16}). The A→B Read Pointer is advanced after every two Port B reads.

CONFIGURATION REGISTER 5 FORMAT

Bit	Function		
0	Select Port B Interface	0	Pins are $\overline{R}_B$ and $\overline{W}_B$ (Intel-style interface)
	$\overline{R}_B$ & $\overline{W}_B$ or $\overline{DS}_B$ & R/$\overline{W}_B$	1	Pins are $\overline{DS}_B$ and R/$\overline{W}_B$ (Motorola-style interface)
1	Byte Order of 18-bit Word	0	Lower byte D_{A7}-D_{A0} and parity D_{A16} are read or written first on Port B
		1	Upper byte D_{A15}-D_{A8} and parity D_{A17} are read or written first on Port B
2	Full Flag Definition	0	Full Flag is asserted when write pointer meets read pointer
		1	Full Flag is asserted when write pointer meets reread pointer
3	Empty Flag Definition	0	Empty Flag is asserted when read pointer meets write pointer
		1	Empty Flag is asserted when read pointer meets rewrite pointer
4	REQ Pin Polarity	0	REQ pin active HIGH
		1	REQ pin active LOW
5	ACK Pin Polarity	0	ACK pin active LOW
		1	ACK pin active HIGH
7-6	REQ / ACK Timing	00	2 internal clocks between REQ assertion and ACK assertion
		01	3 internal clocks between REQ assertion and ACK assertion
		10	4 internal clocks between REQ assertion and ACK assertion
		11	5 internal clocks between REQ assertion and ACK assertion
8	Port B Read and Write	0	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 1 internal clock
	Timing Control for Peripheral Mode	1	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 2 internal clocks
9	Internal Clock	0	internal clock = CLK
	Frequency Control	1	internal clock = CLK divided by 2
10	Port B Interface	0	Processor interface mode (Port B controls are inputs)
	Mode Control	1	Peripheral interface mode (Port B controls are outputs)
12-11	Width Expansion Mode Control	00	Stand-alone mode (18- to 9-bits, 36- to 18-bits)
		01	Reserved
		10	Slave width expansion mode (36- to 9-bits)
		11	Master width expansion mode (36- to 9-bits)
13	Unused		
14	Unused		
15	Unused		

2669 tbl 15

Table 11. BiFIFO Configuration Register 5 Format

CONFIGURATION REGISTER 7 FORMAT

BIT	FUNCTION		
0-7	Unused		
8	Parity Input Control B→A	0	Disable Parity Generate, Enable Parity Check
		1	Enable Parity Generate, Disable Parity Check
9	Parity Output Control A→B	0	Disable Parity Generate, Enable Parity Check
		1	Enable Parity Generate, Disable Parity Check
10	Parity Odd/Even Control	0	Odd
		1	Even
11	Assign Parity Error to Flag A Pin	0	No Parity Error Output
		1	Parity Error on Flag A Pin
12-15	Unused		

2669 tbl 16

Table 12. BiFIFO Configuration Register 7 Format

The BiFIFO can be set to order the 9-bit data so the first 9-bits go to the LSB (DA_0-DA_7, DA_{16}) or the MSB (DA_8-DA_{15}, DA_{17}) of Port A. This data ordering is controlled by bit 1 of Configuration Register 5 (see Table 11).

DMA Control Interface

The BiFIFO has DMA control to simplify data transfers with peripherals. For the BiFIFO DMA controls (REQ, ACK and CLK) to operate, the BiFIFO must be in peripheral interface mode (Configuration Register 5, Table 11).

DMA timing is controlled by the external clock input, CLK. An internal clock is derived from this CLK signal to generate the $\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$ and R/$\overline{W}_B$ output signals. The internal clock also determines the timing between REQ assertion and ACK assertion. Bit 9 of Configuration Register 5 determines whether the internal clock is the same as CLK or whether the internal clock is CLK divided by 2.

Bit 8 of Configuration Register 5 sets whether $\overline{R}_B$, $\overline{W}_B$ and $\overline{DS}_B$ are asserted for 1 or 2 internal clocks. Bits 6 and 7 of Configuration Register 5 set the number of clocks between REQ assertion and ACK assertion. The clocks between REQ assertion and ACK assertion can be 2, 3, 4 or 5.

Bits 4 and 5 of Configuration Register 5 set the polarity of the REQ and ACK pins, respectively.

A DMA transfer command sets the Port B read/write direction (see Table 5). The timing diagram for DMA transfers is shown in Figure 17. The basic DMA transfer starts with REQ assertion. After 2 to 5 internal clocks, ACK is asserted by the BiFIFO. ACK will not be asserted if a read is attempted on an Empty A→B FIFO or if a write is attempted on a Full B→A FIFO. If the BiFIFO is in Motorola-style interface mode, R/$\overline{W}_B$ is set at the same time that ACK is asserted. One internal clock later, $\overline{DS}_B$ is asserted. If the BiFIFO is in Intel-style interface mode, either $\overline{R}_B$ or $\overline{W}_B$ is asserted one internal clock after ACK assertion. These read/write controls stay asserted for 1 or 2 internal clocks, then ACK, $\overline{DS}_B$, $\overline{R}_B$ and $\overline{W}_B$ are made inactive. This completes the transfer of one 9-bit word.

On the next rising edge of CLK, REQ is sampled. If REQ is still asserted, another DMA transfer starts with the assertion of ACK. Data transfers will continue as long as REQ is asserted.

Parity Checking and Generation

Parity generation or checking is performed by the BiFIFO on data passing through Port B. Parity can either be odd or even as determined by Bit 10 of Configuration Register 7.

When parity checking is enabled, DB_8 is treated as a data bit. DB_8 data will be passed to DA_{16} (bypass operation) or stored in the RAM array (FIFO operation) for B->A operation; similarly, DA_{16} or parity bits from the RAM array will be passed to DB_8 for A->B operations. A->B read parity errors and B->A write parity errors are shown in Bit 9 and 10 in the Status Register.

INTERNAL FLAG TRUTH TABLE

Number of Words in FIFO					
From	To	Empty Flag	Almost-Empty Flag	Almost-Full Flag	Full Flag
0	0	Asserted	Asserted	Not Asserted	Not Asserted
1	n	Not Asserted	Asserted	Not Asserted	Not Asserted
n + 1	D - (m + 1)	Not Asserted	Not Asserted	Not Asserted	Not Asserted
D - m	D - 1	Not Asserted	Not Asserted	Asserted	Not Asserted
D	D	Not Asserted	Not Asserted	Asserted	Asserted

NOTE:

2669 tbl 17

1. BiFIFO flags can be assigned to external flag pins to be observed. D = FIFO depth (IDT72510 = 512, IDT72520 = 1,024), n = Almost-Empty flag offset, m = Almost-Full flag offset.

Table 13. Internal Flag Truth Table.

If an external parity error signal is required, a logical OR of the two parity error bits is brought out to FLG_A pin by setting Bit 11 of Configuration Register 7.

Parity generation creates the ninth bit. This ninth bit is placed on D_{B8} for A->B read operation, and on D_{A16} or RAM array for B->A write operation.

It is recommended that if the parity pins (D_{B8}, D_{A16}, and D_{A17}) are not used, they should be pulled down with 10K resistors for noise immunity.

Intelligent Reread/Rewrite

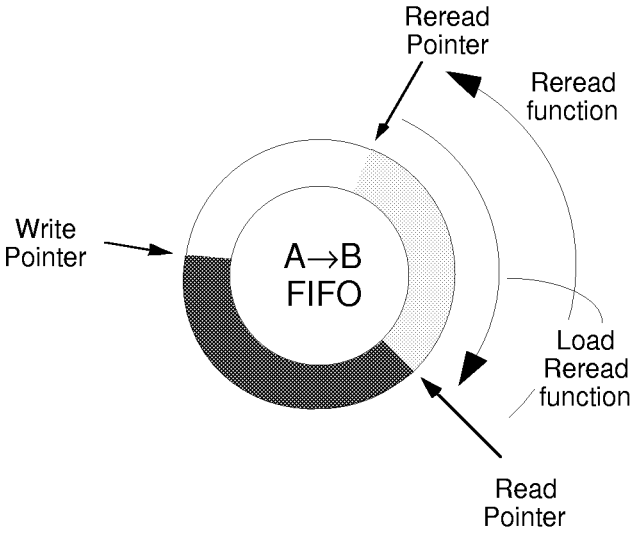
Intelligent reread/rewrite is a method the BiFIFO uses to help assure data integrity. Port B of the BiFIFO has two extra pointers, the Reread Pointer and the Rewrite Pointer. The Reread Pointer is associated with the A->B FIFO Read Pointer, while the Rewrite Pointer is associated with the B->A FIFO Write Pointer. The Reread Pointer holds the start address of a data block in the A->B FIFO RAM, and the Read Pointer is the current address of the same FIFO RAM array. By loading the Read Pointer with the value held in the Reread Pointer (RER asserted), reads will start over at the beginning of the data block. In order to mark the beginning of a data block, the Reread Pointer should be loaded with the Read Pointer value (LDRER asserted) before the first read is performed on this data block. Figure 6 shows a Reread operation.

Similarly, the Rewrite Pointer holds the start address of a data block in the B->A FIFO RAM, while the Write Pointer is the current address within the RAM array. The operation of the REW and LDREW is identical to the RER and LDRER discussed above. Figure 7 shows a Rewrite operation.

For the reread data protection, Bit 2 of Configuration Register 5 can be set to 1 to prevent the data block form being overwritten. In this way, the assertion of A->B full flag will occur when the write pointer meets the reread pointer instead of the read pointer as in the normal definition. For the rewrite data protection, Bit 3 of Configuration Register 5 can be set to 1 to prevent the data block from being read. In this case, the assertion of B->A empty flag will occur when the read pointer meets the rewrite pointer instead of the write pointer.

In conclusion, Bit 2 and 3 of Configuration Register 5 are used to redefine Full & Empty flags for data block partition. Although it can serve the purpose of data protection, the setting of these 2 bits is independent of the functions caused by RER/REW, or LDRER/LDREW assertions.

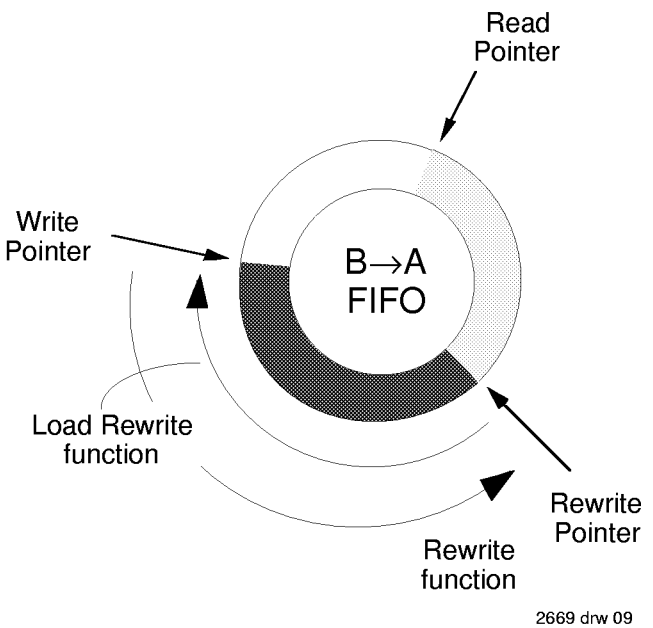
REREAD OPERATIONS (1,2)



NOTES:
1. If bit 2 is set to 1,
   Empty flag asserted if Read = Write
   Full flag asserted if Reread + FIFO size = Write
2. If bit 2 is set to 0,
   Empty flag asserted if Read = Write
   Full flag asserted if Read + FIFO size = Write

Figure 6. BiFIFO Reread Operations

REWRITE OPERATIONS (1,2)



NOTES:
1. If bit 3 is set to 1,
   Empty flag asserted if Read = Rewrite
   Full flag asserted if Read + FIFO size = Write
2. If bit 3 is set to 0,
   Empty flag asserted if Read = Write
   Full flag asserted if Read + FIFO size = Write

Figure 7. BiFIFO Rewrite Operations

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

2669 tbl 18

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input HIGH Voltage	2.0	—	—	V
V_{IL}(1)	Input LOW Voltage	—	—	0.8	V
T_A	Operating Temperature Commercial	0	—	70	°C

2669 tbl 19

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	IDT72510L IDT72520L Commercial t_{CLK} = 25, 35, 50 ns			Unit
		Min.	Typ.	Max.	
I_{LI}(1)	Input Leakage Current (any input)	–1	—	1	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OUT} = –1 mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OUT} = 4 mA	—	—	0.4	V
I_{CC1}(3)	Active Power Supply Current	—	150	220	mA
I_{CC2}(3)	Standby Current ($\overline{R}_B$ = $\overline{W}_B$ = $\overline{DS}_A$ = V_{IH})	—	16	30	mA

2669 tbl 20

NOTES:
1. Measurements with 0.4V ≤ V_{IN} ≤ V_{CC}, $\overline{DS}A$ = $\overline{DS}B$ ≥ V_{IH}.
2. Measurements with 0.4V ≤ V_{OUT} ≤ V_{CC}, $\overline{DS}A$ = $\overline{DS}B$ ≥ V_{IH}.
3. Tested with outputs open (I_{OUT} = 0). Tested at f = 20 MHz.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 8

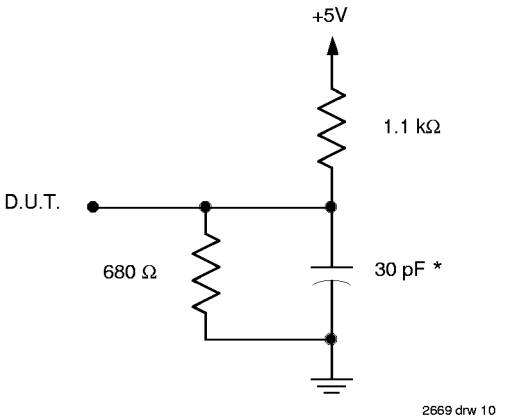
2669 tbl 21

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN} (2)	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT} (1,2)	Output Capacitance	V_{OUT} = 0V	12	pF

2669 tbl 22

NOTES:
1. With output deselected.
2. Characterized values, not currently tested.



or equivalent circuit

Figure 8. Output Load

* Includes jig and scope capacitances

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Commercial						Unit	Timing Figure
		IDT72510L25 IDT72520L25		IDT72510L35 IDT72520L35		IDT72510L50 IDT72520L50			
		Min.	Max.	Min.	Max.	Min.	Max.		
RESET TIMING (Port A and Port B)									
t_{RSC}	Reset cycle time	35	—	45	—	65	—	ns	9
t_{RS}	Reset pulse width	25	—	35	—	50	—	ns	9
t_{RSS}	Reset set-up time	25	—	35	—	50	—	ns	9
t_{RSR}	Reset recovery time	10	—	10	—	15	—	ns	9
t_{RSF}	Flag reset pulse width	—	35	—	45	—	65	ns	9
PORT A TIMING									
t_{aA}	Port A access time	—	25	—	35	—	50	ns	12, 14, 15
t_{aLZ}	Read or write pulse LOW to data bus at Low-Z	5	—	5	—	5	—	ns	12, 15, 16
t_{aHZ}	Read or write pulse HIGH to data bus at High-Z	—	15	—	20	—	30	ns	12, 14, 15, 16
t_{aDV}	Data valid from read pulse HIGH	5	—	5	—	5	—	ns	12, 14, 16
t_{aRC}	Read cycle time	35	—	45	—	65	—	ns	12
t_{aRPW}	Read pulse width	25	—	35	—	50	—	ns	12, 14, 15
t_{aRR}	Read recovery time	10	—	10	—	15	—	ns	12
t_{aS}	$\overline{CS}_A$, A_0, A_1, R/$\overline{W}_A$ set-up time	5	—	5	—	5	—	ns	10, 12, 16
t_{aH}	$\overline{CS}_A$, A_0, A_1, R/$\overline{W}_A$ hold time	5	—	5	—	5	—	ns	10, 12
t_{aDS}	Data set-up time	15	—	18	—	30	—	ns	11, 12, 14, 15
t_{aDH} (1)	Data hold time	0	—	0	—	5	—	ns	11, 12, 14, 15
t_{aWC}	Write cycle time	35	—	45	—	65	—	ns	12
t_{aWPW}	Write pulse width	25	—	35	—	50	—	ns	11, 12, 14
t_{aWR}	Write recovery time	10	—	10	—	15	—	ns	12
t_{aWRCOM}	Write recovery time after a command	25	—	35	—	50	—	ns	11

NOTE:

2669 tbl 23

1. The minimum data hold time is 5ns (10ns for the 80ns speed grade) when writing to the Command or Configuration registers.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Commercial IDT72510L25 IDT72520L25 Min.	Max.	IDT72510L35 IDT72520L35 Min.	Max.	IDT72510L50 IDT72520L50 Min.	Max.	Unit	Timing Figure
PORT B PROCESSOR INTERFACE TIMING									
t_{bA1}	Port B access time with no parity	—	25	—	35	—	50	ns	13, 14, 15
t_{bA2}	Port B access time with parity	—	30	—	42	—	60	ns	13, 14, 15
t_{bLZ}	Read or write pulse LOW to data bus at Low-Z	5	—	5	—	5	—	ns	13, 14, 15
t_{bHZ}	Read or write pulse HIGH to data bus at High-Z	—	15	—	20	—	30	ns	13, 14, 15
t_{bDV}	Data valid from read pulse HIGH	5	—	5	—	5	—	ns	13, 14, 15, 16
t_{bRC}	Read cycle time	35	—	45	—	65	—	ns	13
t_{bRPW}	Read pulse width	25	—	35	—	50	—	ns	13
t_{bRR}	Read recovery time	10	—	10	—	15	—	ns	13
t_{bS}	R/$\overline{W}_B$ set-up time	5	—	5	—	5	—	ns	13
t_{bH}	R/$\overline{W}_B$ hold time	5	—	5	—	5	—	ns	13
t_{bDS1}	Data set-up time with no parity	15	—	18	—	30	—	ns	13, 14, 15
t_{bDH1}	Data hold time with no parity	0	—	0	—	5	—	ns	13, 14, 15
t_{bDS2}	Data set-up time with parity	18	—	22	—	35	—	ns	13, 14, 15
t_{bDH2}	Data hold time with parity	0	—	0	—	5	—	ns	13, 14, 15
t_{bWC}	Write cycle time	35	—	45	—	65	—	ns	13
t_{bWPW}	Write pulse width	25	—	35	—	50	—	ns	13, 15
t_{bWR}	Write recovery time	10	—	10	—	15	—	ns	13
PORT B PERIPHERAL INTERFACE TIMING									
t_{bA1}	Port B access time with no parity	—	25	—	40	—	55	ns	17
t_{bA2}	Port B access time with parity	—	30	—	42	—	60	ns	17
t_{bCKC}	Clock cycle time	15	—	20	—	25	—	ns	17
t_{bCKH}	Clock pulse HIGH time	6	—	6	—	10	—	ns	17
t_{bCKL}	Clock pulse LOW time	6	—	6	—	10	—	ns	17
t_{bREQS}	Request set-up time	5	—	5	—	10	—	ns	17
t_{bREQH}	Request hold time	5	—	5	—	5	—	ns	17
t_{bACKL}	Delay from a rising clock edge to ACK switching	—	15	—	18	—	25	ns	17

2669 tbl 24

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Commercial IDT72510L25 IDT72520L25 Min.	Max.	IDT72510L35 IDT72520L35 Min.	Max.	IDT72510L50 IDT72520L50 Min.	Max.	Unit	Timing Figure
PORT B RETRANSMIT and PARITY TIMING									
t_{bDSBH}	$\overline{RER}$, $\overline{REW}$, LDRER, LDREW set-up and recovery time	10	—	10	—	15	—	ns	9, 18
t_{bPER}	Parity error time	20	—	25	—	30	—	ns	19
BYPASS TIMING									
t_{BYA}	Bypass access time	—	15	—	20	—	30	ns	16
t_{BYD}	Bypass delay	—	10	—	15	—	20	ns	16
t_{aBYDV}	Bypass data valid time from $\overline{DS}_A$	15	—	15	—	15	—	ns	16
t_{bBYDV} (3)	Bypass data valid time from $\overline{DS}_B$	3	—	3	—	3	—	ns	16
FLAG TIMING									
t_{REF}	Read clock edge to Empty Flag asserted	—	25	—	35	—	45	ns	14, 15, 20, 22
t_{WEF}	Write clock edge to Empty Flag not asserted	—	25	—	35	—	45	ns	14, 15, 20, 22
t_{RFF}	Read clock edge to Full Flag not asserted	—	25	—	35	—	45	ns	14, 15, 21, 23
t_{WFF}	Write clock edge to Full Flag asserted	—	25	—	35	—	45	ns	14, 15, 21, 23
t_{RAEF}	Read clock edge to Almost-Empty Flag asserted	—	40	—	50	—	60	ns	20, 22
t_{WAEF}	Write clock edge to Almost-Empty Flag not asserted	—	40	—	50	—	60	ns	20, 22
t_{RAFF}	Read clock edge to Almost-Full Flag not asserted	—	40	—	50	—	60	ns	21, 23
t_{WAFF}	Write clock edge to Almost-Full Flag asserted	—	40	—	50	—	60	ns	21, 23

NOTES:

2669 tbl 25

1. Read and Write are internal signals derived from $\overline{DS}_A$, R/$\overline{W}_A$, $\overline{DS}_B$, R/$\overline{W}_B$, $\overline{R}_B$ and $\overline{W}_B$.
2. Although the flags, Empty, Almost-Empty, Almost-Full and Full Flags are internal flags , the timing given is for those assigned to external pins.
3. Values guaranteed by design, not currently tested.

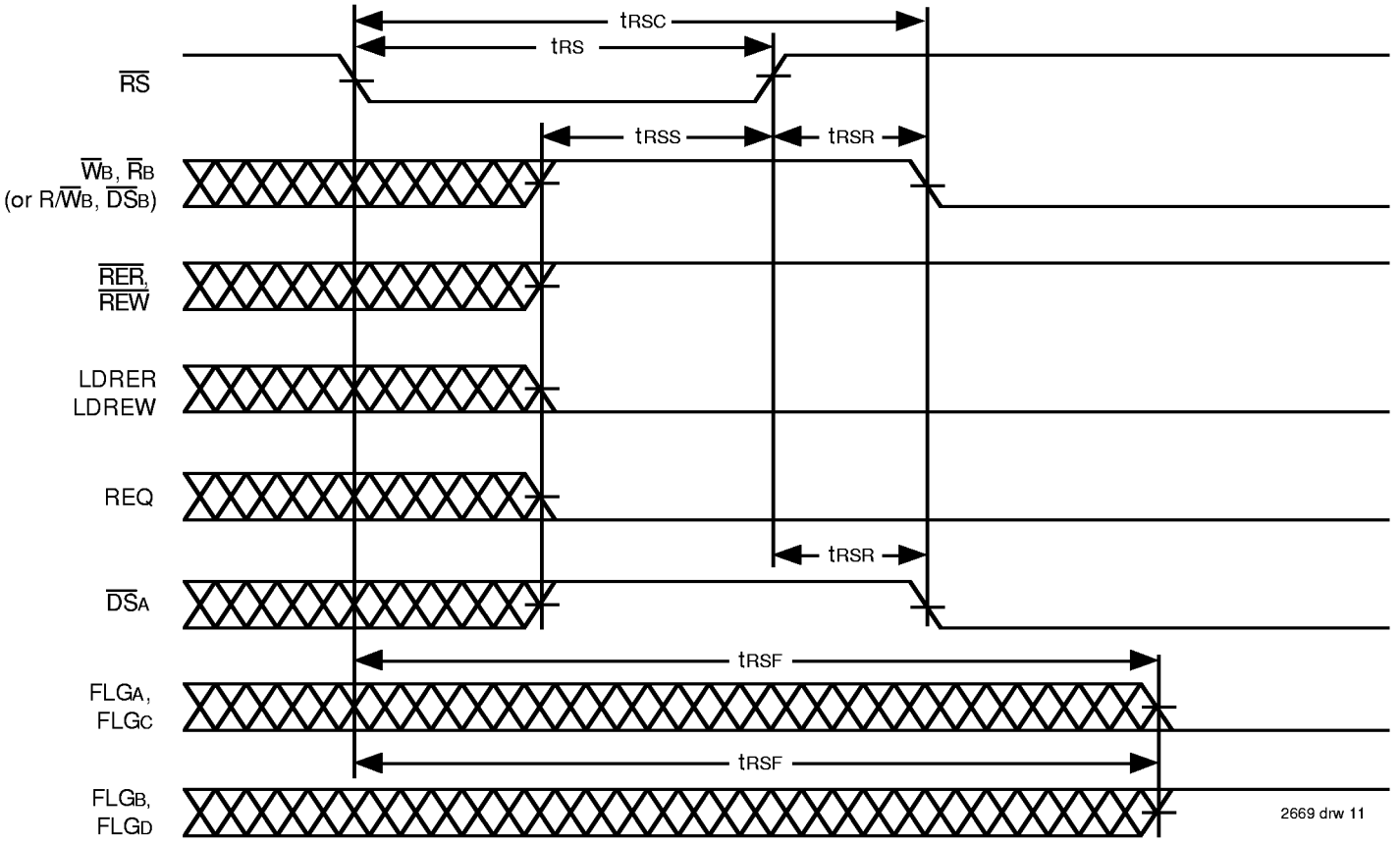


Figure 9. Hardware Reset Timing

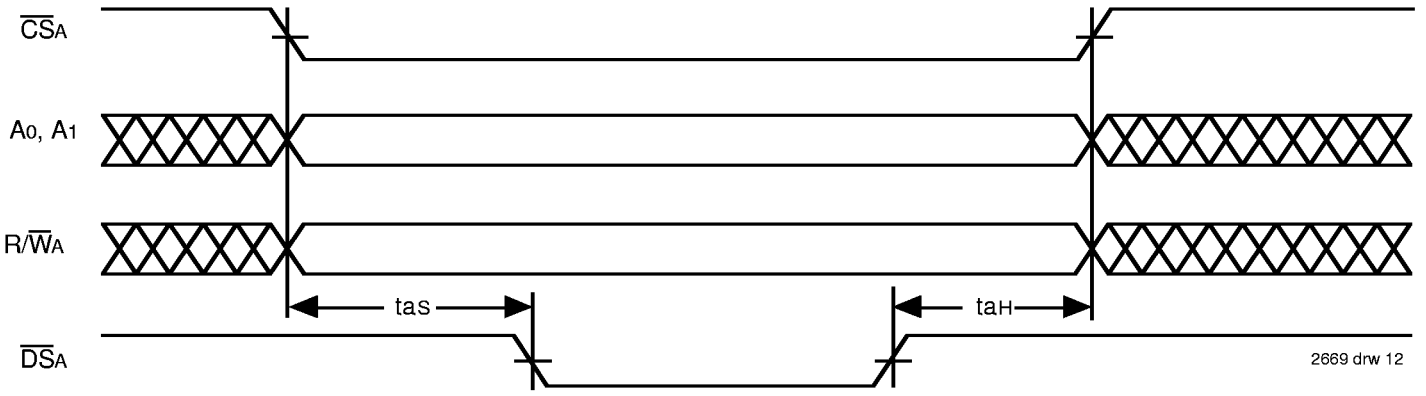


Figure 10. Basic Port A Control Signal Timing (Applies to All Port A Timing)

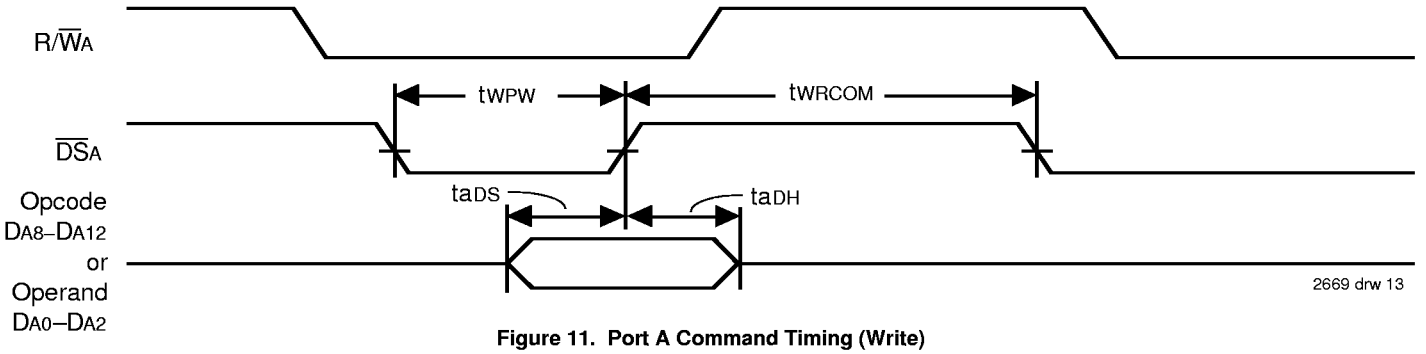
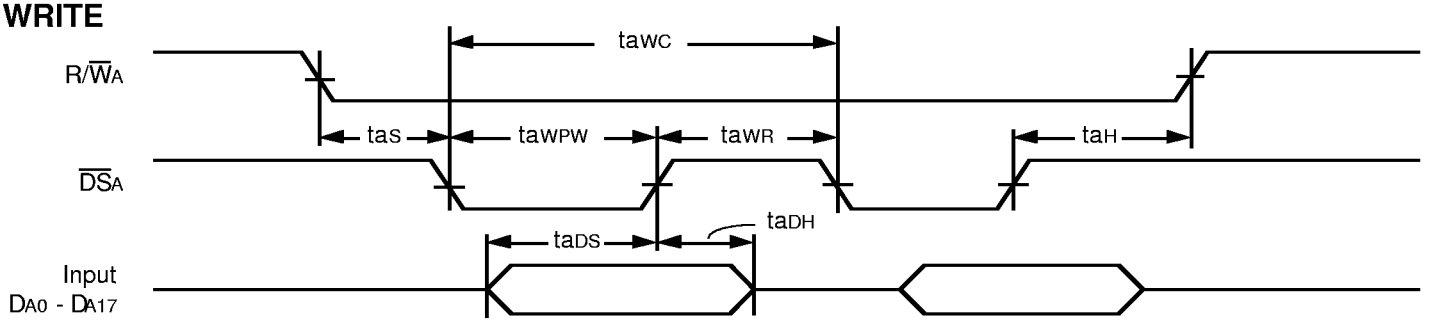


Figure 11. Port A Command Timing (Write)

WRITE



READ

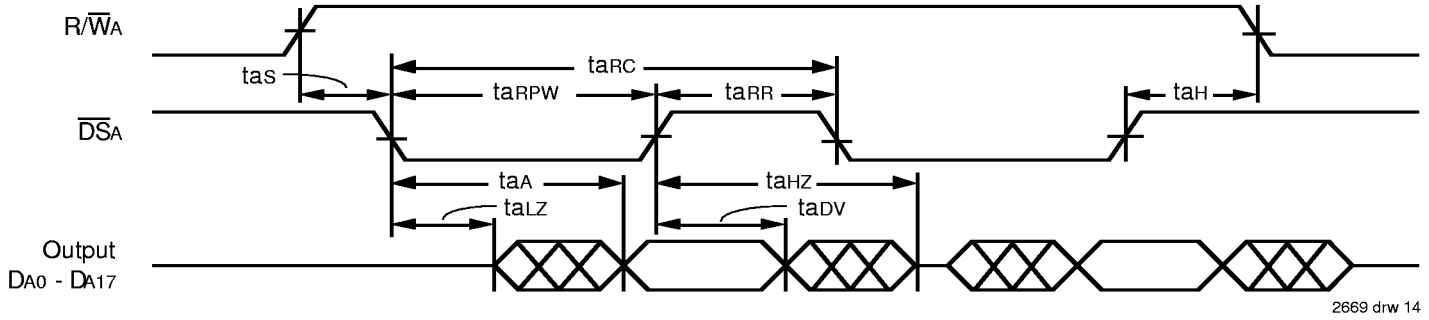
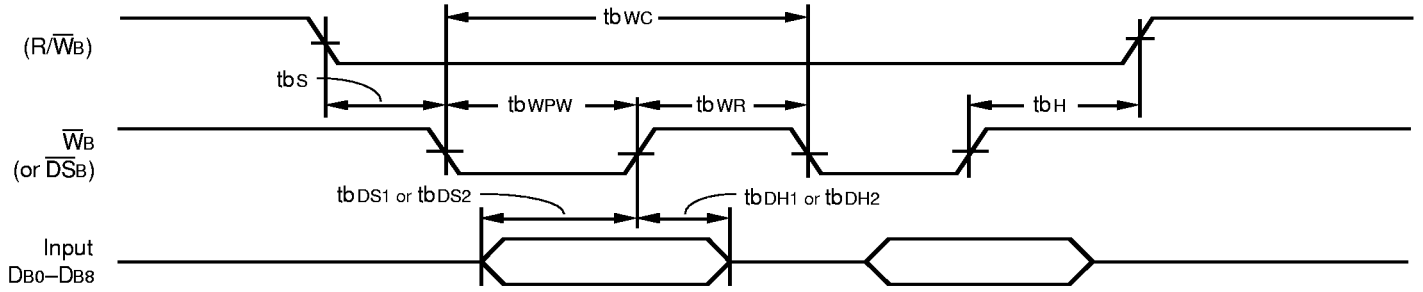


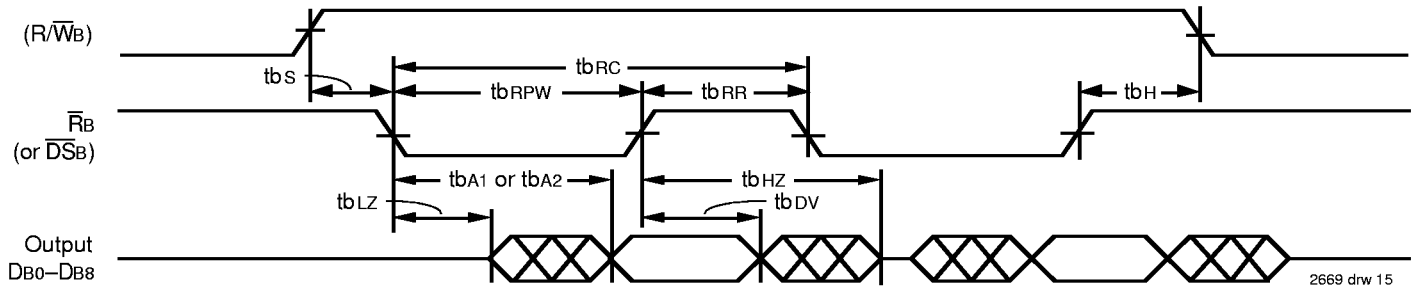
Figure 12. Read and Write Timing for Port A

WRITE



NOTES:
1. tbDS1 and tbDH1 are with parity checking or if parity is ignored, tbDS2 and tbDH2 are with parity generation.
2. RB = 1

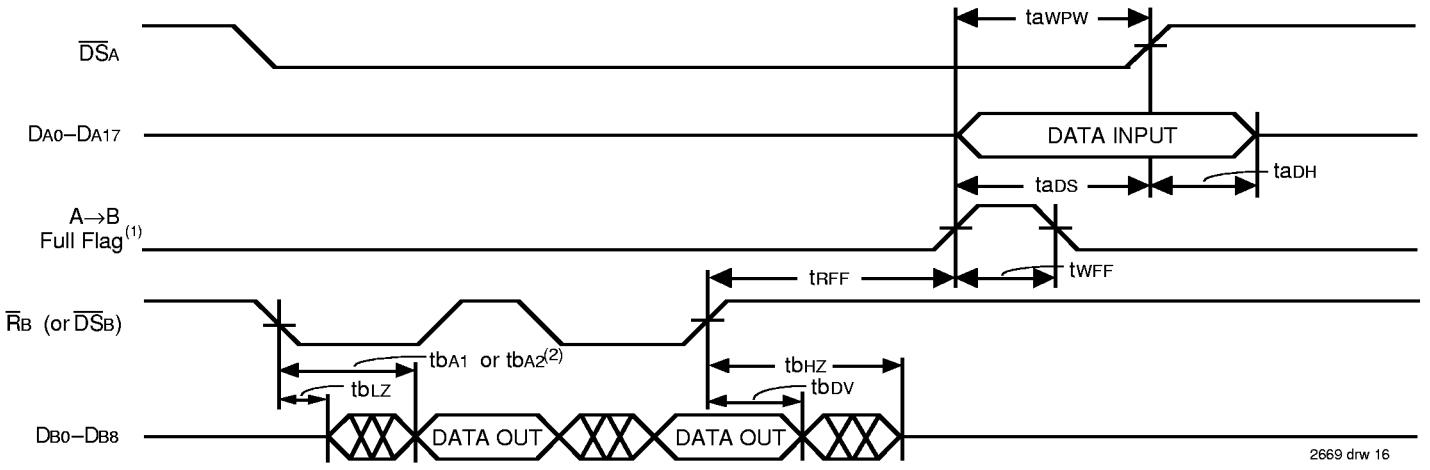
READ



NOTES:
1. tbA1 is with parity checking or if parity is ignored, tbA2 is with parity generation.
2. RB = 1

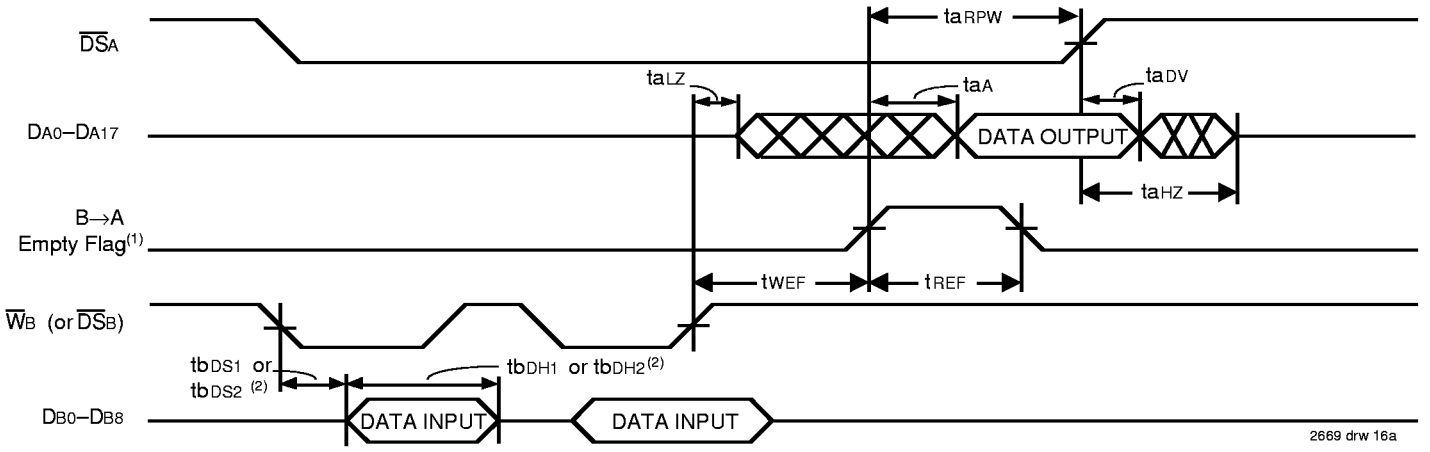
Figure 13. Port B Read and Write Timing, Processor Interface Mode Only

A→B FIFO WRITE FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active LOW.
2. tbA1 is with parity checking or if parity is ignored, tbA2 is with parity generation.
3. R/WA = 0

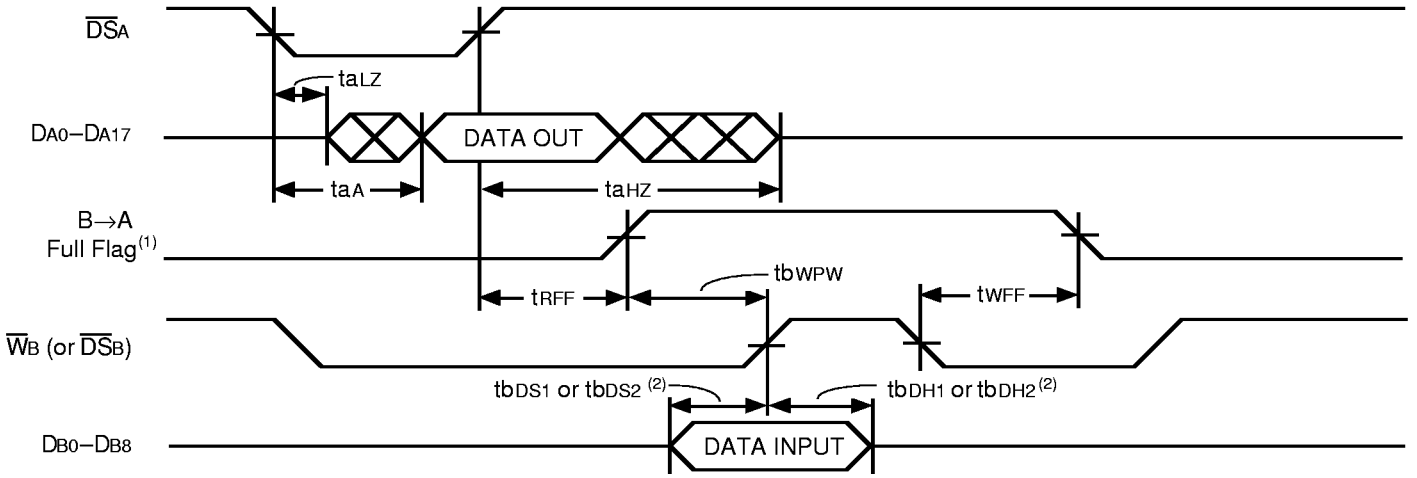
B→A FIFO READ FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active LOW.
2. tbDS1 & tbDH1 are with parity checking or if parity is ignored, tbDS2 & tbDH2 is with parity generation.
3. R/WA = 1

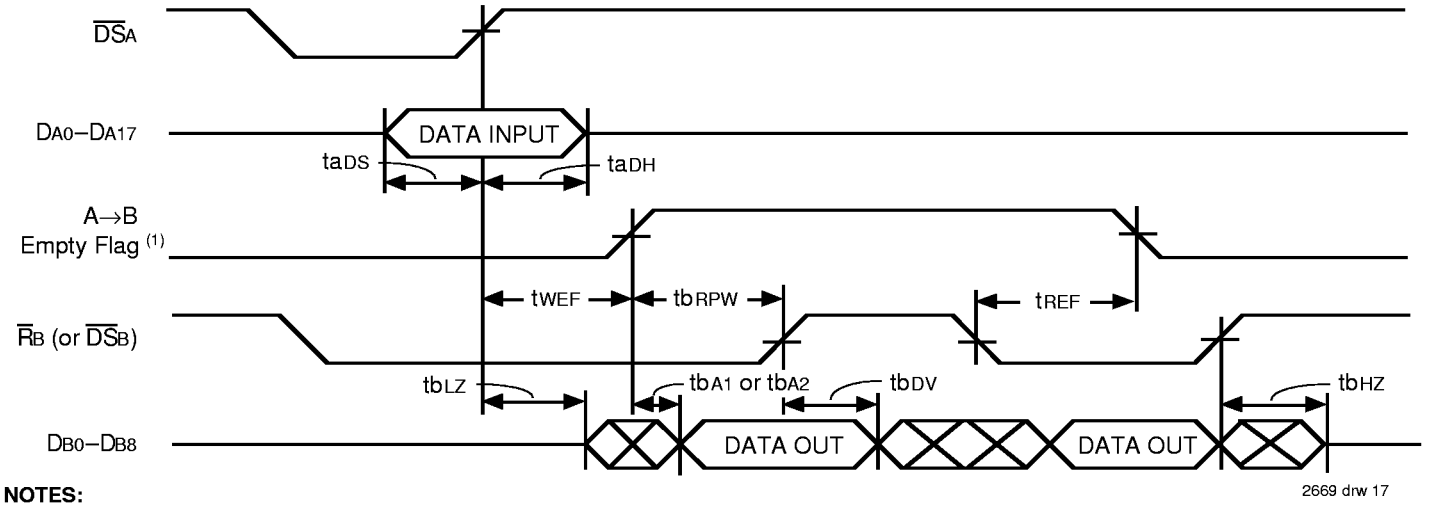
Figure 14. Port A Read and Write Flow-Through Timing, Processor Interface Mode Only

B→A FIFO WRITE FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active LOW.
2. tbDS1 & tbDH1 are with parity checking or if parity is ignored, tbDS2 & tbDH2 are with parity generation.
3. R/WA = 1

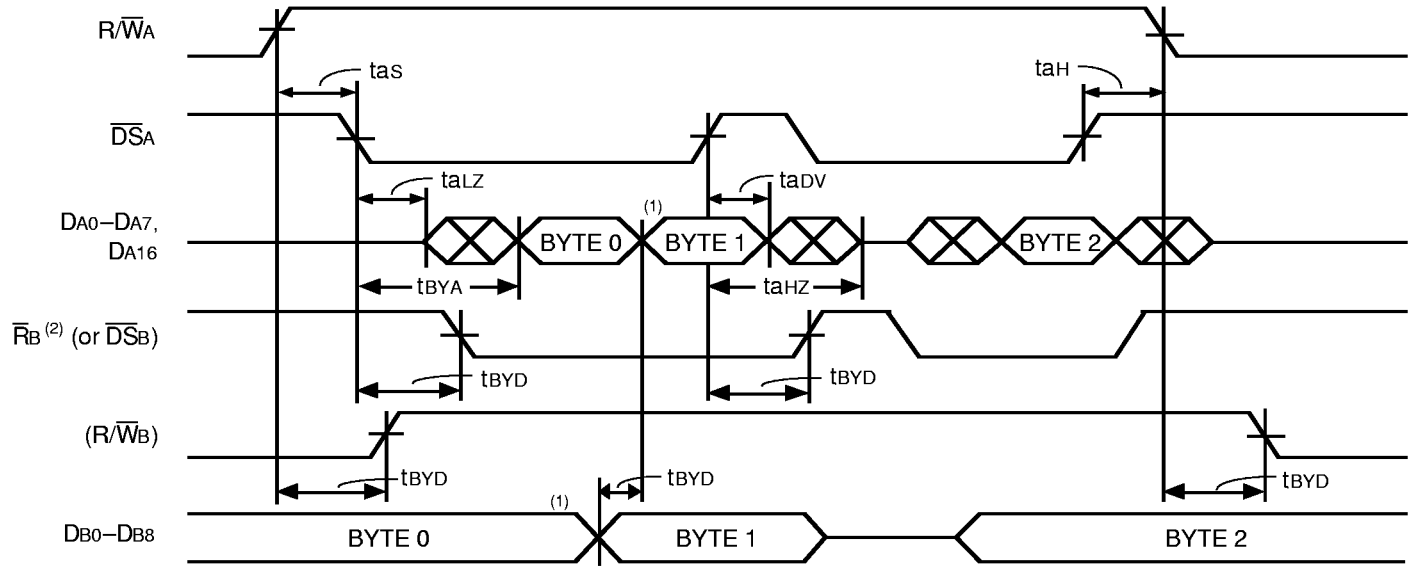
A→B FIFO READ FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active LOW.
2. tbA1 is with parity checking or if parity is ignored, tbA2 is with parity generation.
3. R/WA = 0

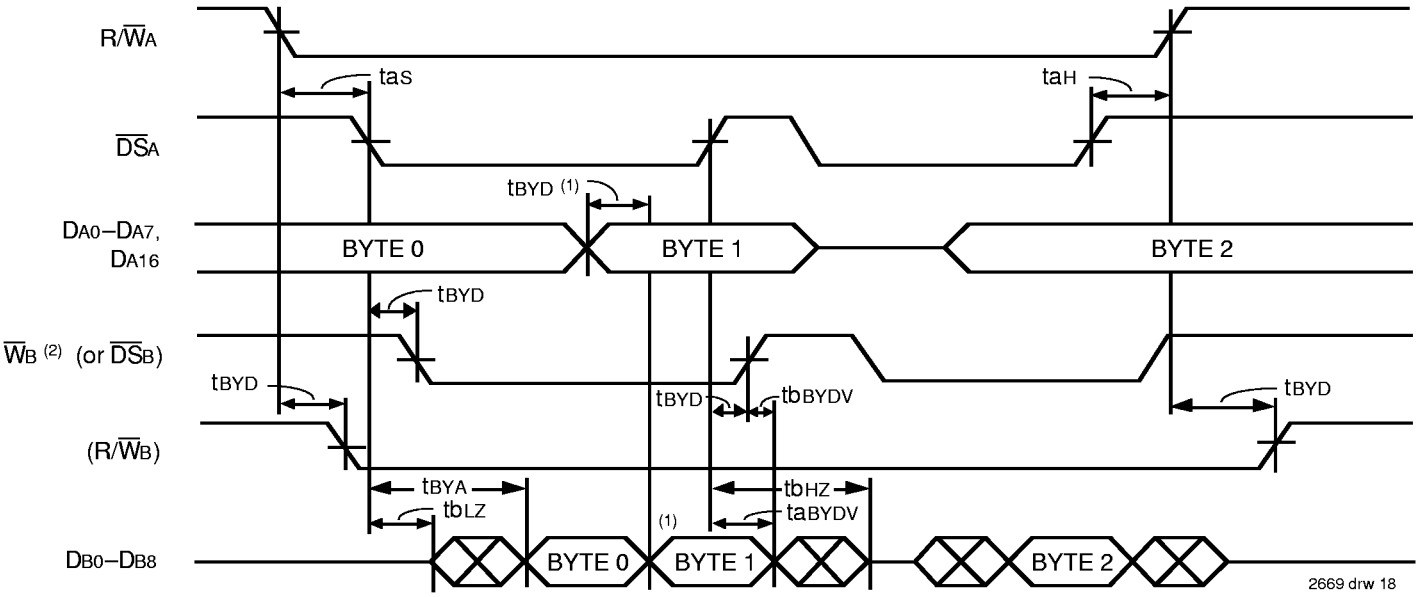
Figure 15. Port B Read and Write Flow-Through Timing

B→A READ BYPASS



NOTES:
1. Once the bypass starts, any data changes on Port B bus (Byte 0→Byte 1) will be passed to Port A bus.
2. WB = 1.

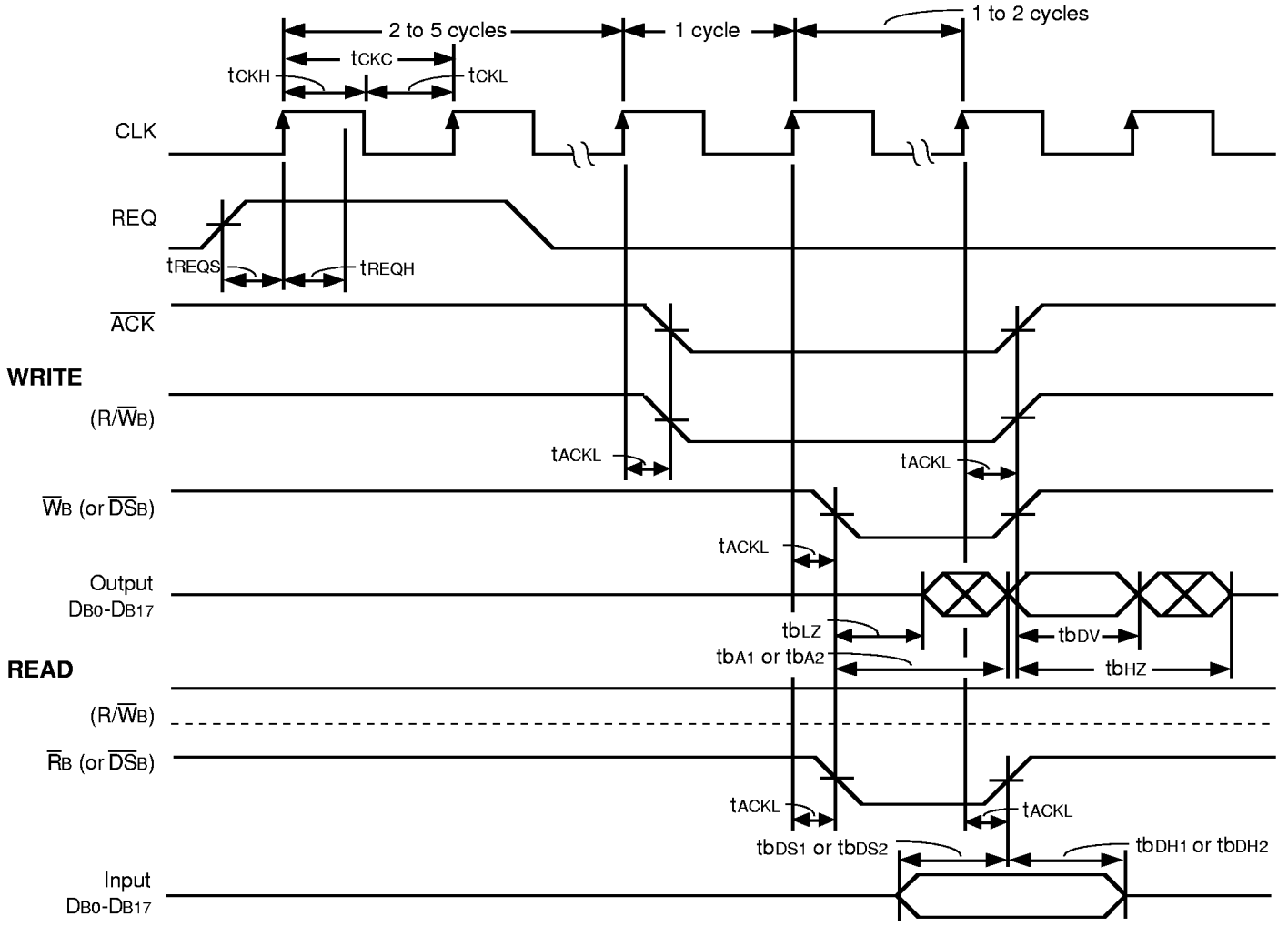
A→B WRITE BYPASS



NOTES:
1. Once the bypass starts, any data changes on Port A bus (Byte 0→Byte 1) will be passed to Port B bus.
2. RB = 1.

Figure 16. Bypass Path Timing. BiFIFO Must be in Peripheral Interface Mode.

SINGLE WORD DMA TRANSFER



NOTES:
1. tbA1, tbDS1and tbDH1are with parity checking or if parity is ignored, tbA2 & tbDS2 and tbDH2 are with parity.

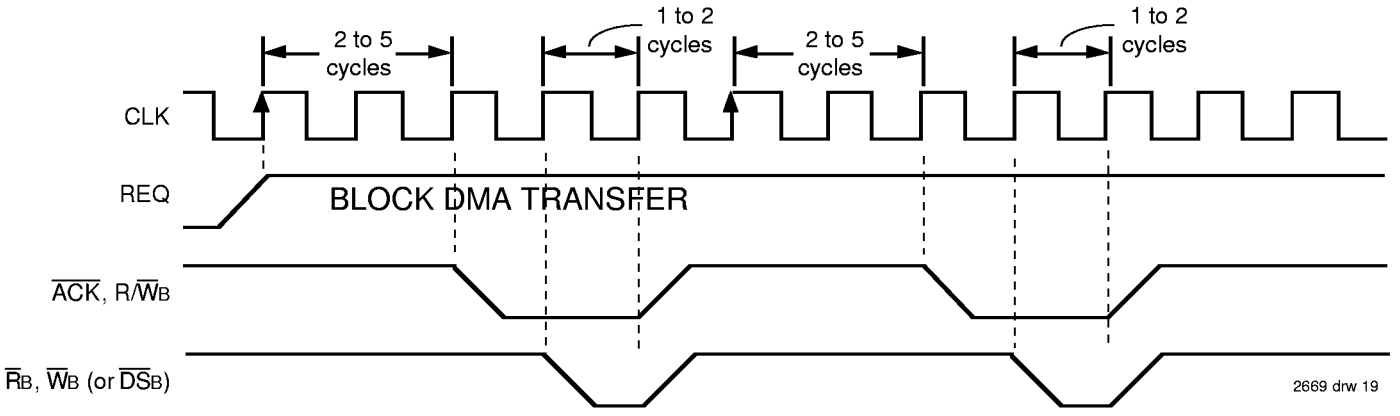


Figure 17. Port B Read and Write DMA Timing, Peripheral Interface Mode Only

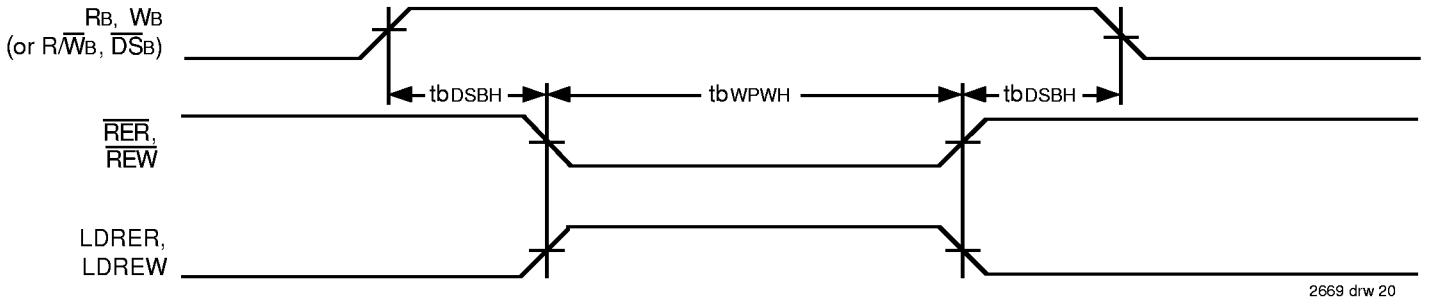
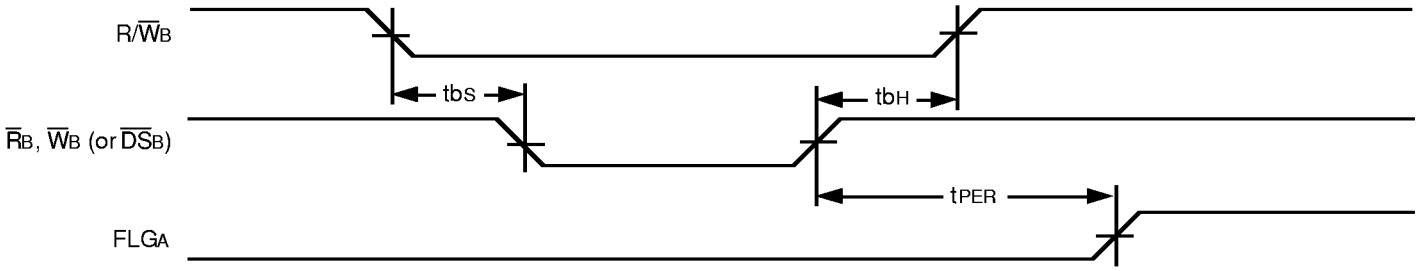
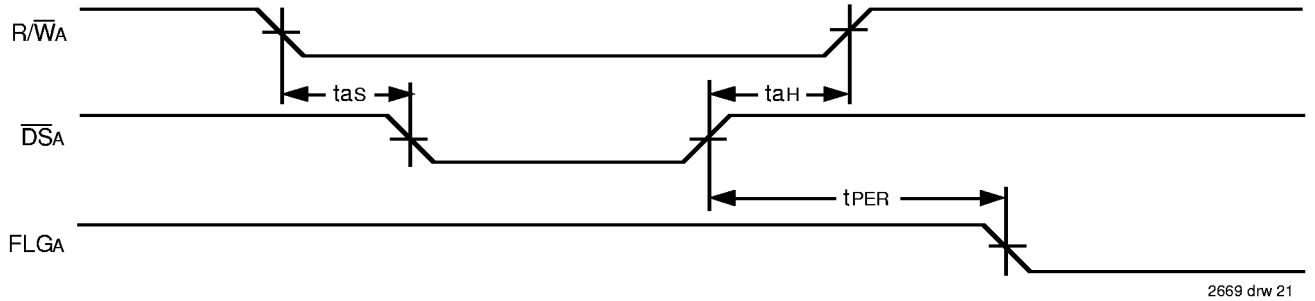


Figure 18. Port B Reread and Rewrite Timing for Intelligent Retransmit

SET PARITY ERROR: FLGA IS ASSIGNED AS THE PARITY ERROR PIN

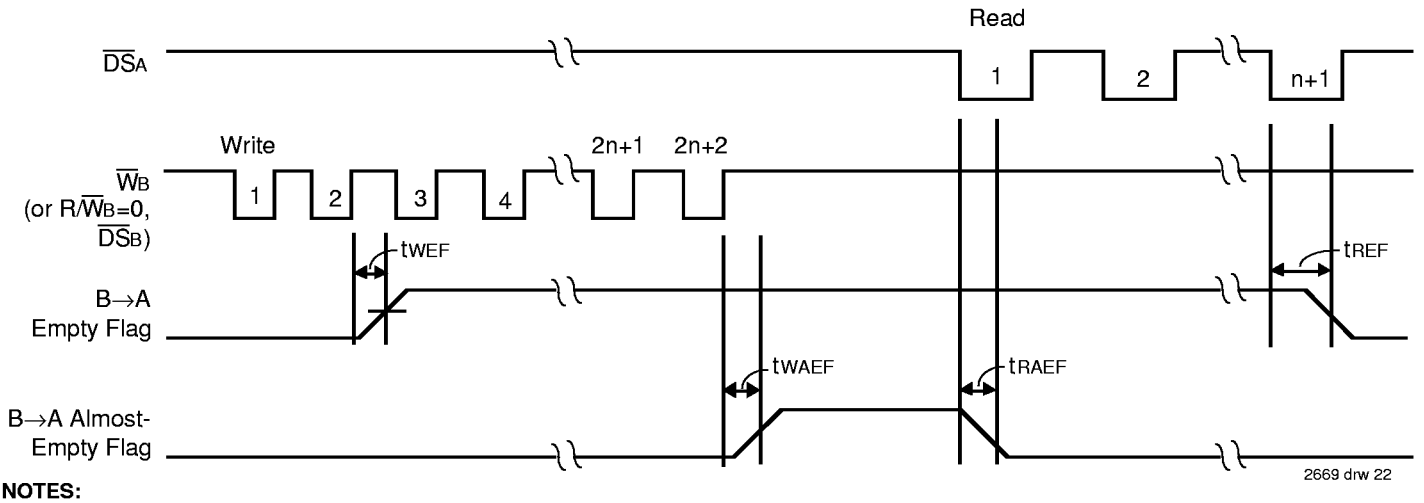


CLEAR PARITY ERROR: COMMAND WRITTEN INTO PORT A CLEARS PARITY ERROR ON FLGA PIN



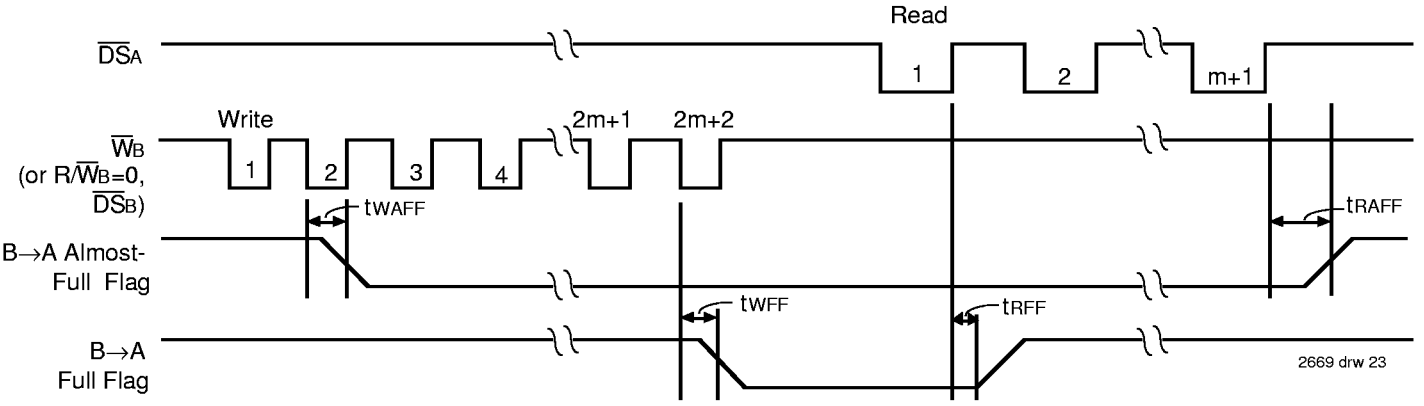
NOTE:
1. FLGA is the only pin that can be assigned as a parity error output.

Figure 19. Port B Parity Error Timing



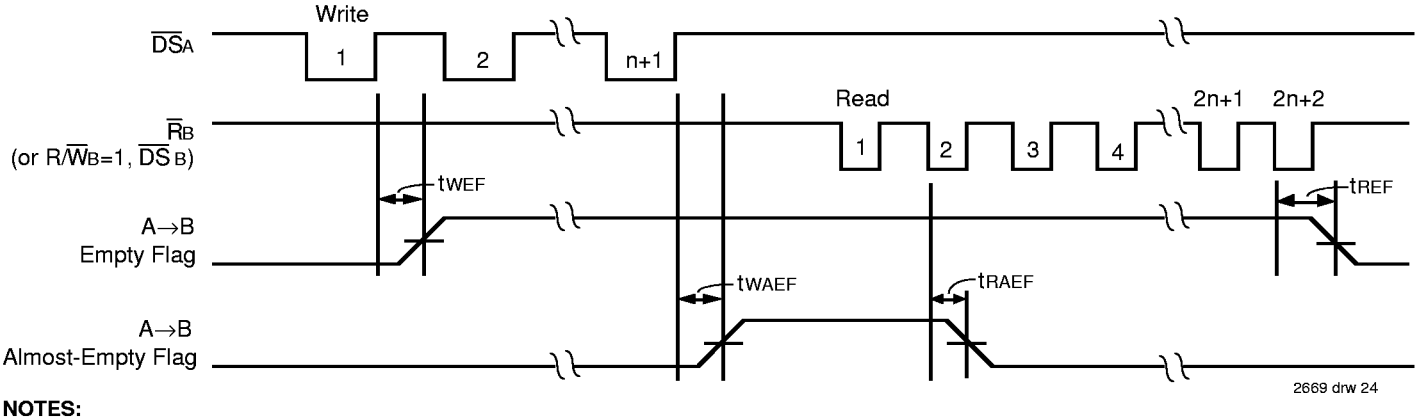
NOTES:
1. B→A FIFO is initially empty.
2. Assume the flag pins are programmed active LOW.
3. For stand-alone mode only; in a 36- to 9-bit configuration, Port B reads must be doubled.
4. R/WA = 1

Figure 20. Empty and Almost-Empty Flag Timing for B→A FIFO. (n = Programmed Offset)



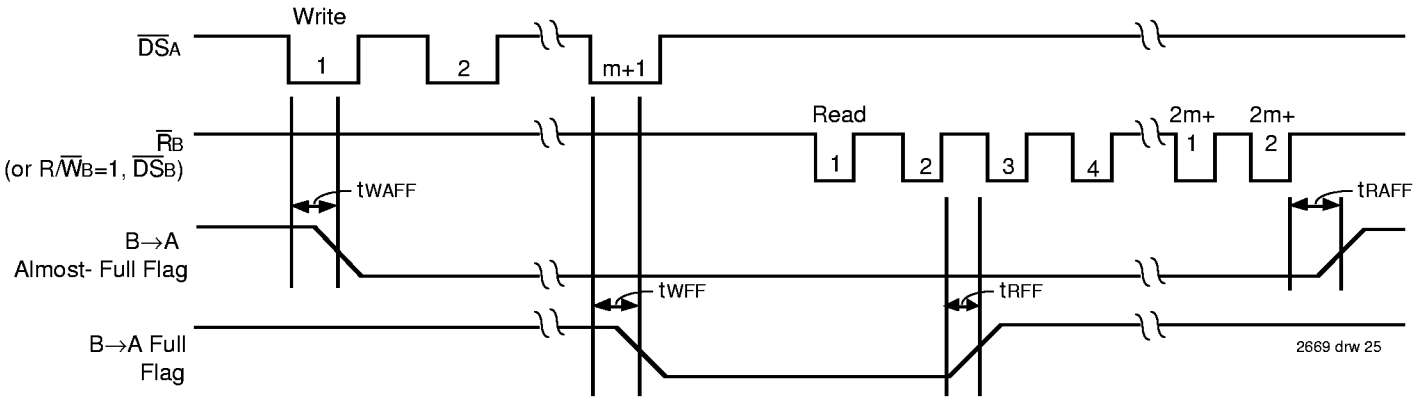
NOTES:
1. B→A FIFO initially contains D–(M+1) data words. D = 512 for IDT 72510; D = 1,024 for IDT72520.
2. Assume the flag pins are programmed active LOW.
3. For stand-alone mode only; in a 36- to 9-bit configuration, Port B reads must be doubled.
4. R/WA = 1

Figure 21. Full and Almost-Full Flag Timing for B→A FIFO. (m = Programmed Offset)



NOTES:
1. A→B FIFO is initially empty.
2. Assume the flag pins are programmed active LOW.
3. For stand-alone mode only; in a 36- to 9-bit configuration, Port B reads must be doubled.
4. R/WA = 1

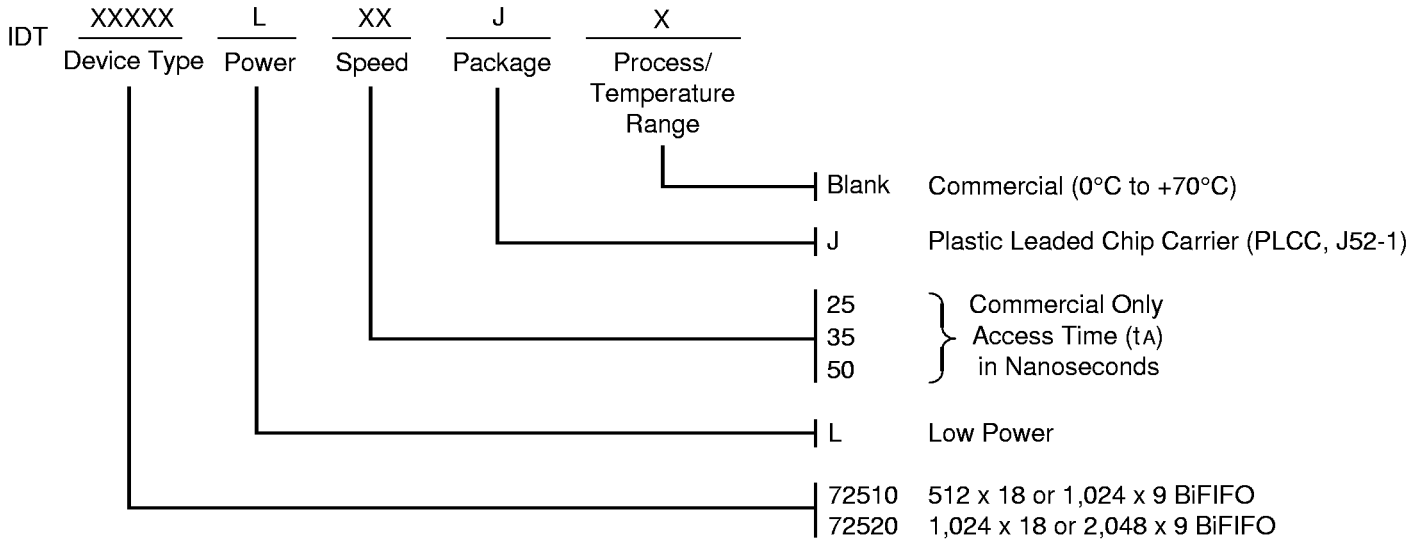
Figure 22. Empty and Almost-Empty Flag Timing for A→B FIFO. (n = Programmed Offset)



NOTES:
1. A→B FIFO initially contains D–(M+1) data words. D = 512 for IDT 72510; D = 1,024 for IDT72520.
2. Assume the flag pins are programmed active LOW.
3. For stand-alone mode only; in a 36- to 9-bit configuration, Port B reads must be doubled.
4. R/WA = 0

Figure 23. Full and Almost-Full Flag Timing for A→B FIFO. (m = Programmed Offset)

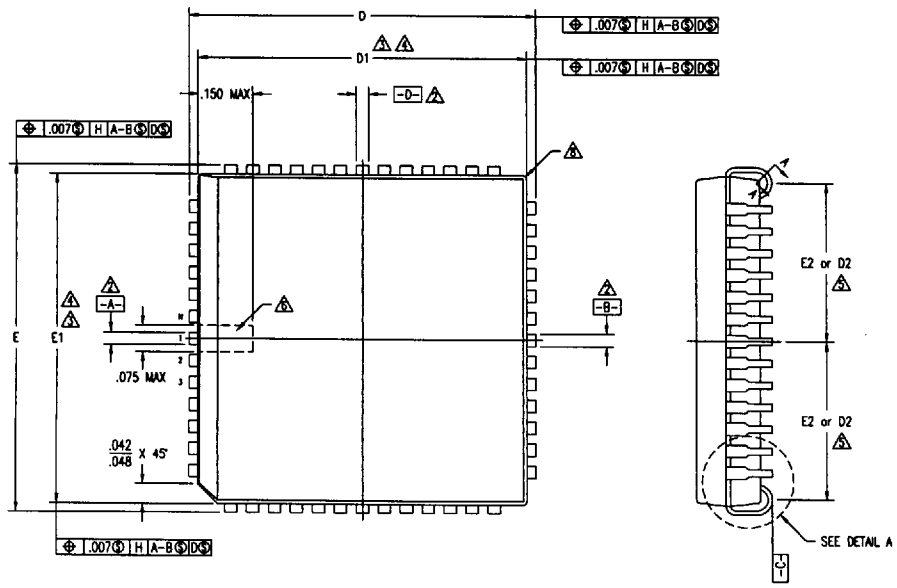
ORDERING INFORMATION

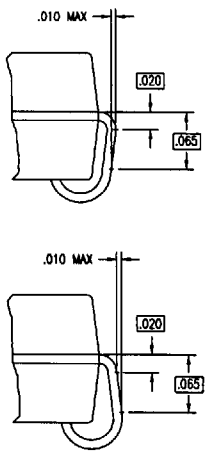


NOTE:
1. Industrial temperature range is available by special order.

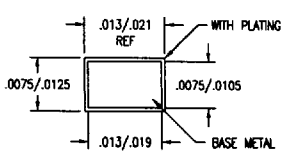
PLCC

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	06	REDRAW TO JEDEC FORMAT	03/15/95	





DETAIL A ⚠



SECTION A-A ⚠

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070
DECIMAL ANGULAR XX± ± XXX± XXXX±		
APPROVALS	DATE	TITLE PL PACKAGE OUTLINE SQUARE PLCC .050 PITCH
DRAWN dd	08/15/88	
CHECKED		SIZE C DRAWING No. PSC-4008 REV 06
		DO NOT SCALE DRAWING

PLCC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	06	REDRAW TO JEDEC FORMAT	03/15/95	

DWG #	J28-1			
SYMBOL	JEDEC VARIATION AB			NOTE
	MIN	NOM	MAX	
A	.165	.172	.180	
A1	.095	.105	.115	
A2	.062	–	.083	
D	.485	.490	.495	
D1	.450	.453	.456	3,4
D2	.195	.205	.215	5
E	.485	.490	.495	
E1	.450	.453	.456	3,4
E2	.191	.205	.219	5
N	28			

DWG #	J44-1			
JEDEC VARIATION AC				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.062	–	.083		
.685	.690	.695		
.650	.653	.656	3,4	
.295	.305	.315	5	
.685	.690	.695		
.650	.653	.656	3,4	
.291	.305	.319	5	
44				

DWG #	J52-1			
JEDEC VARIATION AD				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.062	–	.083		
.785	.790	.795		
.750	.753	.756	3,4	
.345	.355	.365	5	
.785	.790	.795		
.750	.753	.756	3,4	
.341	.355	.369	5	
52				

DWG #	J68-1			
JEDEC VARIATION AE				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.062	–	.083		
.985	.990	.995		
.950	.953	.956	3,4	
.445	.455	.465	5	
.985	.990	.995		
.950	.953	.956	3,4	
.441	.455	.469	5	
68				

DWG #	J84-1			
JEDEC VARIATION AF				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.059	–	.080		
1.185	1.190	1.195		
1.150	1.154	1.156	3,4	
.545	.555	.565	5	
1.185	1.190	1.195		
1.150	1.154	1.156	3,4	
.541	.555	.569	5	
84				

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
3. DIMENSIONS D1 AND E1 ARE TO BE DETERMINED AT DATUM PLANE [-H-]
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .010 PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
5. DIMENSIONS D2 AND E2 ARE TO BE DETERMINED AT SEATING PLANE [-C-] CONTACT POINT
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .007 TOTAL MAXIMUM PER LEAD
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS DETERMINE THE MAXIMUM ANGLE OF THE LEAD FOR SOCKET APPLICATIONS
10. ALL DIMENSIONS ARE IN INCHES
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-018, VARIATION AB, AC, AD, AE & AF. EXCEPTIONS: JEDEC MAXIMUM BASE METAL LEAD WIDTH IS .018

TOLERANCES UNLESS SPECIFIED		
DECIMAL	ANGULAR	
XX±	±	
XXX±		
XXXX±		

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

APPROVALS	DATE
DRAWN AA	06/15/95
CHECKED	

TITLE: PL PACKAGE OUTLINE
SQUARE PLCC
.050 PITCH

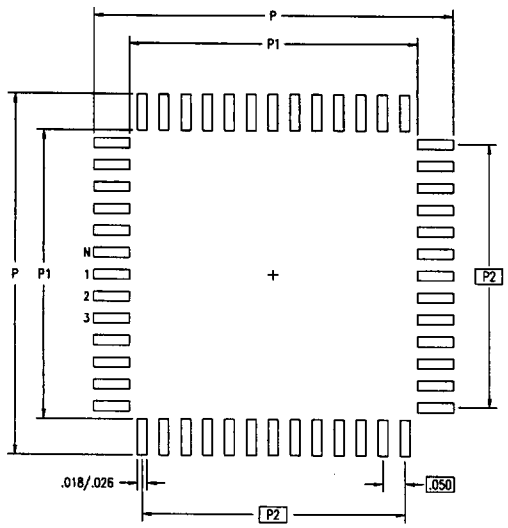
SIZE	DRAWING No.	REV
C	PSC-4008	06

DO NOT SCALE DRAWING

PLCC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	08	REDRAW TO JEDEC FORMAT	03/15/95	

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	.520	.528	.720	.728	.820	.828	1.020	1.028	1.220	1.228
P1	.354	.362	.554	.562	.654	.662	.854	.862	1.054	1.062
P2	.300 BSC		.500 BSC		.600 BSC		.800 BSC		1.000 BSC	
N	28		44		52		68		84	

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL XX± XXX± XXXX±	ANGULAR ±		
APPROVALS	DATE	TITLE PL PACKAGE OUTLINE SQUARE PLCC .050 PITCH	
DRAWN dd	08/15/89		
CHECKED		SIZE C	DRAWING No. PSC-4008 REV 06
		DO NOT SCALE DRAWING	