8-Bit Buffer Transceivers
SN54LS645

Features/Benefits

- **Three-state outputs drive bus lines**
- **Low current PNP inputs reduce loading**
- **Symmetric — equal driving capability in each direction**
- **8-bit data path matches byte boundaries**
- **Ideal for microprocessor interface**

Ordering Information

PART NUMBER	TYPE	TEMP	POLARITY	POWER
SN54LS645	J,L,W	Mil	Noninvert	LS

Description

These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The enable input ($\overline{E}$) can be used to disable the device so that the buses are effectively isolated.

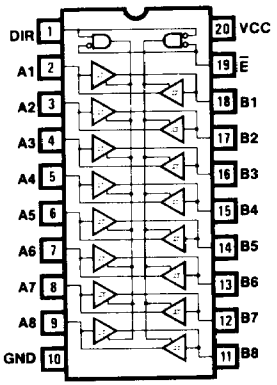
All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

Function Table

ENABLE $\overline{E}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolated

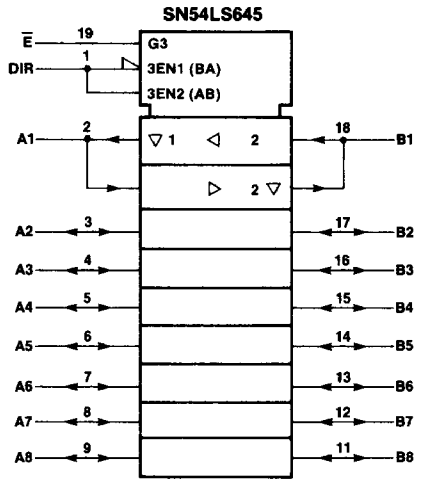
Logic Symbol

SN54LS645



IEEE Symbol

SN54LS645



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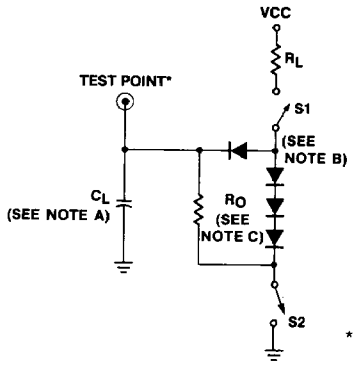
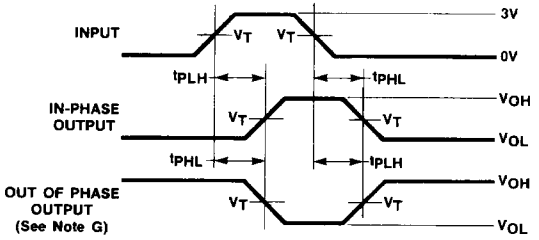
TWX: 910-338-2376
Monolithic Memories AMI

Test Load

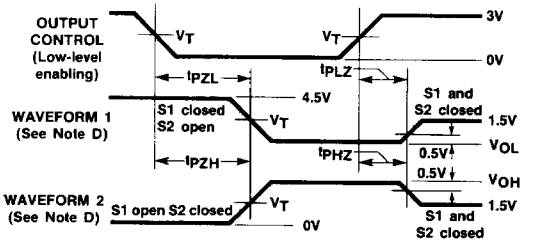


* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



Propagation Delay



Enable and Disable

V_T = 1.3 V

Notes: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. For Series 54LS, R_O = 5 K, V_T = 1.3 V.

D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{OUT} = 50 Ω and:
For series 54S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
For Series 54LS, $t_R \leq 15$ ns, $t_F \leq 6$ ns.

G. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

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