

55/75471 • 55/75472 • 55/75473 • 55/75474

DUAL HIGH VOLTAGE HIGH CURRENT PERIPHERAL DRIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 55/75471 series are dual very high voltage interface peripheral drivers with medium switching speeds. These devices are pin-for-pin replacements of the (55/75451A-55/75454A), (55/75461-55/75464) and the (DS3611-DS3614) peripheral drivers.

The 55/75471 peripheral driver series converts TTL and DTL logic levels to high voltage, high current levels.

The 55/75471, 55/75472, 55/75473 and 55/75474 feature two standard TTL input gates in AND, NAND, OR and NOR configurations respectively. The logic gates are internally connected to the bases of the npn transistors.

The 55/75471 series offers flexibility in designing very high voltage logic buffers, power drivers, lamp drivers, line drivers and relay drivers.

- HIGH VOLTAGE OUTPUT (80 V)
- NO LATCH-UP AT 55 V
- HIGH SPEED SWITCHING
- HIGH OUTPUT CURRENT CAPABILITY
- TTL OR DTL INPUT COMPATIBILITY
- INPUT CLAMP DIODES
- +5 V SUPPLY VOLTAGE

TEST TABLE 1 — Operating Temperature Range and Supply Voltage Range

	55471 Series	75471 Series
Temperature, T_A	-55°C to +125°C	0°C to 70°C
Supply Voltage, V_{CC}	+4.5 V to +5.5 V	+4.75 V to +5.25 V

ABSOLUTE MAXIMUM RATINGS

	55471 55472 55473 55474	75471 74572 75473 75474
Supply Voltage, V_{CC} (See Note 1)	7.0 V	7.0 V
Input Voltage (See Note 1)	5.5 V	5.5 V
Interemitter Voltage (See Note 2)	5.5 V	5.5 V
Output Voltage (See Notes 1 and 3)	80 V	80 V
Continuous Collector Current (See Note 4)		
Continuous Output Current (See Note 4)	300 mA	300 mA
Continuous Total Power Dissipation (See Note 5)	800 mW	800 mW
Operating Free-Air Temperature Range	-55°C to +125°C	0°C to 70°C
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C
Pin Temperature		
Molded DIP (Soldering, 10 s)	260°C	260°C
Hermetic DIP (Soldering, 60 s)	300°C	300°C

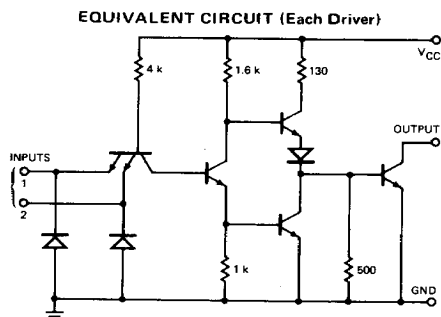
NOTES:

1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter input transistor.
3. This is the maximum voltage which should be applied to any output when it is in the off state.
4. Both halves of these dual circuits may conduct rated current simultaneously.
5. Above 60°C ambient temperature, derate linearly at 8.3 mW/°C for Hermetic DIP and Molded DIP. For the Molded Mini DIP and Hermetic Mini DIP, derate at 6.7 mW/°C above 30°C.

FAIRCHILD • 55471/75471 SERIES

55471/75471

DUAL POSITIVE AND PERIPHERAL DRIVER



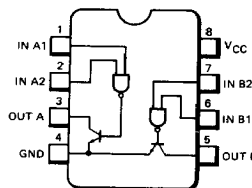
Component values shown are nominal. All resistor values in ohms.

TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	L	(on state)
L	H	L	(on state)
H	L	L	(on state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

CONNECTION DIAGRAMS
8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



ORDER INFORMATION

TYPE	PART NO.
55471	55471RM
75471	75471RC
75471	75471TC

Positive Logic: Z = XY

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP (Note 6)	MAX	UNITS
V _{IH}	Input HIGH Voltage	1		2.0			V
V _{IL}	Input LOW Voltage	1				0.8	V
V _{CD}	Input Clamp Diode Voltage	2	V _{CC} = MIN, I _I = -12 mA		-1.2	-1.5	V
I _{OH}	Output HIGH Current	1	V _{CC} = MIN, V _{OH} = 80 V V _{IH} = 2 V	55471 75471		300 100	μA
V _{OL}	Output LOW Voltage	1	V _{CC} = MIN, V _{IL} = 0.8 V I _{OL} = 100 mA V _{CC} = MIN, V _{IL} = 0.8 V I _{OL} = 300 mA	55471 75471 55471 75471	0.16 0.16 0.35 0.35	0.5 0.4 0.8 0.7	V
I _I	Input Current at Maximum Input Voltage	3	V _{CC} = MAX, V _I = 5.5 V			1.0	mA
I _{IH}	Input HIGH Current	3	V _{CC} = MAX, V _I = 2.4 V			40	μA
I _{IL}	Input LOW Current	2	V _{CC} = MAX, V _I = 0.4 V		-1.0	-1.6	mA
I _{CCH}	Supply Current, Output HIGH	4	V _{CC} = MAX, V _I = 5 V		8.0	11	mA
I _{CCL}	Supply Current Output LOW		V _{CC} = MAX, V _I = 0 V		61	76	mA

NOTE 6. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

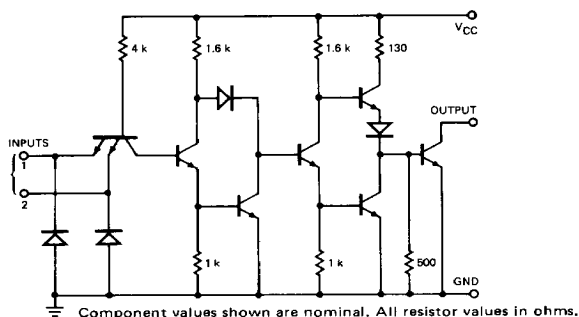
SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t _{PLH}	Propagation Delay Time, Output LOW to HIGH	6	I _O ≈ 200 mA, C _L = 15 pF, R _L = 50 Ω		30	55	ns
t _{PHL}	Propagation Delay Time, Output HIGH to LOW				25	40	ns
t _{TLH}	Transition Time, Output LOW to HIGH				8.0	20	ns
t _{THL}	Transition Time, Output HIGH to LOW				10	20	ns
V _{OH}	HIGH Level Output Voltage After Switching	7	V _S = 55 V, I _O ≈ 300 mA	V _S - 18			mV



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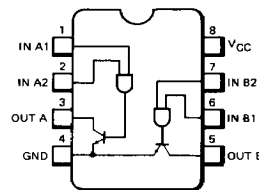
55472/75472 DUAL POSITIVE NAND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



CONNECTION DIAGRAMS

**8-PIN DIP
(TOP VIEW)**
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	H	(off state)
L	H	H	(off state)
H	L	H	(off state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level.

ORDER INFORMATION

TYPE	PART NO.
55472	55472RM
75472	75472RC
75472	75472TC

Positive Logic: Z = \overline{XY}

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS	
V_{IH}	Input HIGH Voltage	1		2.0			V	
V_{IL}	Input LOW Voltage	1				0.8	V	
V_{CD}	Input Clamp Diode Voltage	2	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$		-1.2	-1.5	V	
I_{OH}	Output HIGH Current	1	$V_{CC} = \text{MIN}, V_{OH} = 80 \text{ V}$ $V_{IL} = 0.8 \text{ V}$	55472		300	μA	
				75472		100		
V_{OL}	Output LOW Voltage	1	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}$ $I_{OL} = 100 \text{ mA}$	55472	0.16	0.5	V	
				75472	0.16	0.4		
				$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}$ $I_{OL} = 300 \text{ mA}$	55472	0.35		0.8
					75472	0.35		0.7
I_I	Input Current at Maximum Input Voltage	3	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1.0	mA	
I_{IH}	Input HIGH Current	3	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μA	
I_{IL}	Input LOW Current	2	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1.0	-1.6	mA	
I_{CCH}	Supply Current, Output HIGH	4	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		13	17	mA	
				$V_{CC} = \text{MAX}, V_I = 5 \text{ V}$		65		76
I_{CCL}	Supply Current Output LOW		$V_{CC} = \text{MAX}, V_I = 5 \text{ V}$				mA	

NOTE 7. All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

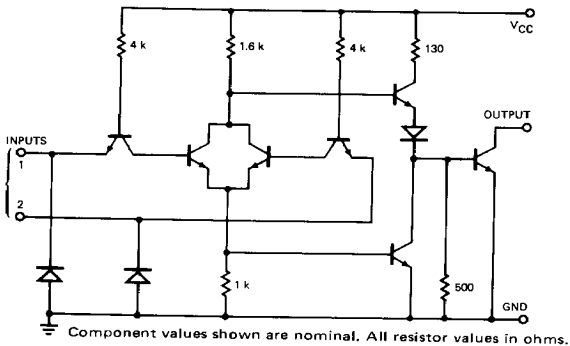
AC CHARACTERISTICS: $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	6	$I_O \approx 200 \text{ mA}, C_L = 15 \text{ pF}$ $R_L = 50 \Omega$		45	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				30	50	
t_{TLH}	Transition Time, Output LOW to HIGH				13	25	
t_{THL}	Transition Time, Output HIGH to LOW				10	20	
V_{OH}	HIGH Level Output Voltage After Switching	7	$V_{SS} = 55 \text{ V}, I_O \approx 300 \text{ mA}$	$V_S - 18$			mV

FAIRCHILD • 55471/75471 SERIES

55473/75473 DUAL POSITIVE OR PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	L	(on state)
L	H	H	(off state)
H	L	H	(off state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP (Note 8)	MAX	UNITS	
V_{IH}	Input HIGH Voltage	1		2.0			V	
V_{IL}	Input LOW Voltage	1				0.8	V	
V_{CD}	Input Clamp Diode Voltage	2	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$		-1.2	-1.5	V	
I_{OH}	Output HIGH Current	1	$V_{CC} = \text{MIN}, V_{OH} = 80 \text{ V}$ $V_{IH} = 2 \text{ V}$	55473		300	μA	
				75473		100		
V_{OL}	Output LOW Voltage	1	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}$ $I_{OL} = 100 \text{ mA}$	55473	0.18	0.5	V	
				75473	0.18	0.4		
				55473	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}$ $I_{OL} = 300 \text{ mA}$	0.39		0.8
						75473		0.39
I_I	Input Current at Maximum Input Voltage	3	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1.0	mA	
I_{IH}	Input HIGH Current	3	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μA	
I_{IL}	Input LOW Current	2	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1.0	-1.6	mA	
I_{CCH}	Supply Current, Output HIGH	5	$V_{CC} = \text{MAX}, V_I = 5 \text{ V}$		8.0	11	mA	
				$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		63		76
I_{CCL}	Supply Current Output LOW		$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$				mA	

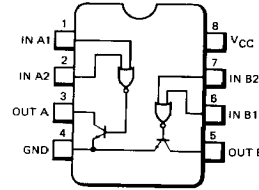
NOTE 8. All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

AC CHARACTERISTICS: $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	6	$I_O \approx 200 \text{ mA}, C_L = 15 \text{ pF}$ $R_L = 50 \Omega$		30	55	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				25	40	
t_{TLH}	Transition Time, Output LOW to HIGH				8	25	
t_{THL}	Transition Time, Output HIGH to LOW				10	25	
V_{OH}	HIGH Level Output Voltage After Switching	7	$V_S = 55 \text{ V}, I_O \approx 300 \text{ mA}$	$V_S - 18$			mV

CONNECTION DIAGRAMS

**8-PIN DIP
(TOP VIEW)**
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



ORDER INFORMATION

TYPE	PART NO.
55473	55473RM
75473	75473RC
75473	75473TC

Positive Logic: $Z = X + Y$

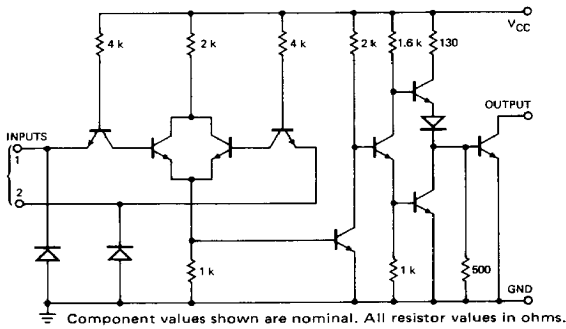
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FAIRCHILD • 55471/75471 SERIES

55474/75474

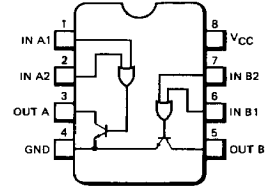
DUAL POSITIVE NOR PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



CONNECTION DIAGRAMS

8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	H	(off state)
L	H	L	(on state)
H	L	L	(on state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55474	55474RM
75474	75474RC
75474	75474TC

Positive Logic: $Z = \overline{X + Y}$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP (Note 9)	MAX	UNITS	
V_{IH}	Input HIGH Voltage	1		2.0			V	
V_{IL}	Input LOW Voltage	1				0.8	V	
V_{CD}	Input Clamp Diode Voltage	2	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V	
I_{OH}	Output HIGH Current	1	$V_{CC} = \text{MIN}, V_{OH} = 80 \text{ V}$ $V_{IL} = 0.8 \text{ V}$	55474		300	μA	
				75474		100		
V_{OL}	Output LOW Voltage	1	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}$ $I_{OL} = 100 \text{ mA}$	55474	0.17	0.5	V	
				75474	0.17	0.4		
				$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}$ $I_{OL} = 300 \text{ mA}$	55474	0.38		0.8
					75474	0.38		0.7
I_I	Input Current at Maximum Input Voltage	3	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1.0	mA	
I_{IH}	Input HIGH Current	3	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μA	
I_{IL}	Input LOW Current	2	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1.0	-1.6	mA	
I_{CCH}	Supply Current, Output HIGH	5	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		14	19	mA	
				$V_{CC} = \text{MAX}, V_I = 5 \text{ V}$		72		85

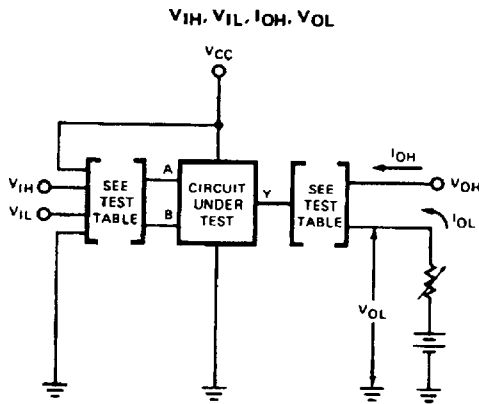
NOTE 9. All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

AC CHARACTERISTICS: $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	6	$I_O \approx 200 \text{ mA}, C_L = 15 \text{ pF},$ $R_L = 50 \Omega$		40	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				30	50	
t_{TLH}	Transition Time, Output LOW to HIGH				8	20	
t_{THL}	Transition Time, Output HIGH to LOW				10	20	
V_{OH}	HIGH Level Output Voltage After Switching	7	$V_S = 55 \text{ V}, I_O \approx 300 \text{ mA}$	$V_S - 18$			mV

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CHARACTERISTICS MEASUREMENT INFORMATION

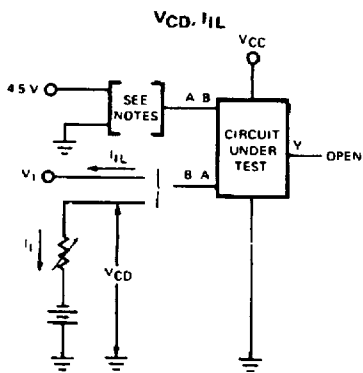


NOTE: Each input is tested separately.

Fig. 1

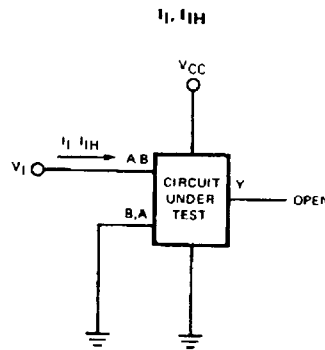
TEST TABLE II

CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
55/75471	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
55/75472	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
55/75473	V_{IH} V_{IL}	GND V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}
55/75474	V_{IH} V_{IL}	GND V_{IL}	I_{OL} V_{OH}	V_{OL} I_{OH}



- NOTES:
- A. Each input is tested separately.
 - B. When testing I_{IL} , 55/75473 and 55/75474, the input not under test is grounded. For all other circuits it is at 4.5 V.
 - C. When testing V_{CD} , input not under test is open.

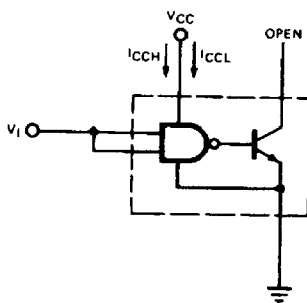
Fig. 2



Each input is tested separately.

Fig. 3

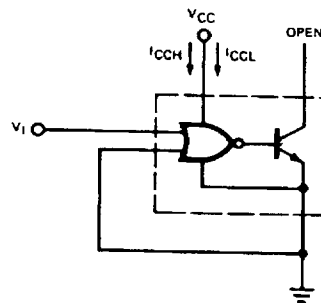
I_{CCH} , I_{CCL} FOR AND, NAND CIRCUITS



Both gates are tested simultaneously.

Fig. 4

I_{CCH} , I_{CCL} FOR OR, NOR CIRCUITS



Both gates are tested simultaneously.

Fig. 5

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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CHARACTERISTICS MEASUREMENT INFORMATION

AC CHARACTERISTICS

SWITCHING TIMES OF COMPLETE DRIVERS

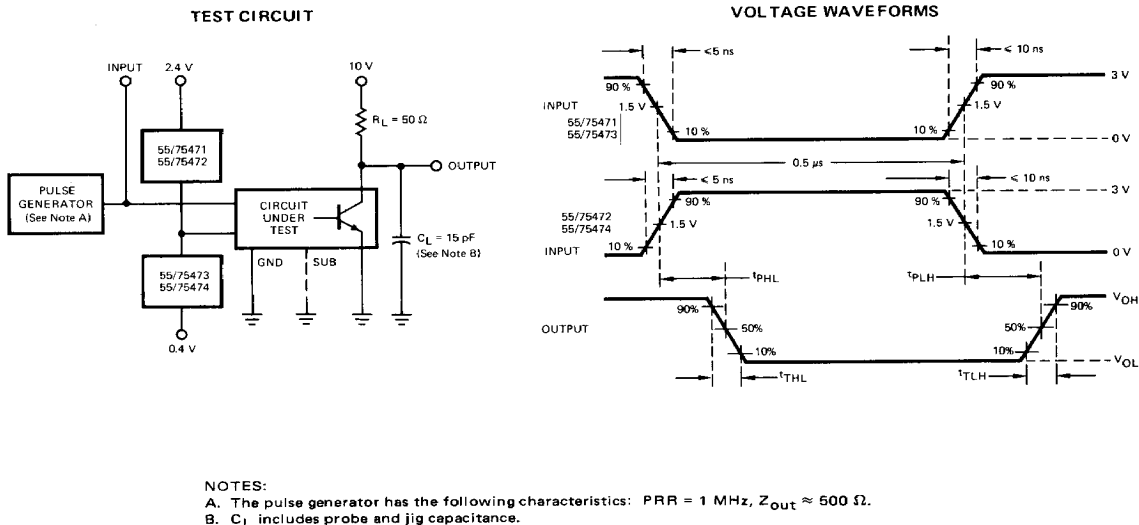


Fig. 6

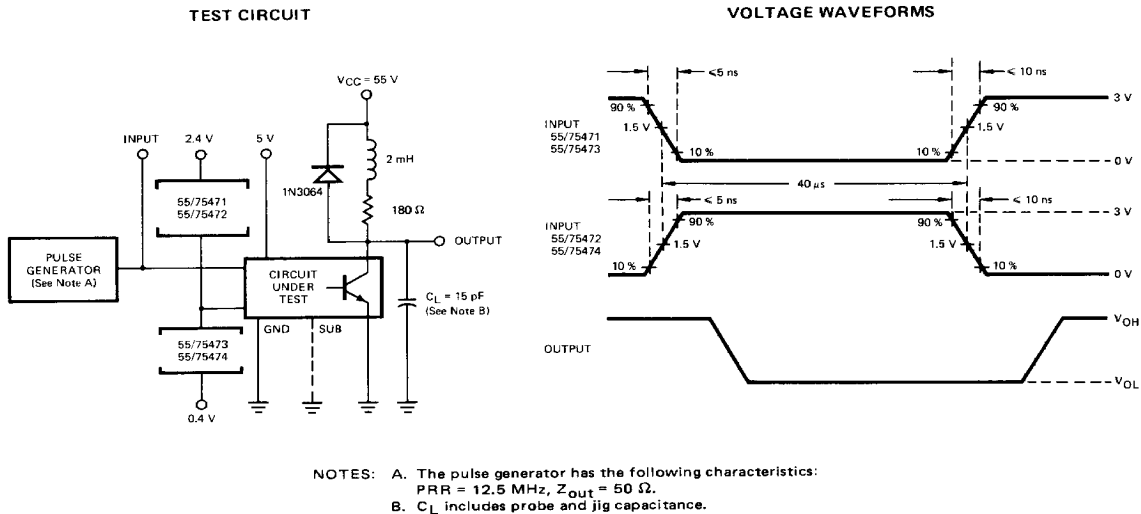


Fig. 7