MOTOROLA

Military 54F191

Advance Information

Synchronous 4-Bit Up/Down Decade Counter With Mode Control

ELECTRICALLY TESTED PER:
MIL-M-38510/34303

The 54F191 is a reversible modulo-16 counter featuring synchronous counting and asynchronous presetting. The preset feature allows the F191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

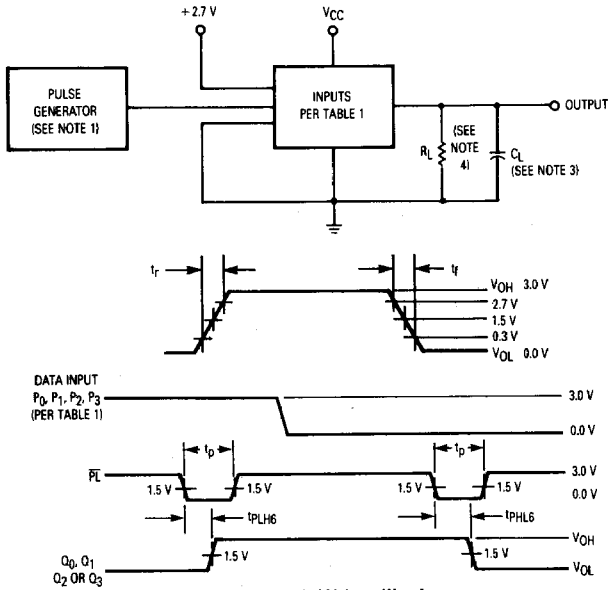
- High-Speed 110 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Parallel Load
- Cascadable

AVAILABLE AS:

1) JAN: *
2) SMD: *
3) 883C: *

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2
***Call Factory for latest update**

TEST CIRCUIT AND WAVEFORMS



Parallel Loaded Voltage Waveforms

NOTES:
1. Pulse generator has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR $\leq$ 1.0 MHz, $Z_{out} \approx 50\ \Omega$.
2. Terminal conditions (pins not designated may be high $\geq$ 2.0 V, low $\leq$ 0.8 V, or open).
3. C_L = 50 pF ± 10%, including scope probe, wiring, and stray capacitance without package in test fixture.
4. R_L = 499 Ω ± 5.0%.
5. Voltage measurements are to be made with respect to network terminal ground.

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
P_1	1	1	2	V_{CC}
Q_1	2	2	3	V_{CC}
Q_0	3	3	4	V_{CC}
$\overline{CE}$	4	4	5	V_{CC}
$\overline{U}/D$	5	5	7	V_{CC}
Q_2	6	6	8	V_{CC}
Q_3	7	7	9	V_{CC}
GND	8	8	10	GND
P_3	9	9	12	V_{CC}
P_2	10	10	13	V_{CC}
$\overline{PL}$	11	11	14	GND
TC	12	12	15	OPEN
$\overline{RC}$	13	13	17	V_{CC}
CP	14	14	18	GND
P_0	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

MODE SELECT TABLE

Inputs				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}/D$	CP	
H	L	L	⎍	Count Up
H	L	H	⎍	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

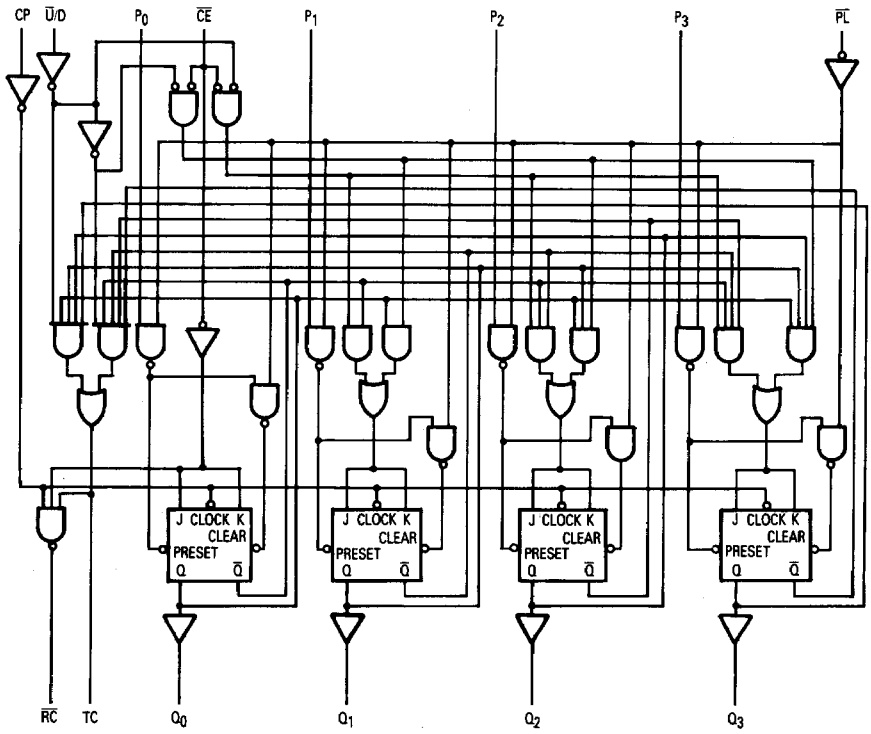
This document contains information on a new product. Specifications and information herein are subject to change without notice.

FUNCTIONAL DESCRIPTION

The F191 is a synchronous up/down 4-Bit binary counter containing four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations. It has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs (P_0–P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table. A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated Synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. $\overline{CE}$ and $\overline{U}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 15 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures A and B. In Figure A, each $\overline{RC}$ output is used as a clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the

LOGIC DIAGRAM

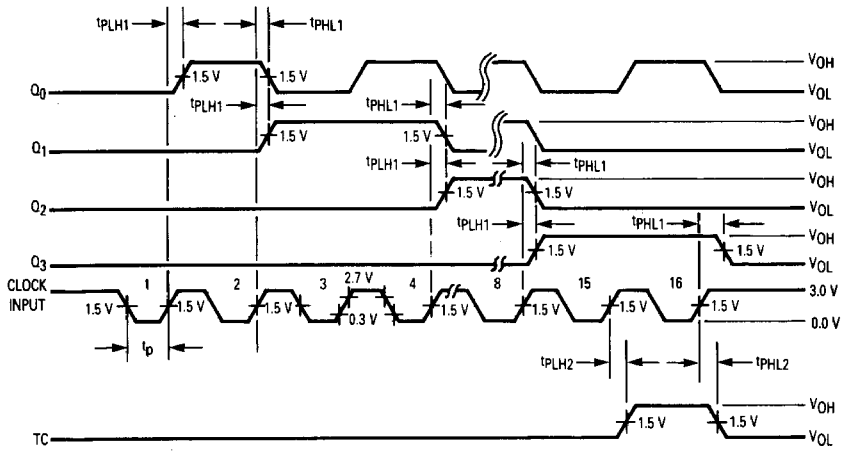


clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure B. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure C avoids ripple delays and their associated restrictions. The $\overline{CE}$ input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures A and B doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

WAVEFORMS

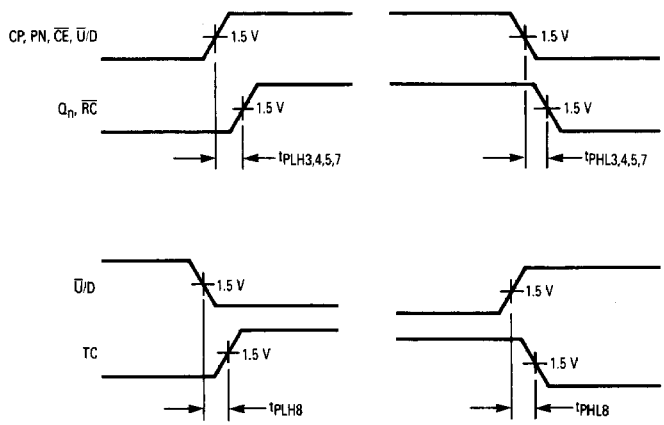


Serial Loaded Voltage Waveforms (Count Up Mode)

RC TRUTH TABLE

Inputs			Outputs
$\overline{CE}$	TC	CP	$\overline{RC}$
L	H	⊓	⊓
H	X	X	H
X	L	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial



Switching Time Waveforms

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IL} = 0.8 V, V_{IH} = 2.0 V.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, $\overline{PL}$ = 5.5 V or (2.7 V), other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, $\overline{PL}$ = 5.5 V or (7.0 V), other inputs are open.
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V, $\overline{PL}$ = 0 V or (0.5 V), other inputs are open.
$I_{IL(CE)}$	Logical "0" Input Current	−0.09	−1.8	−0.09	−1.8	−0.09	−1.8	mA	V_{CC} = 5.5 V, $V_{IN(\overline{U}/D)}$ = 0.5 V, other inputs are open.
I_{OS}	Short Circuit Output Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V or open, V_{OUT} = 0 V, $\overline{PL}$ = 0 V.
I_{CC}	Power Supply Current Off		55		55		55	mA	V_{CC} = 5.5 V, V_{IN} = 0 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output CP to Q_n	5.0	11	5.0	13.5	5.0	13.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH1}	Propagation Delay /Data-Output CP to Q_n	3.0	7.5	3.0	9.5	3.0	9.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL2}	Propagation Delay /Data-Output CP to TC	5.0	11	4.5	13.5	4.5	13.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH2}	Propagation Delay /Data-Output CP to TC	6.0	13	5.0	16.5	5.0	16.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL3}	Propagation Delay /Data-Output CP to $\overline{RC}$	3.0	7.0	3.0	12.5	3.0	12.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH3}	Propagation Delay /Data-Output CP to $\overline{RC}$	3.0	7.5	3.0	11.5	3.0	11.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL4}	Propagation Delay /Data-Output P_n to Q_n	6.0	13	6.0	16	6.0	16	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH4}	Propagation Delay /Data-Output P_n to Q_n	3.0	7.0	2.0	9.0	2.0	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL5}	Propagation Delay /Data-Output $\overline{CE}$ to $\overline{RC}$	3.0	7.0	3.0	9.0	3.0	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH5}	Propagation Delay /Data-Output $\overline{CE}$ to $\overline{RC}$	3.0	7.0	3.0	9.0	3.0	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL6}	Propagation Delay /Data-Output $\overline{PL}$ to Q_n	5.5	12	5.5	14.5	5.5	14.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH6}	Propagation Delay /Data-Output $\overline{PL}$ to Q_n	5.0	11	5.0	13	5.0	13	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL7}	Propagation Delay /Data-Output $\overline{U}$/D to $\overline{RC}$	5.5	12	5.5	14	5.5	14	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH7}	Propagation Delay /Data-Output $\overline{U}$/D to $\overline{RC}$	7.0	18	7.0	22.5	7.0	22.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL8}	Propagation Delay /Data-Output $\overline{U}$/D to TC	4.0	10	4.0	12.5	4.0	12.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH8}	Propagation Delay /Data-Output $\overline{U}$/D to TC	4.0	10	4.0	13.5	4.0	13.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
f_{MAX}	Maximum Clock Frequency	100		70		70		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.

APPLICATION NOTES:

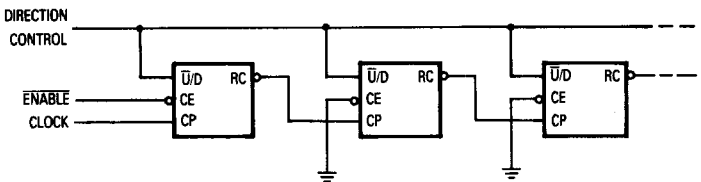

Figure A — N-Stage Counting Using Ripple Clock

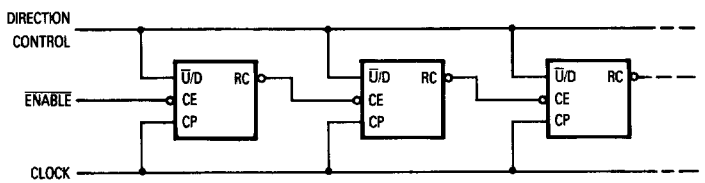

Figure B — Synchronous N-Stage Counter Using Ripple Carry/Borrow

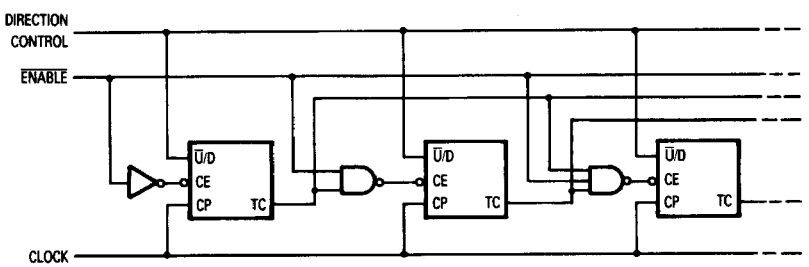

Figure C — Synchronous N-Stage Counter with Parallel Gated Carry/Borrow