# M-947 DTMF Receiver

The Teltone® M-947 combines switched-capacitor and digital techniques to decode Dual-Tone Multifrequency (DTMF) signals to four-bit binary data. No prefiltering of the DTMF signal is required. The M-947 is contained in a 22-pin DIP, operates from a single 12-volt supply, and uses an inexpensive 3.579-MHz television crystal for frequency reference.

The SIGNAL IN input to the M-947 is typically connected to a Touch-Tone® telephone, radio receiver, tape player, or other DTMF signal source. The M-947 filters out dial tone and noise, splits the signal into its high- and low-frequency components, and analyzes these components to determine the validity of the composite pair. Valid signals are decoded and stored at the DATA outputs; invalid signals are ignored. The CLEAR input resets all M-947 functions, while the BD and DV outputs provide, respectively, an early indication of signal presence and a DATA strobe.

All M-947 outputs interface with CMOS, standard voltage translation ICs, and transistor drivers. For applications incorporating multiple M-947s, the output from one oscillator can be cascaded through them all.

The M-947 is manufactured under U.S. Patent 4,145,576.

### Features

- Decodes all 16 DTMF signals
- Capacitor-coupled SIGNAL IN input
- Latching four-bit binary output
- Built-in dial tone and noise filtering
- Superior immunity to speech and noise
- Early signal presence and valid data strobe outputs
- Single 12-VDC supply
- 22-pin DIP for high-density packaging

### Telephone Switching Applications

- Central office products
- PBX and key system products
- Radio telephone products

### Access and Control Applications

- Answering and recording devices
- Monitoring and alarm devices
- Equipment control devices

### Data Entry Applications

- Computer systems
- Telephone banking, credit, bill-paying, and shopping systems

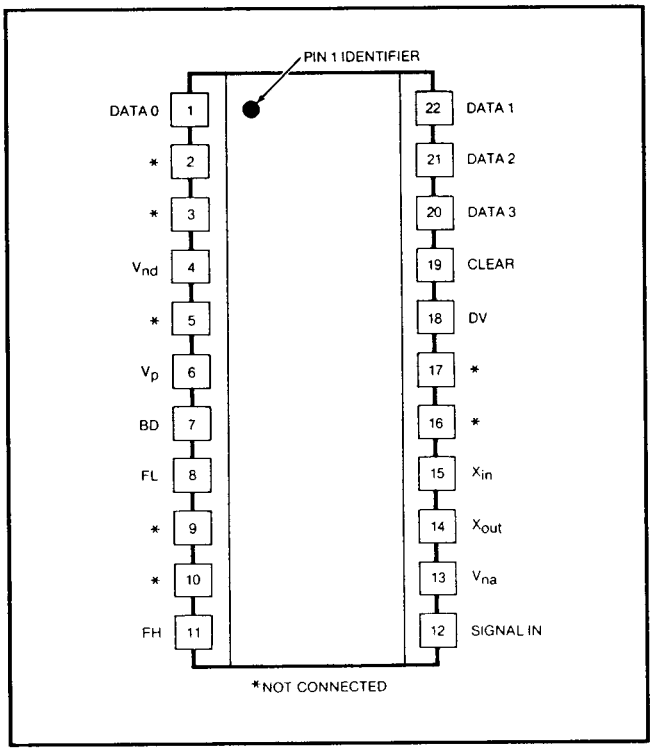



**Figure 1 Pin Diagram**

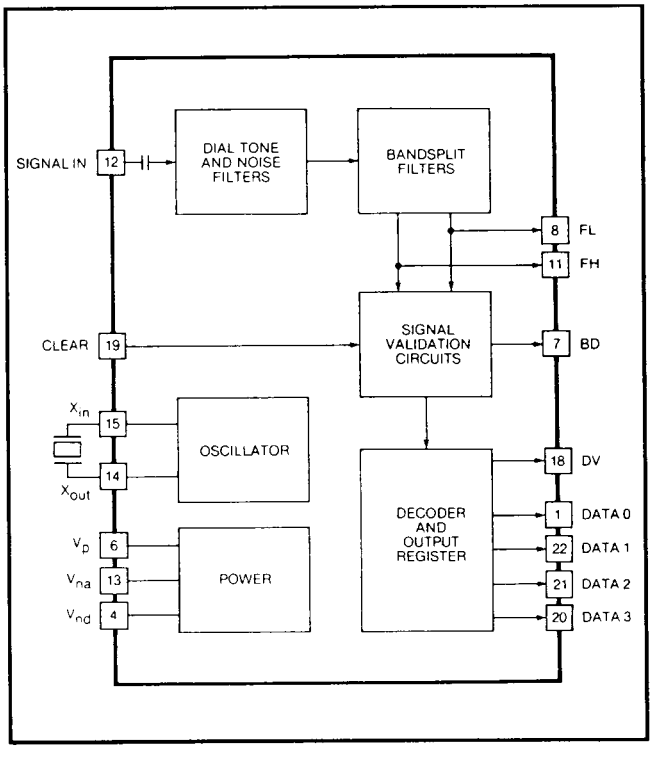


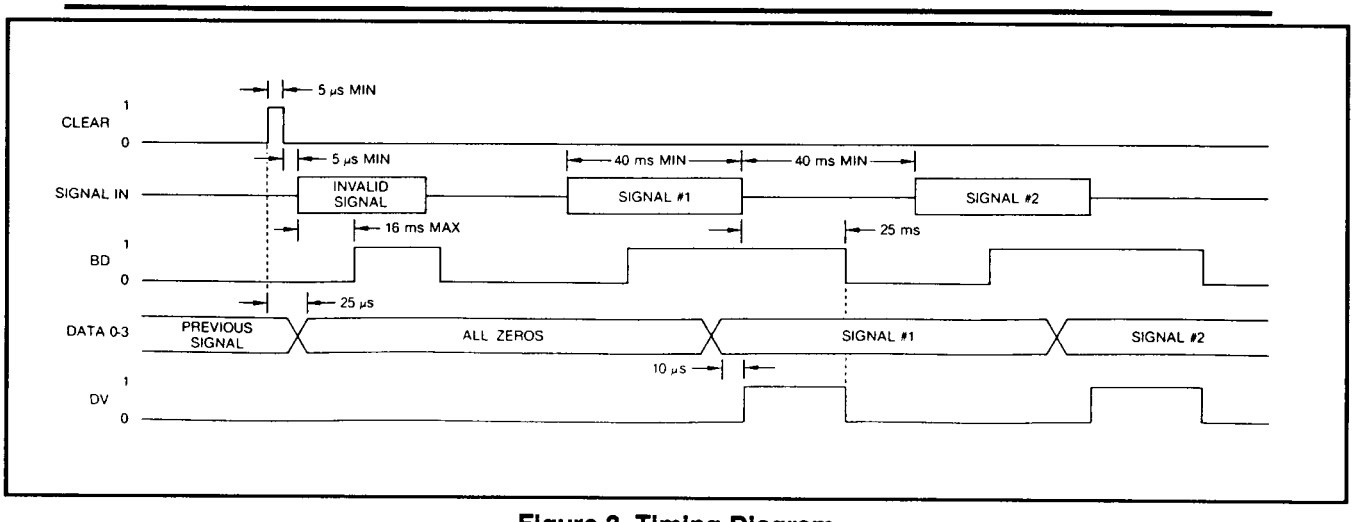

**Figure 2 Block Diagram**

## Table 1 DTMF to Binary Decoding

| SIGNAL | LOW-FREQUENCY COMPONENT | HIGH FREQUENCY COMPONENT | DATA OUTPUTS 3 2 1 0 | OUTPUT EQUIVALENT HEX | OCTAL |
|---|---|---|---|---|---|
| 1 | 697 Hz | 1209 Hz | 0 0 0 1 | 1 | 1 |
| 2 | 697 Hz | 1336 Hz | 0 0 1 0 | 2 | 2 |
| 3 | 697 Hz | 1477 Hz | 0 0 1 1 | 3 | 3 |
| 4 | 770 Hz | 1209 Hz | 0 1 0 0 | 4 | 4 |
| 5 | 770 Hz | 1336 Hz | 0 1 0 1 | 5 | 5 |
| 6 | 770 Hz | 1477 Hz | 0 1 1 0 | 6 | 6 |
| 7 | 852 Hz | 1209 Hz | 0 1 1 1 | 7 | 7 |
| 8 | 852 Hz | 1336 Hz | 1 0 0 0 | 8 | 10 |
| 9 | 852 Hz | 1477 Hz | 1 0 0 1 | 9 | 11 |
| 0 | 941 Hz | 1336 Hz | 1 0 1 0 | A | 12 |
| * | 941 Hz | 1209 Hz | 1 0 1 1 | B | 13 |
| # | 941 Hz | 1477 Hz | 1 1 0 0 | C | 14 |
| A | 697 Hz | 1633 Hz | 1 1 0 1 | D | 15 |
| B | 770 Hz | 1633 Hz | 1 1 1 0 | E | 16 |
| C | 852 Hz | 1633 Hz | 1 1 1 1 | F | 17 |
| D | 941 Hz | 1633 Hz | 0 0 0 0 | 0 | 0 |

## Table 2 Pin Functions

| Pin | Function |
|---|---|
| $V_p$ | Postive power supply connection. |
| $V_{na}$, $V_{nd}$ | Negative power supply connections. $V_{na}$ and $V_{nd}$ should be at equal potential. |
| CLEAR | Clear. As shown in Figure 3, logic 1 applied to CLEAR resets the Signal Validation Circuits (see Figure 2) and forces the DATA outputs to the "D" row (all zeros) of Table 1. Logic 0 applied to CLEAR enables the Signal Validation Circuits. |
| SIGNAL IN | DTMF input, internally AC-coupled. See Table 1 for the frequency pairs associated with each DTMF signal. |
| DATA 0-3 | Data. As shown in Figure 3, the DATA outputs change when a signal is validated and are maintained until a new signal is validated or logic 1 is applied to CLEAR. See Table 1 for the outputs associated with each DTMF signal. |
| BD | Button Down. As shown in Figure 3, BD goes to logic 1 after a signal is detected but before it has been validated as one of the frequency pairs listed in Table 2. If the signal is determined to be invalid, BD returns to logic 0 immediately. If the signal is determined to be valid, BD returns to logic 0 after the signal ends. |
| DV | Data Valid. As shown in Figure 3, DV goes to logic 1 after the DATA outputs change and returns to logic 0 after the signal ends. To read DATA during signal presence, use the leading edge of DV. To read DATA after signal presence, use the trailing edge of DV. |
| FL, FH | Normally not used. |
| $X_{in}$, $X_{out}$ | Input and output connections for a 3.579-MHz television color burst crystal. |




## Figure 3 Timing Diagram

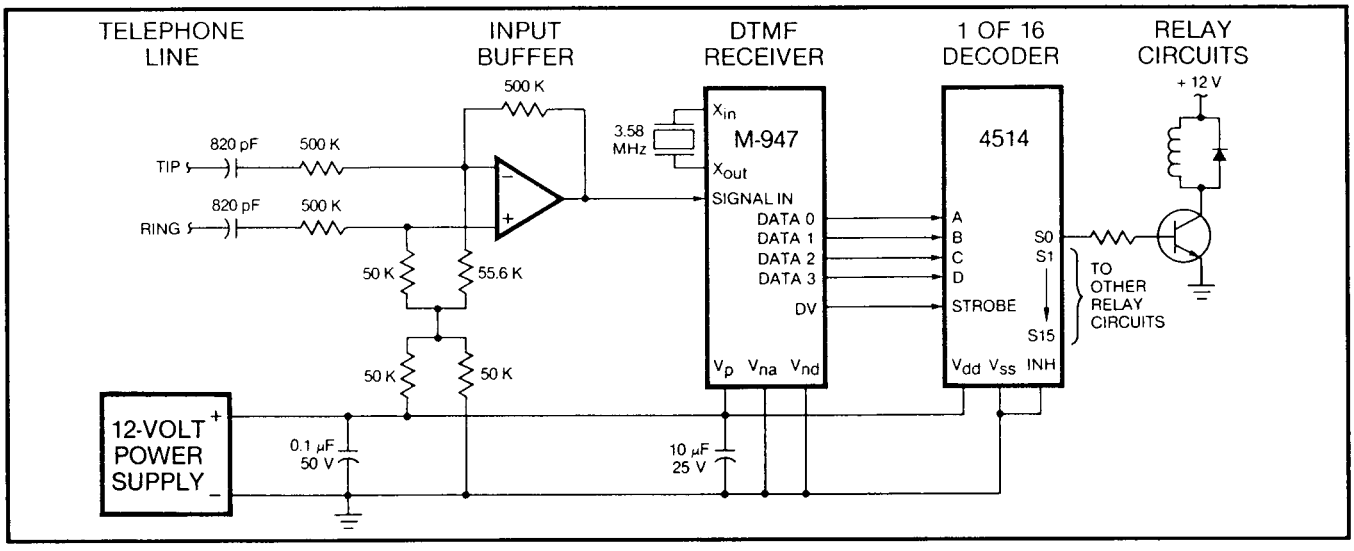
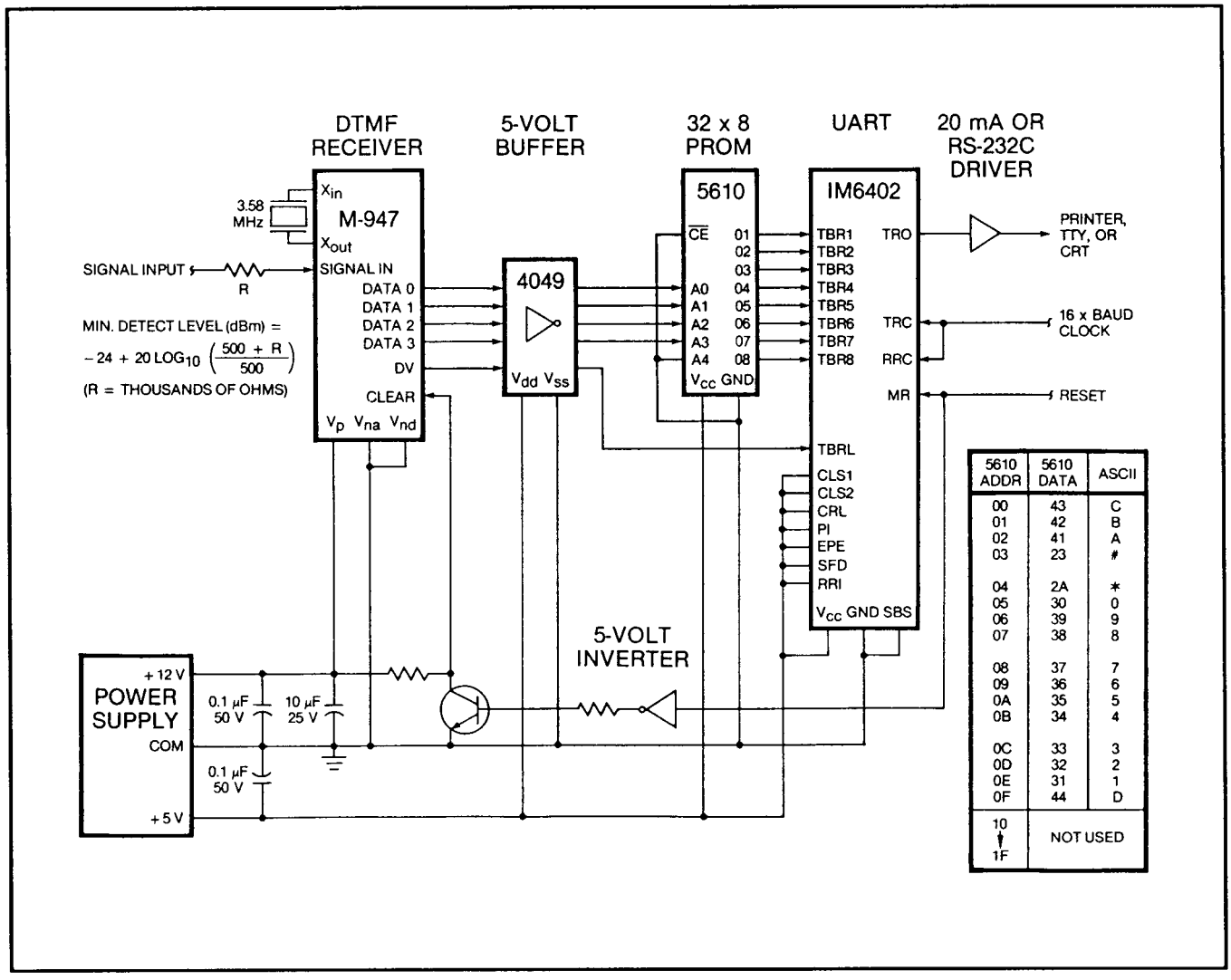



**Figure 4 Controlling Relays over a Telephone Line**




| 5610 ADDR | 5610 DATA | ASCII |
|---|---|---|
| 00 | 43 | C |
| 01 | 42 | B |
| 02 | 41 | A |
| 03 | 23 | # |
| 04 | 2A | * |
| 05 | 30 | 0 |
| 06 | 39 | 9 |
| 07 | 38 | 8 |
| 08 | 37 | 7 |
| 09 | 36 | 6 |
| 0A | 35 | 5 |
| 0B | 34 | 4 |
| 0C | 33 | 3 |
| 0D | 32 | 2 |
| 0E | 31 | 1 |
| 0F | 44 | D |
| 10 ↓ 1F | NOT USED | |

**Figure 5 DTMF to Asynchronous Serial ASCII with Adjustable Minimum Detect Level**

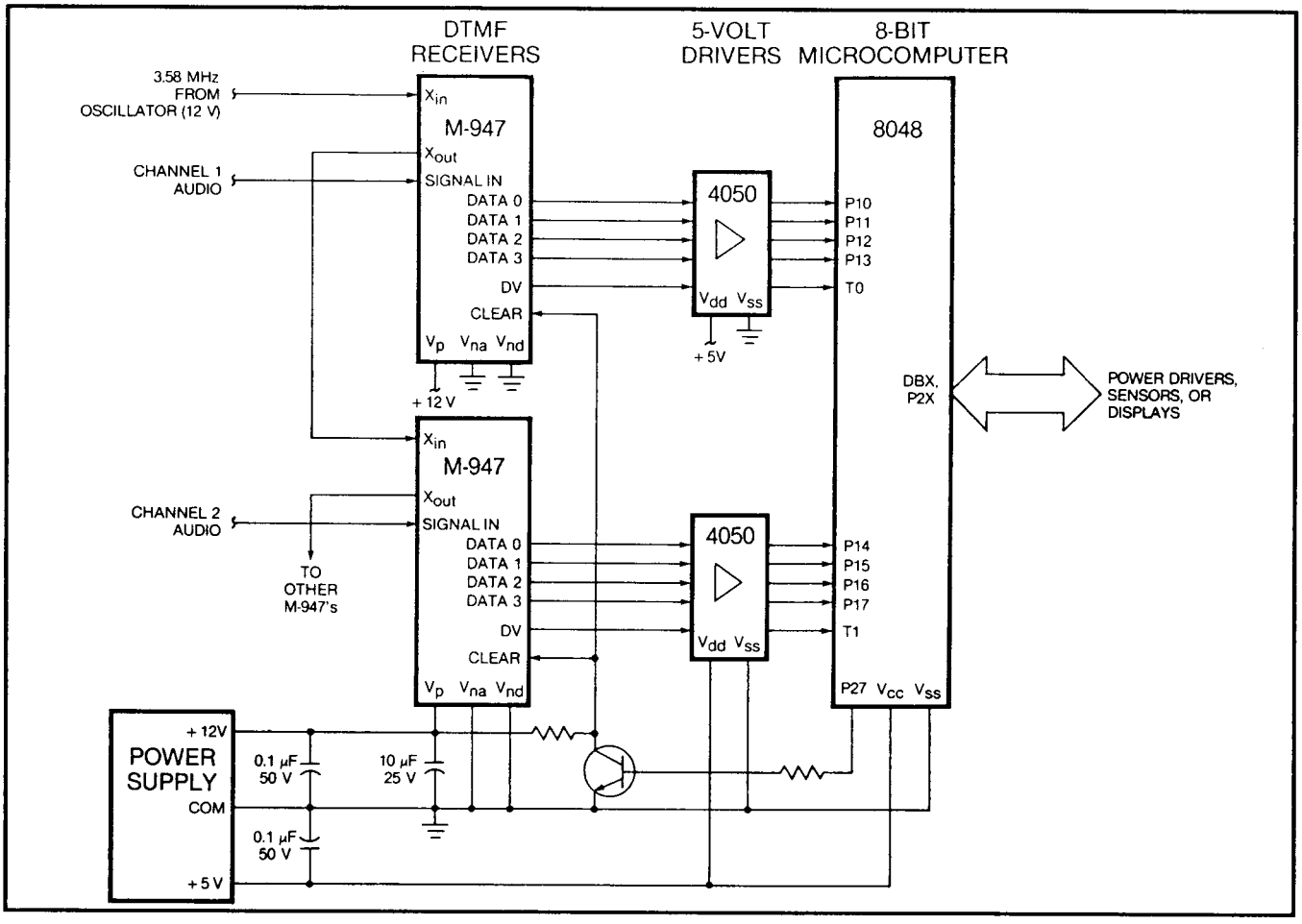



**Figure 6 Intelligent Two-Channel DTMF Receiver Using an External Clock Source**

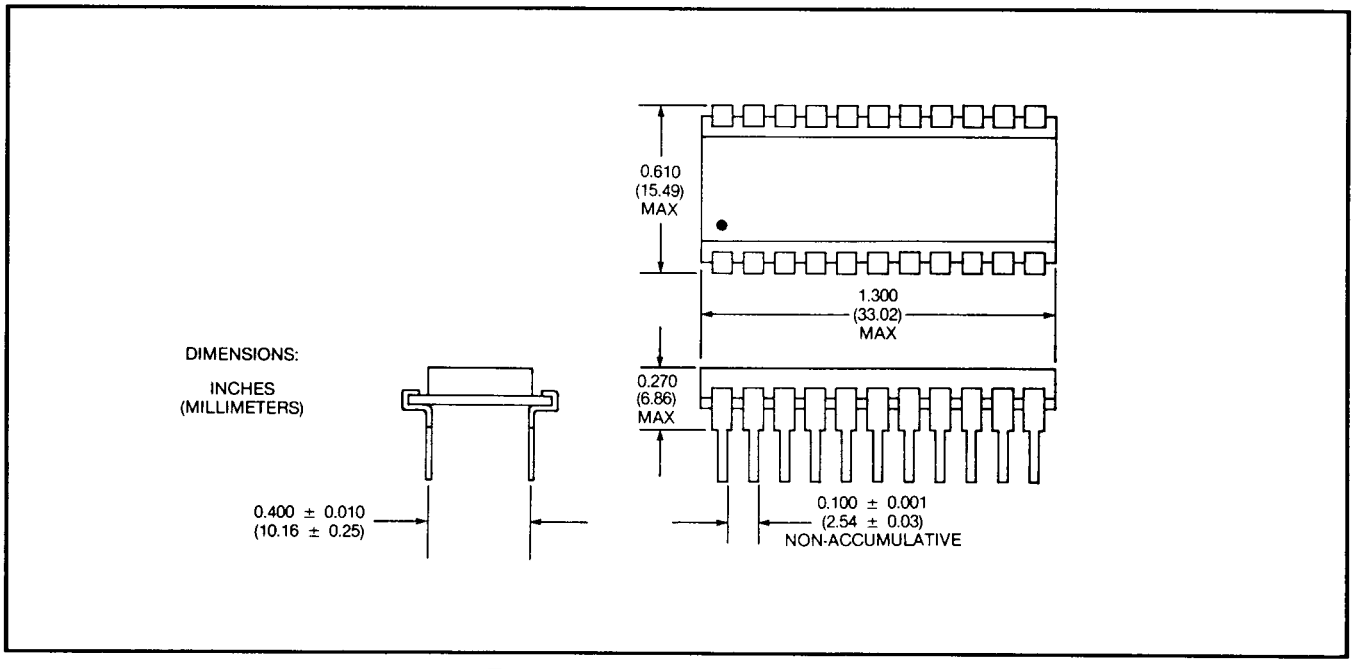



**Figure 7 Package Dimensions**

## Table 3 Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| DC Supply Voltage (Note 2) | 14.5 V |
| Voltage on SIGNAL IN | ($V_P$ + 25 V) to ($V_{na}$ − 25 V) |
| Voltage on Any Pin Except SIGNAL IN | ($V_P$ + 0.3 V) to ($V_{na}$ − 0.3 V) |
| Storage Temperature Range | −40° to 85° C |
| Operating Temperature Range | 0° to 70° C |
| Lead Soldering Temperature | 260° C for 5 seconds at 0.035 inches (0.89 mm) from package |

**Notes:**
1. Exceeding these ratings may permanently damage the M-947.
2. $V_P$ referenced to $V_{na}$. $V_{na}$ should be at equal potential to $V_{nd}$. $V_{na}$ may be at ground.

## Table 4 Specifications

| | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| **Power Requirements** | Supply Voltage | 11.0 | 13.5 | Vdc | 1 |
| | Supply Voltage Ripple | — | 30 | mVpp | 2 |
| | Supply Current | — | 85 | mA | |
| **CLEAR Input Requirements** | Logic 0 Voltage | −0.3 | 2.0 | V | 3 |
| | Logic 1 Voltage | 10.0 | 12.3 | V | 3 |
| | Input Current | −50 | 50 | μA | |
| **SIGNAL IN Input Requirements** | Signal Level | −24 | +6 | dBm | 4, 5, 6 |
| | Signal Duration | 40 | — | ms | |
| | Interval Between Signals | 40 | — | ms | |
| | Signal Cycle Time | 85 | — | ms | |
| | Signal Present Without Detection | — | 20 | ms | |
| | Interruption of Signal Without Redetection | — | 20 | ms | |
| | Signal Frequency Deviation | −(1.5% + 2) | +(1.5% +2) | Hz | |
| | Twist | −10 | +10 | dB | 7 |
| | Signal-to-Noise Ratio | 18 | — | dB | 6, 8 |
| | Noise Level | — | −37 | dBm | 5, 6 |
| | Dial Tone Level (f≤500 Hz) | — | −5 | dBm | 4, 5 |
| | Precise Dial Tone Level | — | 0 | dBm | 4, 5, 9 |
| **DATA, BD, and DV Output Characteristics** | Logic 0 Voltage | — | 2 | V | 3 |
| | Logic 1 Voltage | 10 | — | V | 3 |
| | Output Current | −0.1 | 0.1 | mA | |
| **Miscellaneous Characteristics** | Power Dissipation | — | 1.3 | W | |
| | CLEAR Input Capacitance | — | 15 | pF | |
| | SIGNAL IN Input Impedance (1 kHz) | 450k | — | ohms | |

**Notes:**

1. $V_P$ referenced to $V_{na}$. $V_{na}$ may be at ground.
2. A bypass capacitor may be necessary.
3. Logic levels are shown for a supply voltage ($V_P$ − $V_{na}$) of 12 V, and are referenced to $V_{na}$.
4. Per tone.
5. The unit "dBm" refers to decibels above or below a reference power of one milliwatt into a 600-ohm load. (For example, −24 dBm equals 49 mV.)
6. Measurement made with a 12 ±0.1 V power supply. Levels may change ±1 dB over the supply range of 11 to 13.5 V.
7. Twist is defined as the ratio of the level of the high-frequency DTMF component to the level of the low-frequency DTMF component.
8. With the signal level −19 dBm per component, the signal 50 ms on and 50 ms off, no twist or frequency deviation, all 16 signals received randomly, 0 through 3 kHz flat Gaussian noise, and an error rate of less than one in 10,000. This is essentially the test method of EIA, AT&T, and USITA.
9. Precise Dial Tone is 350 Hz and 440 Hz.