

DATA SHEET (Preliminary)

NEC
ELECTRON DEVICE

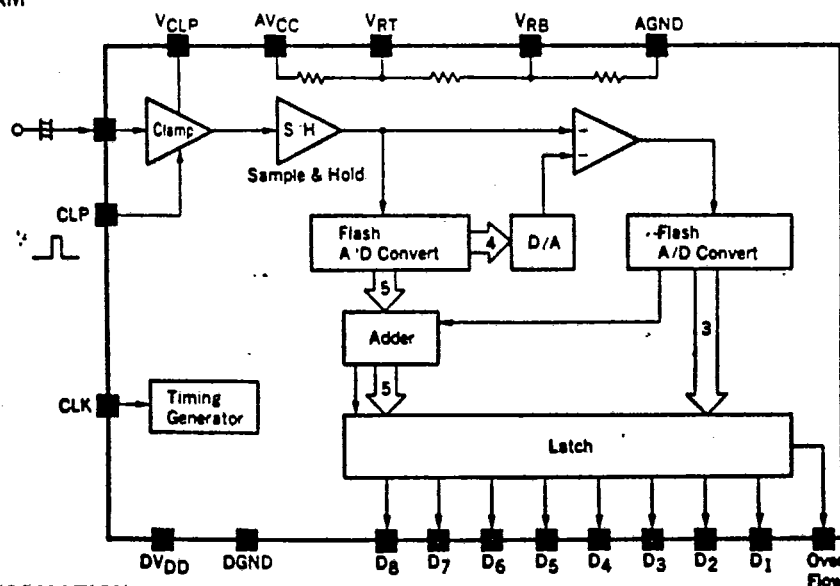
BIPOLAR ANALOG INTEGRATED CIRCUIT
 μ PC659
8 BIT A/D CONVERTER FOR VIDEO PROCESSING
WITH REFERENCE GENERATOR AND CLAMP CIRCUIT

The μ PC659 is a 8 bit A/D converter for video signal processing. The high speed and high quality Bipolar processing technology have enabled fast conversion rate and high resolution to be achieved. Conversion Rate is up to 20 MHz and Linearity Error within ± 0.5 LSB while operating at low power consumption. Also, this IC include clamp circuit and reference voltage generator, which enables simple external circuits to be constructed.

FEATURES

- Resolution: 8 bits
- Conversion Rate: 20 MspS MAX.
- Linearity: ± 0.5 LSB MAX.
- Power Supply Voltage: +5 V single
- Analog Input Voltage: 1.0 V_{p-p} TYP.
- Include Clamp Circuit (Clamp voltage and clamp pulse must be supplied.)
- Include Reference Voltage Generator: $V_{RT} = 3.3$ V, $V_{RB} = 2.3$ V
- Low Power Consumption: 395 mW TYP.

BLOCK DIAGRAM



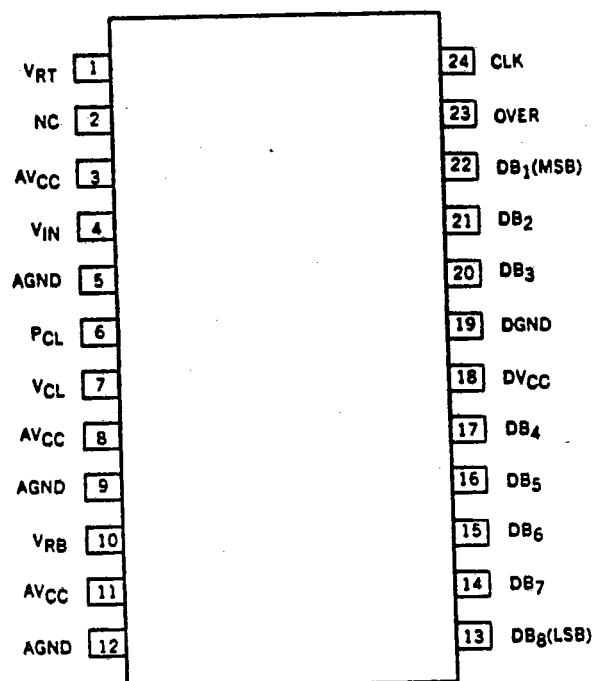
ORDERING INFORMATION

ORDER NAME	PACKAGE
μ PC659G	24 Pin Plastic SOP (300 mil)

μ PC659

NEC ELECTRON DEVICE

CONNECTION DIAGRAM (Top View)



No.	Symbol	Pin Name	No.	Symbol	Pin Name
1	VRT	Ref. Voltage (High Voltage)	13	DB ₈	Digital Data Output (LSB)
2	NC	No Connection	14	DB ₇	Digital Data Output (7th)
3	AVCC	Power Supply for Analog Circuit	15	DB ₆	Digital Data Output (6th)
4	VIN	Analog Signal Input Terminal	16	DB ₅	Digital Data Output (5th)
5	AGND	Ground for Analog Circuit	17	DB ₄	Digital Data Output (4th)
6	PCL	Clamp Pulse Input Terminal	18	DVCC	Power Supply for Digital Circuit
7	VCL	Clamp Voltage Input Terminal	19	DGND	Ground for Digital Circuit
8	AVCC	Power Supply for Analog Circuit	20	DB ₃	Digital Data Output (3rd)
9	AGND	Ground for Analog Circuit	21	DB ₂	Digital Data Output (2nd)
10	VRB	Ref. Voltage (Low Voltage)	22	DB ₁	Digital Data Output (MSB)
11	AVCC	Power Supply for Analog Circuit	23	OVER	Digital Over Range Output
12	AGND	Ground for Analog Circuit	24	CLK	Sampling Clock Input Terminal

NEC ELECTRON DEVICE

 μ PC659ABSOLUTE MAXIMUM RATINGS ($T_s = 25^\circ\text{C}$)

Supply Voltage	A, DV_{CC}	-0.3 to +6.0	V
Digital Input Voltage	V_{IND}	-0.3 to $DV_{CC}+0.3$	V
Analog Input Voltage	V_{INA}	-0.3 to $AV_{CC}+0.3$	V
Reference Input Voltage	V_{RT}, V_{RB}	-0.3 to $AV_{CC}+0.3$	V
Clamp Voltage	V_{CL}	-0.3 to $AV_{CC}+0.3$	V
Clamp Pulse Input Voltage	V_{PCL}	-0.3 to $AV_{CC}+0.3$	V
Operating Temperature	T_{op1}	-20 to +75 (SHD) -20 to +65 (SOP)	$^\circ\text{C}$
Storage Temperature	T_{stg}	-40 to +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($T_s = -20$ to $+75^\circ\text{C}$ (SHD), $T_s = -20$ to $+65^\circ\text{C}$ (SOP))

TITLE	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	A, DV_{CC}	4.7	5.0	5.3	V	AGND = DGND = 0
Analog Input Voltage	V_{INA}	$V_{RB}-0.4$		$V_{RT}+0.4$	V	
Clamp Input Voltage	V_{CL}	$V_{RB}-0.4$		$V_{RT}+0.4$	V	
Sampling Clock	f_{SAMP}	1.0		20	MHz	
Sampling Clock Low Pulse Width	t_{PWL}	25			ns	
Sampling Clock High Pulse Width	t_{PWH}	25			ns	
Clock Input High Level Voltage	V_{CKH}	2.0			V	
Clock Input Low Level Voltage	V_{CKL}			0.9	V	
Clamp Pulse Width	t_{PWCL}	1.0			μs	
Clamp Pulse High Level Voltage	V_{CPH}	2.0			V	
Clamp Pulse Low Level Voltage	V_{CPL}			0.9	V	
Clamp Capacitance	C_{CP}		10		μF	
Maximum Analog Input Frequency	f_{AIN}		8		MHz	

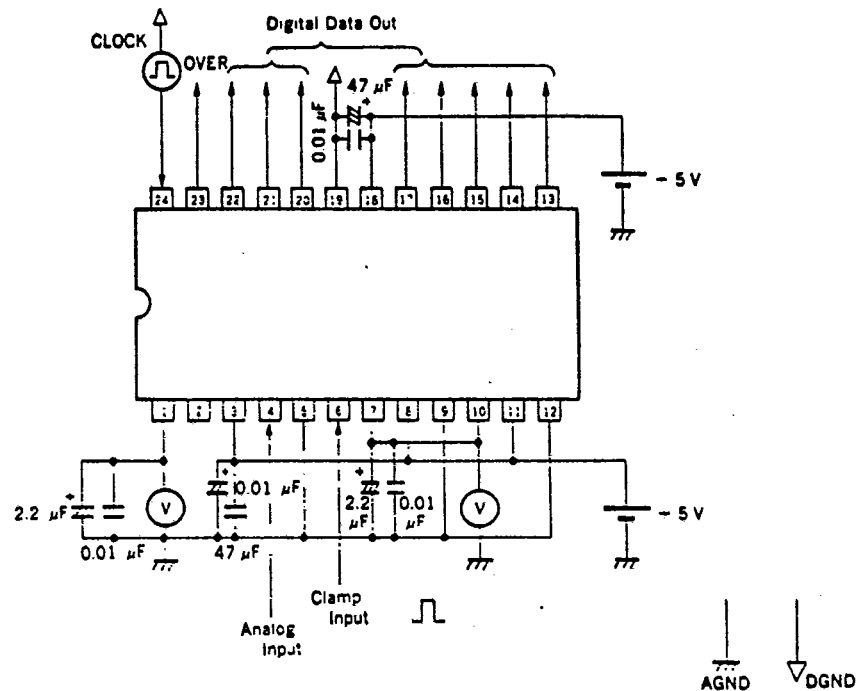
μ PC659

NEC ELECTRON DEVICE

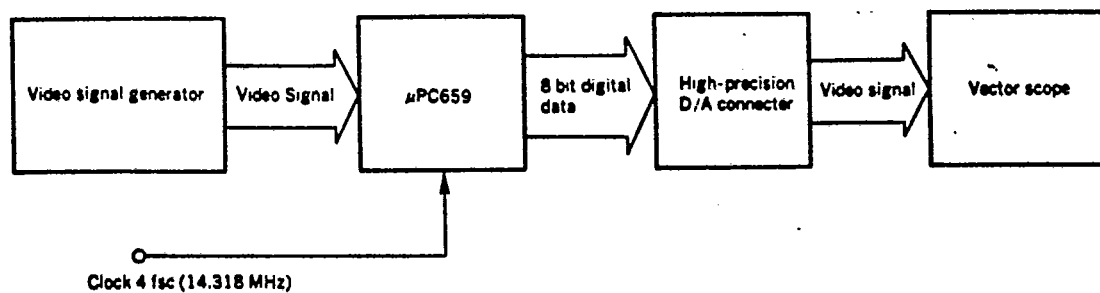
ELECTRICAL CHARACTERISTICS ($T_a = -20$ to $+75$ °C for SHD, $T_a = -20$ to $+65$ °C for SOP)
 $AV_{CC} = DV_{CC} = 5.0 \pm 0.3$ V

TITLE	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Current	I_{CC}	50	79	110	mA	$V_{CC} = 5.0$ V, $T_a = 25$ °C
Resolution	RES		8		bit	
Non-linearity	NL			± 1.5	LSB	$V_{CC} = 0.5$ V, $T_a = 25$ °C $V_{IN} = 1.0$ Vp.p
Differential Non-linearity	DNL			± 0.5	LSB	$V_{CC} = 0.5$ V, $T_a = 25$ °C $V_{IN} = 1.0$ Vp.p
Differential Gain	DG		1.5	3.0	%	$f_{SAMP} = 14.318$ MHz NTSC Lamp wave (40 IRE)
Differential Phase	DP		0.8	3.0	deg	$f_{SAMP} = 14.318$ MHz NTSC Lamp wave (40 IRE)
Digital Data Output Delay Time	t_D		12		ns	Delay time from falling edge of sampling clock.
Digital Output Low Voltage	V_{OL}			0.4	V	$I_{OL} = 1.6$ mA D ₁ to D ₈ , OVER
Digital Output High Voltage	V_{OH}	2.7			V	$I_{OH} = -400$ μ A D ₁ to D ₈ , OVER
Digital Input Low Input Current	I_{INDL}			-200	μ A	$V_{IN} = 0.8$ V
Digital Input High Input Current	I_{INDH}			10	μ A	$V_{IN} = 2.0$ V
Analog Input Current	I_{INA}		10	35	μ A	Measure input current from analog input terminal.
Reference Voltage (Low)	V_{RB}	2.1	2.3	2.5	V	$V_{CC} = 5.0$ V
Reference Voltage (High)	V_{RT}	3.1	3.3	3.5	V	$V_{CC} = 5.0$ V
Analog Input Equivalent Capacitance	C_{IN}		3.0		pF	$V_{IN} = V_{RB}$
Clock Input Equivalent Capacitance	C_{CLK}		2.0		pF	

TEST CIRCUIT



DG, DP TEST BLOCK

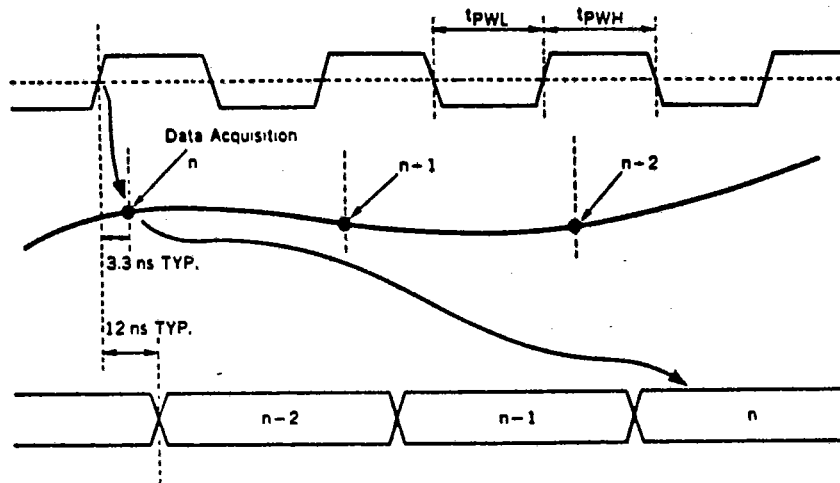


The video signal from the video signal generator is 40 IRE Ramp signal.

μ PC659

NEC ELECTRON DEVICE

TIMING CHART

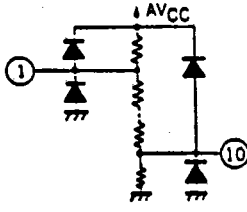
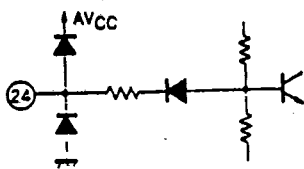
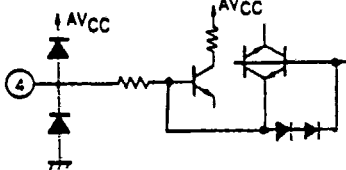
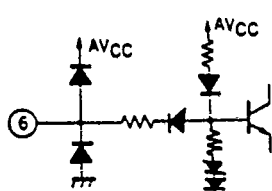
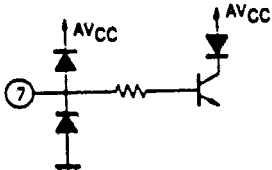
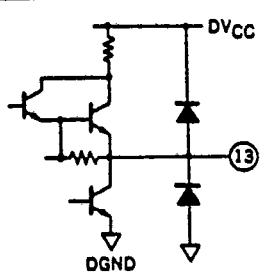


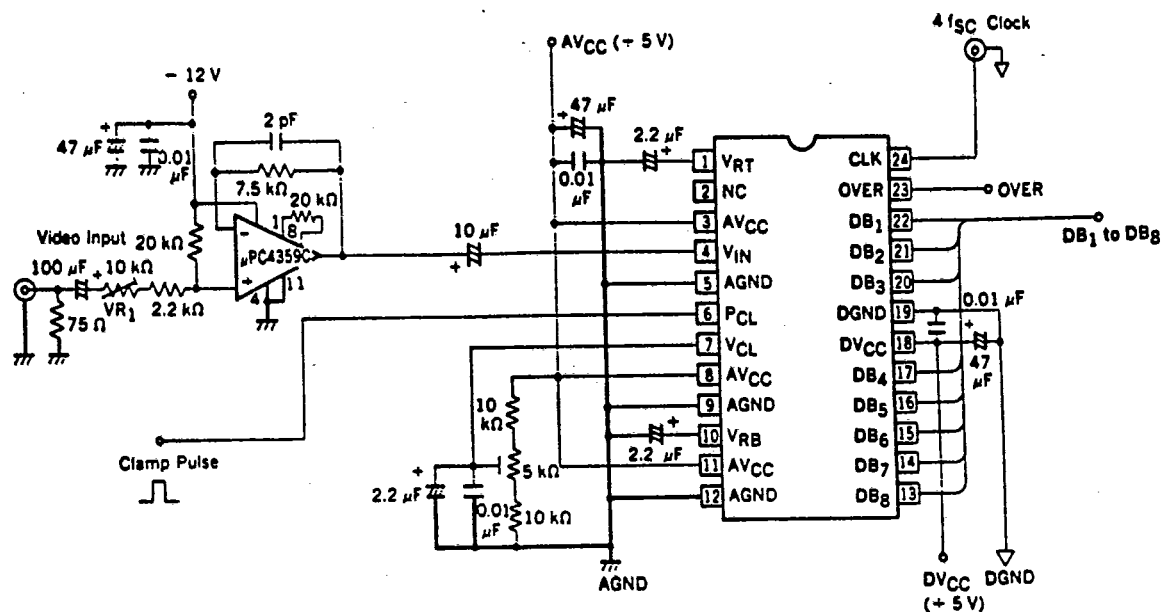
Analog signal is sampled with sampling clock and after the acquisition time (3.3 ns TYP.) started to be sampled. And converted data will be out after 2 sampling clock synchronized with the rise edge of sampling clock. Delay time from the rise edge of sampling clock is typically 12 ns.

NEC ELECTRON DEVICE

 μ PC659

EQUIVALENT CIRCUIT AROUND TERMINAL

Pin No.	Equivalent Circuit	Function
1, 10		1: Reference voltage (Top) V_{RT} 10: Reference voltage (Bottom) V_{RB}
5, 9, 12		Ground for Analog Circuit.
24		Sampling Clock input terminal. Analog data acquisition and digital data out are synchronized with the rise edge of this clock.
3, 8, 11		Power supply for analog circuit.
4		Analog signal input terminal. Input analog signal from this terminal. The clamp function also will be worked on this terminal. So it's necessary to connect capacitance and low impedance source.
6		Clamp pulse input terminal. Analog signal input from analog input terminal is clamped to the voltage; V_{CL} according to the high level term of this pulse.
7		Clamp bias input terminal. Analog input signal is clamped nearly to this input voltage; V_{CL} according to the clamp pulse; P_{CL} high level period.
13 to 17 21 to 22 23		Digital data output terminal. 13: Out of LSB data 14: Out of 7th data 15: Out of 6th data 16: Out of 5th data 17: Out of 4th data 20: Out of 3rd data 21: Out of 2nd data 22: Out of MSB data 23: Out of Over Flow
18		Power supply for digital.
19		Ground for digital.

μPC659**NEC** ELECTRON DEVICE**APPLICATION**

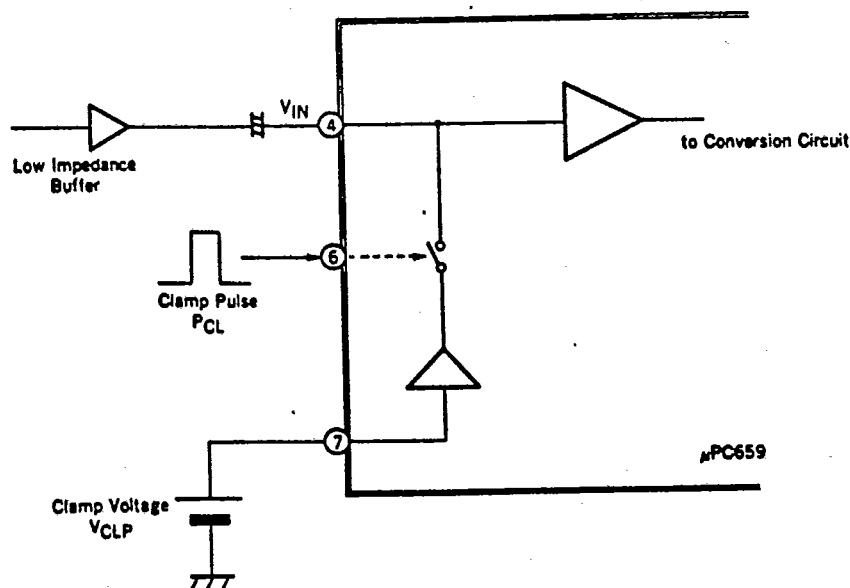
AGND and DGND
must be connect at
one point

ATTENTION FOR APPLICATION

- Analog input terminal

Please connect low impedance signal source to analog input terminal.

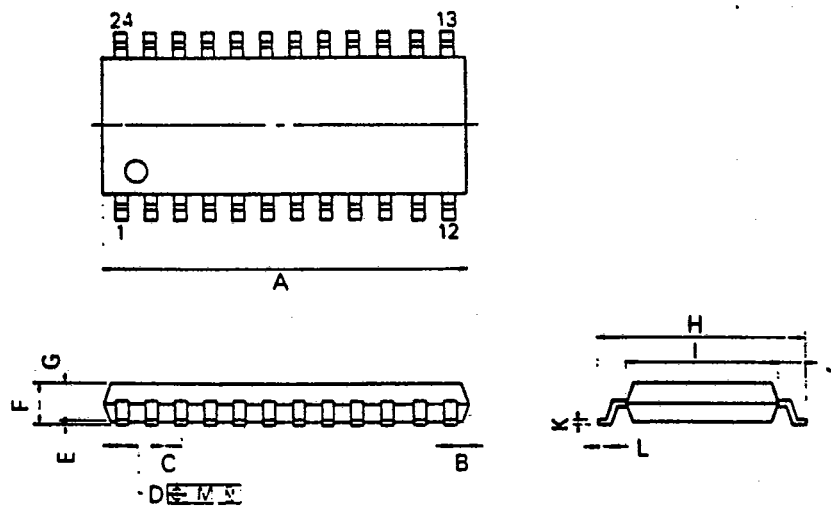
And must be AC coupled. Clamp circuit is appeared by following rough block diagram.



μ PC659

NEC ELECTRON DEVICE

24 PIN PLASTIC SOP (300 mil)



P24GM-50-300B

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.08}$	$0.016^{+0.004}_{-0.003}$
E	$0.1^{+0.1}_{-0.0}$	$0.004^{+0.004}_{-0.000}$
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	$7.7^{+0.3}_{-0.2}$	$0.303^{+0.012}_{-0.010}$
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.08}$	$0.008^{+0.004}_{-0.003}$
L	$0.6^{+0.2}_{-0.1}$	$0.024^{+0.008}_{-0.006}$
M	0.12	0.005