

**LC7527E****Graphic Equalizer System****Overview**

The LC7527E is a microprocessor controllable seven-band graphic equalizer LSI that does not require the use of external semiconductor inductors (simulated inductors).

**Functions**

- Left and right channel seven-band graphic equalizers
- Each band operates in  $\pm 2$  dB steps.
- Each band has a maximum boost of +12 dB and a maximum cut of -12 dB for a total of 13 settings.
- Independent left and right channel operation
- Serial data input supports CCB format communications with the system controller.
- CMOS LSI with a 12 V breakdown voltage

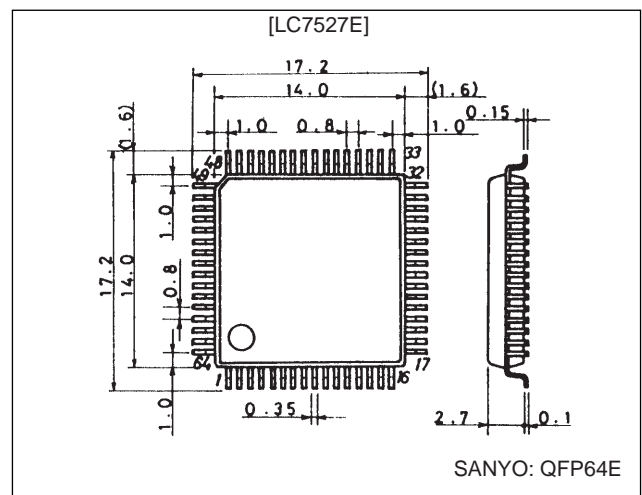
**Features**

- This LSI, in conjunction with a control microprocessor, can implement in two chips, an electronic graphic equalizer with the following features.
  - One touch gain control for each band
  - One touch memory setting recall allows users to select desired frequency characteristics for each track.
  - Since the LC7527E includes band filter amplifiers on chip, capacitors are the only external components required in application systems.
  - Minimal switching noise due to the use of a Silicon gate CMOS process.

- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

**Package Dimensions**

unit: mm

**3159-QFP64E**

## LC7527E

### Specifications

**Absolute Maximum Ratings at  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD-V_{EE\ max}}$	$AV_{DD}$ , $AV_{EE}$ , $DV_{DD}$ , $DV_{EE}^*$	12	V
Maximum input voltage	$V_{IN\ max1}$	CL, DI, CE	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
	$V_{IN\ max2}$	LIN1, LIN2, RIN1, RIN2	$V_{EE} - 0.3$ to $V_{DD} + 0.3$	V
	$V_{IN\ max3}$	S1	$V_{EE} - 0.3$ to $V_{DD} + 0.3$	V
Allowable power dissipation	$P_d\ max$	$T_a \leq 85^\circ\text{C}$	280	mW
Operating temperature	$T_{opr}$		-40 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-50 to +125	$^\circ\text{C}$

Note: \*  $-6\text{ V} \leq V_{EE} \leq V_{SS} \leq V_{DD}$

**Allowable Operating Ranges at  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$**

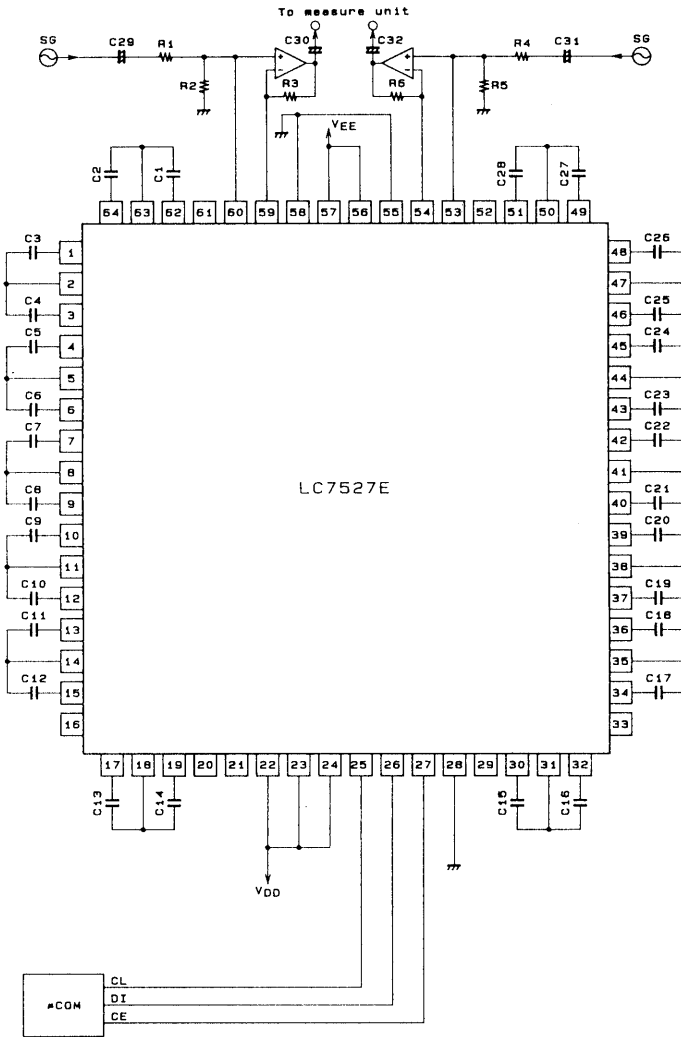
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}$	$AV_{DD}$ , $DV_{DD}$		5		V
	$V_{EE}$	$AV_{EE}$ , $DV_{EE}$		-5		V
	$V_{DD-V_{EE}}$	$AV_{DD}$ , $AV_{EE}$ , $DV_{DD}$ , $DV_{EE}$	8.0		11.0	V
Input high level voltage	$V_{IH}$	CL, DI, CE	3.0		$V_{DD}$	V
Input low level voltage	$V_{IL}$	CL, DI, CE	$V_{SS}$		1.0	V
Input amplitude voltage	$V_{IN1}$	LIN1, LIN2, RIN1, RIN2	$V_{EE}$		$V_{DD}$	Vp-p
	$V_{IN2}$	S1	$V_{EE}$		$V_{DD}$	V
Clock pulse width	$t_{\phi W}$	CL	1			$\mu\text{s}$
Setup time	$t_{setup}$	CL, DI, CE	1			$\mu\text{s}$
Hold time	$t_{HOLD}$	CL, DI, CE	1			$\mu\text{s}$
Operating frequency	fopg	CL			500	kHz

**Electrical Characteristics at  $T_a = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$ ,  $V_{EE} = -5\text{ V}$ ,  $V_{SS} = 0\text{ V}$**

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Total harmonic distortion	THD (1)	$V_{OUT} = 1\text{ V}_{rms}$ , FLAT, $f = 20\text{ kHz}$		0.01	0.05	%
	THD (2)	$V_{OUT} = 1\text{ V}_{rms}$ , FLAT, $f = 1\text{ kHz}$		0.001	0.005	%
	THD (3)	$V_{OUT} = 300\text{ mV}_{rms}$ , FLAT, $f = 20\text{ kHz}$ with all bands at full boost		0.042	0.2	%
	THD (4)	$V_{OUT} = 300\text{ mV}_{rms}$ , FLAT, $f = 1\text{ kHz}$ with all bands at full boost		0.045	0.2	%
Crosstalk	CT	$V_{OUT} = 1\text{ V}_{rms}$ , $f = 20\text{ kHz}$ , FLAT, $R_g = 1\text{ k}\Omega$		58		dB
Setting error	$\Delta B$	with other bands flat	-2		+2	dB
Current drain	$I_{DD}$	$V_{DD-V_{EE}} = 11\text{ V}$			30	mA
Analog switch off leakage current	$I_{OFF}$	LIN1, LIN2, RIN1, RIN2			10	$\mu\text{A}$

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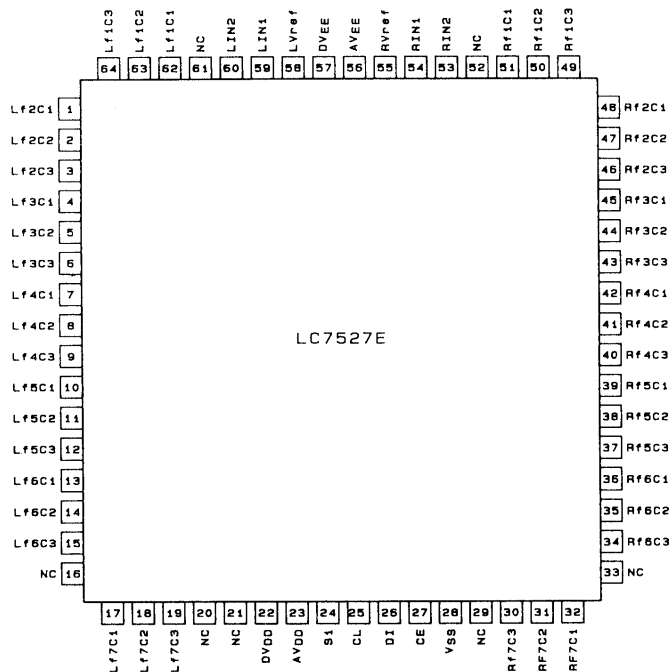
## Electrical Characteristics Test Circuit



No.	Unit (F)
C1, C28	0.94 $\mu$
C2, C27	0.034 $\mu$
C3, C26	0.377 $\mu$
C4, C25	0.0133 $\mu$
C5, C24	0.1506 $\mu$
C6, C23	5390 p
C7, C22	0.057 $\mu$
C8, C21	2156 p
C9, C20	0.0242 $\mu$
C10, C19	867 p
C11, C18	9200 p
C12, C17	3322 p
C13, C16	3770 p
C14, C15	1330 p

No.	Unit (F)
C29, C30, C31, C32	10 $\mu$
No.	Unit ( $\Omega$ )
R1, R3, R4, R6	7.5 k
R2, R5	1 M

## Pin Assignment



Top view

AD1252

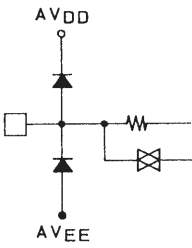
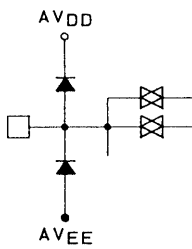
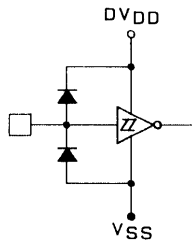
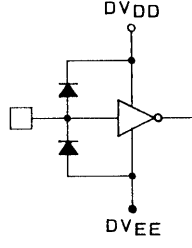
Pin Functions

Pin	Pin No.	Circuit type	Function
Lf1C1 Lf1C2 Lf1C3	62 63 64		Left channel f1 band control block External capacitor connections
Rf1C1 Rf1C2 Rf1C3	51 50 49		Right channel f1 band control block External capacitor connections
Lf2C1 Lf2C2 Lf2C3	1 2 3		Left channel f2 band control block External capacitor connections
Rf2C1 Rf2C2 Rf2C3	48 47 46		Right channel f2 band control block External capacitor connections
Lf3C1 Lf3C2 Lf3C3	4 5 6		Left channel f3 band control block External capacitor connections
Rf3C1 Rf3C2 Rf3C3	45 44 43		Right channel f3 band control block External capacitor connections
Lf4C1 Lf4C2 Lf4C3	7 8 9		Left channel f4 band control block External capacitor connections
Rf4C1 Rf4C2 Rf4C3	42 41 40		Right channel f4 band control block External capacitor connections
Lf5C1 Lf5C2 Lf5C3	10 11 12		Left channel f5 band control block External capacitor connections
Rf5C1 Rf5C2 Rf5C3	39 38 37		Right channel f5 band control block External capacitor connections
Lf6C1 Lf6C2 Lf6C3	13 14 15		Left channel f6 band control block External capacitor connections
Rf6C1 Rf6C2 Rf6C3	36 35 34		Right channel f6 band control block External capacitor connections
Lf7C1 Lf7C2 Lf7C3	17 18 19		Left channel f7 band control block External capacitor connections
Rf7C1 Rf7C2 Rf7C3	32 31 30		Right channel f7 band control block External capacitor connections
AV <sub>DD</sub> AV <sub>EE</sub> DV <sub>DD</sub> DV <sub>EE</sub> V <sub>SS</sub>	23 56 22 57 28		Power supply: +5 V typ. Audio signal power supply Power supply: -5 V typ. Audio signal power supply Power supply: +5 V typ. Logic signal power supply Power supply: -5 V typ. Logic signal power supply Power supply: 0 V AV <sub>DD</sub> must be equal to DV <sub>DD</sub> , and AV <sub>EE</sub> must be equal to DV <sub>EE</sub> .

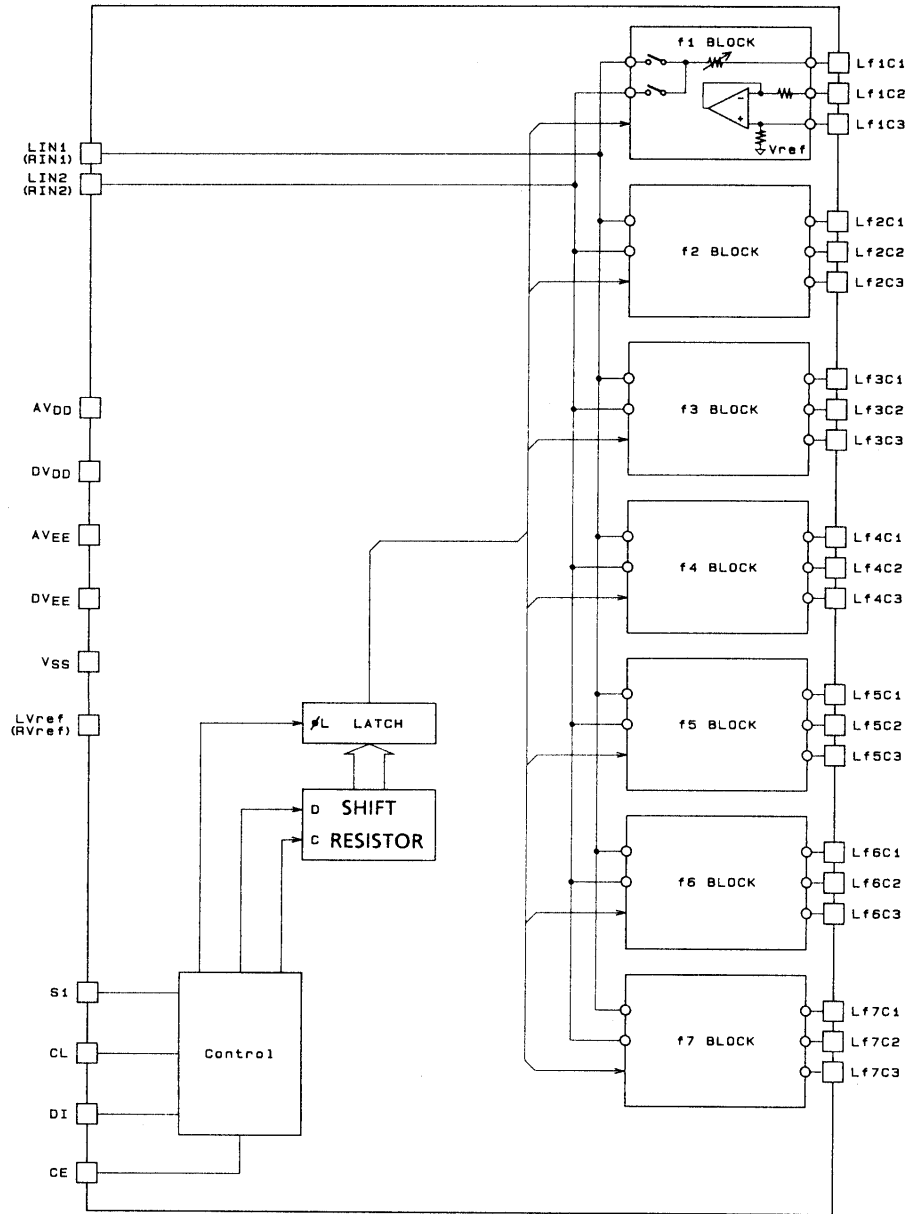
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## LC7527E

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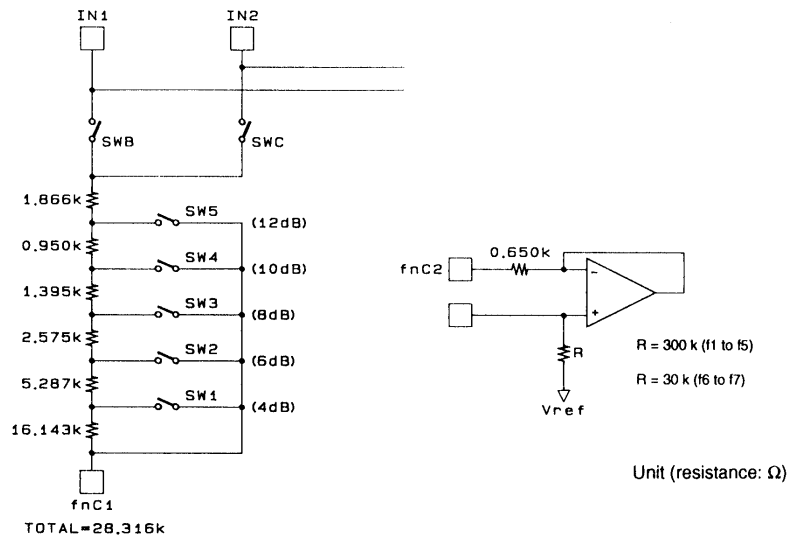
Pin	Pin No.	Circuit type	Function
LVref RVref	58 55	 <p style="text-align: right;"><b>A01922</b></p>	<p>Power supply: Analog ground</p> <p>The impedance of the pattern connected to these pins should be kept as low as possible.</p> <p>LVref and RVref are not connected to the V<sub>SS</sub> pin.</p>
LIN1 LIN2	59 60	 <p style="text-align: right;"><b>A01923</b></p>	<p>Left channel audio signal input</p> <p>IN1 is normally connected to an operational amplifier inverting input.</p> <p>IN2 is normally connected to an operational amplifier non-inverting input.</p>
RIN1 RIN2	54 53		<p>Right channel audio signal input</p> <p>IN1 is normally connected to an operational amplifier inverting input.</p> <p>IN2 is normally connected to an operational amplifier non-inverting input.</p>
CE	27	 <p style="text-align: right;"><b>A01924</b></p>	<p>Chip enable input. Internal data is latched when this pin goes from high to low and the analog switches operate. Data transfers are enabled when this pin is high.</p>
CL	25		<p>Clock input. Schmitt inverter input circuit</p>
DI	26		<p>Data input. Schmitt inverter input circuit</p>
S1	24	 <p style="text-align: right;"><b>A01925</b></p>	<p>Dual chip system chip select input. By connecting S1 (this pin) to either V<sub>DD</sub> or V<sub>EE</sub>, data input is enabled when the address matches the corresponding address listed below.</p> <p>S1 = V<sub>DD</sub> → Address: 8C</p> <p>S1 = V<sub>EE</sub> → Address: 8D</p>
NC NC NC NC NC NC NC	16 20 21 29 33 52 61		<p>No connection. Do not connect signals to these pins.</p>

Equivalent Circuit



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Internal Equivalent Circuit (for a single band)

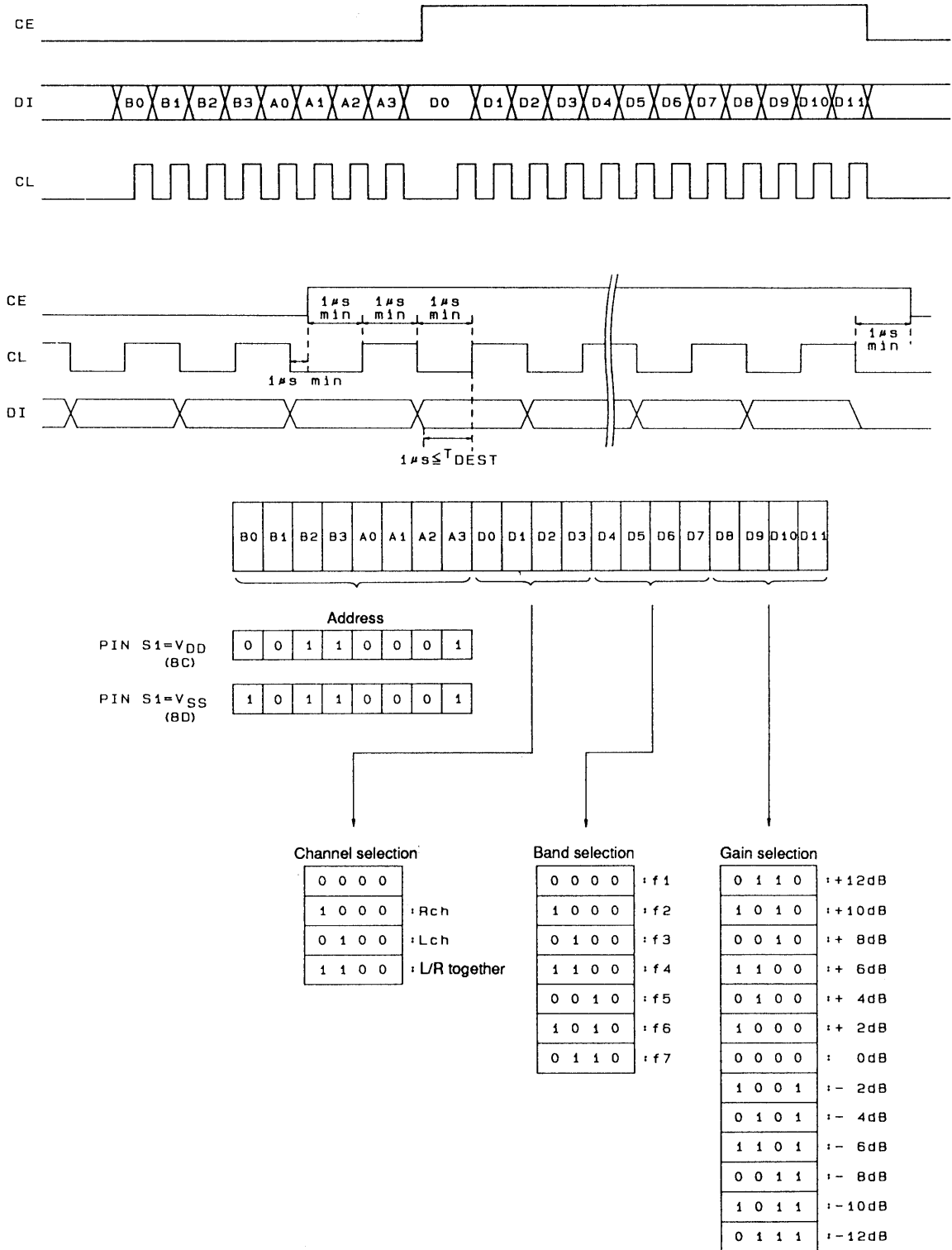


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# LC7527E

## Data Input

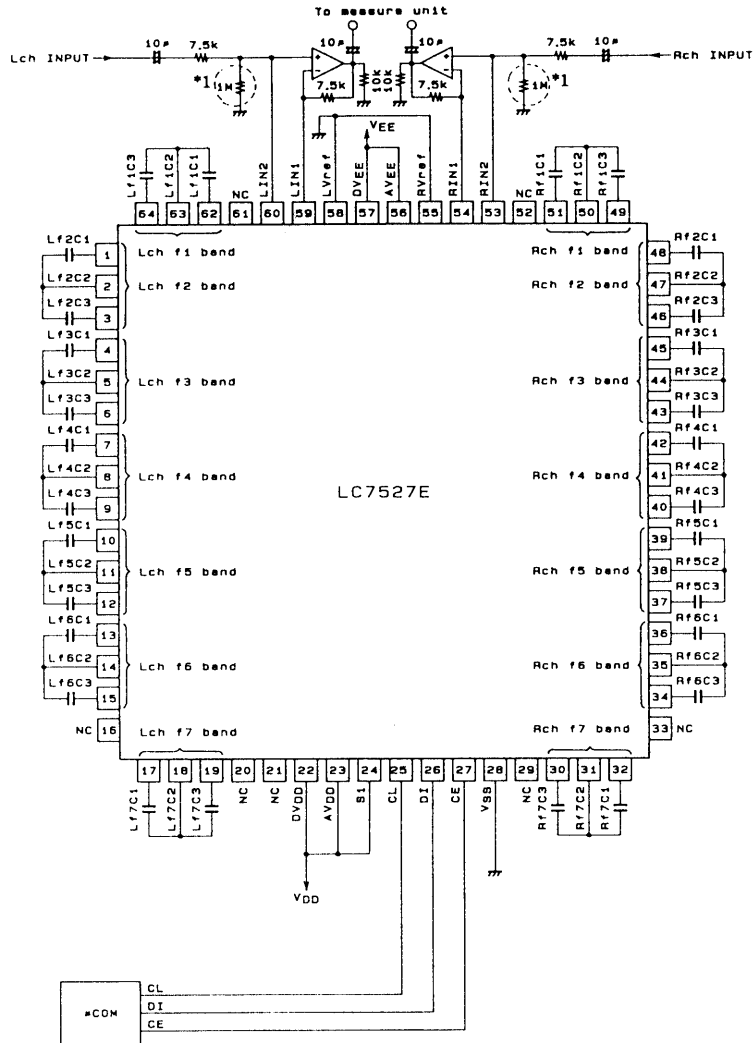
The LC7527E is controlled by inputting stipulated data using the CE, CL, and DI pins. The data has a total of 20 bits, of which eight are address and 12 are data.



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# LC7527E

## Sample Application Circuit



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Unit (resistance: Ω, capacitance: F)

Note: If at all possible, use bipolar capacitors for all capacitors that do not have a polarity specified.

\*1. A resistor of about 100 kΩ is recommended if impulse noise (popping sounds) is a problem.

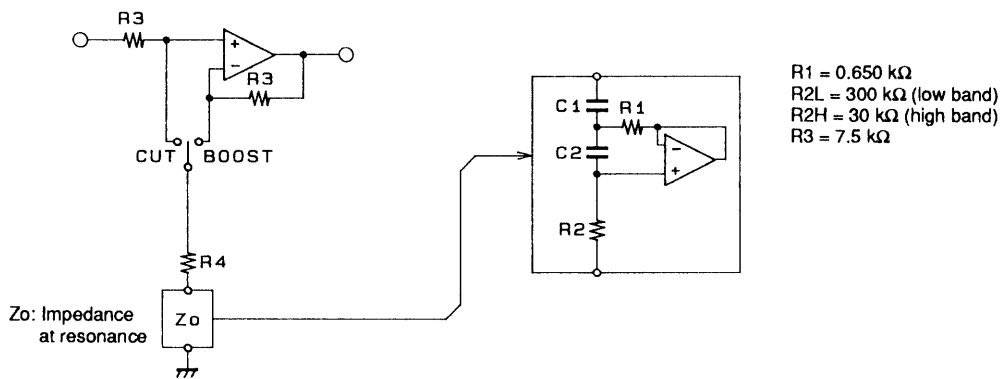


**External Component Value Calculations**

The external capacitors required for each band in the LC7527E are the structural elements in semiconductor inductors (simulated inductors). The remainder of this section presents the equivalent circuits and the formulas used to determine the center frequencies.

1. Semiconductor Inductor Equivalent Circuit

The LC7527E provides circuits with differing constants for the low and high bands.



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2. Calculation Example

Specifications: 1) Center frequency:  $F_0 = 63 \text{ Hz}$

2) Q at maximum boost:  $Q_{+12 \text{ dB}} = 1.05$

- Derive the sharpness  $Q_0$  of the semiconductor inductor itself.

$$Q_0 = \frac{(R1 + R4)}{R1} \times Q_{+12 \text{ dB}} \approx 4.064 \quad \text{See the internal equivalent circuit figure for R4.}$$

- Derive C1.

$$C1 = 1/2\pi F_0 R1 Q_0 \approx 0.953 \text{ (}\mu\text{F)}$$

- Derive C2.

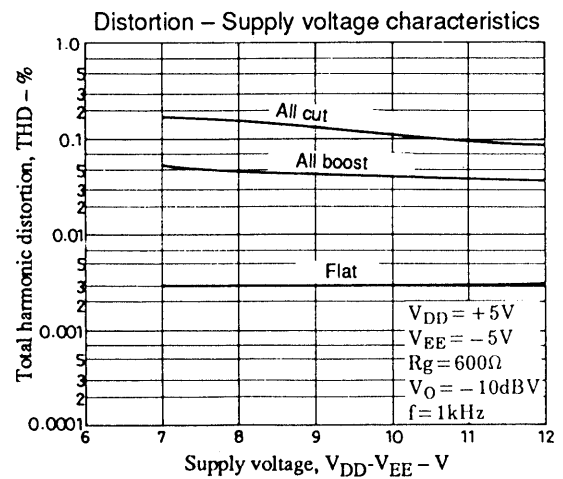
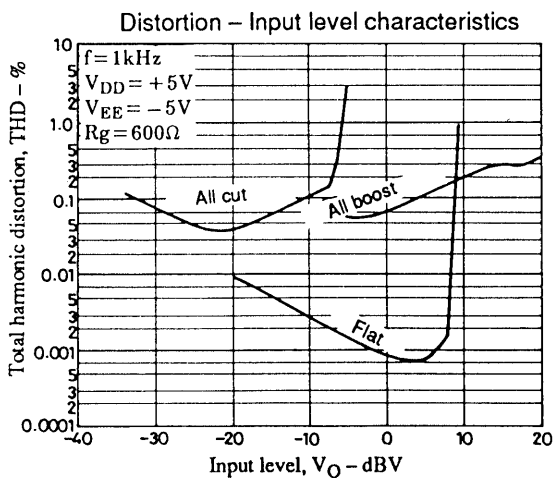
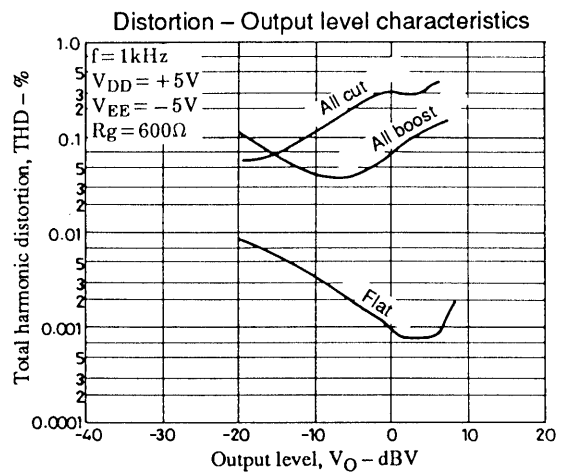
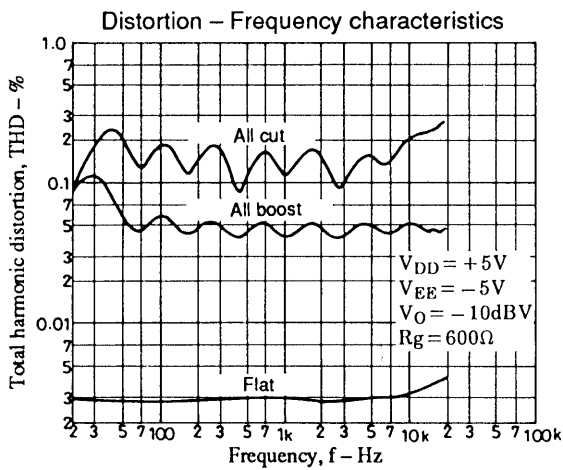
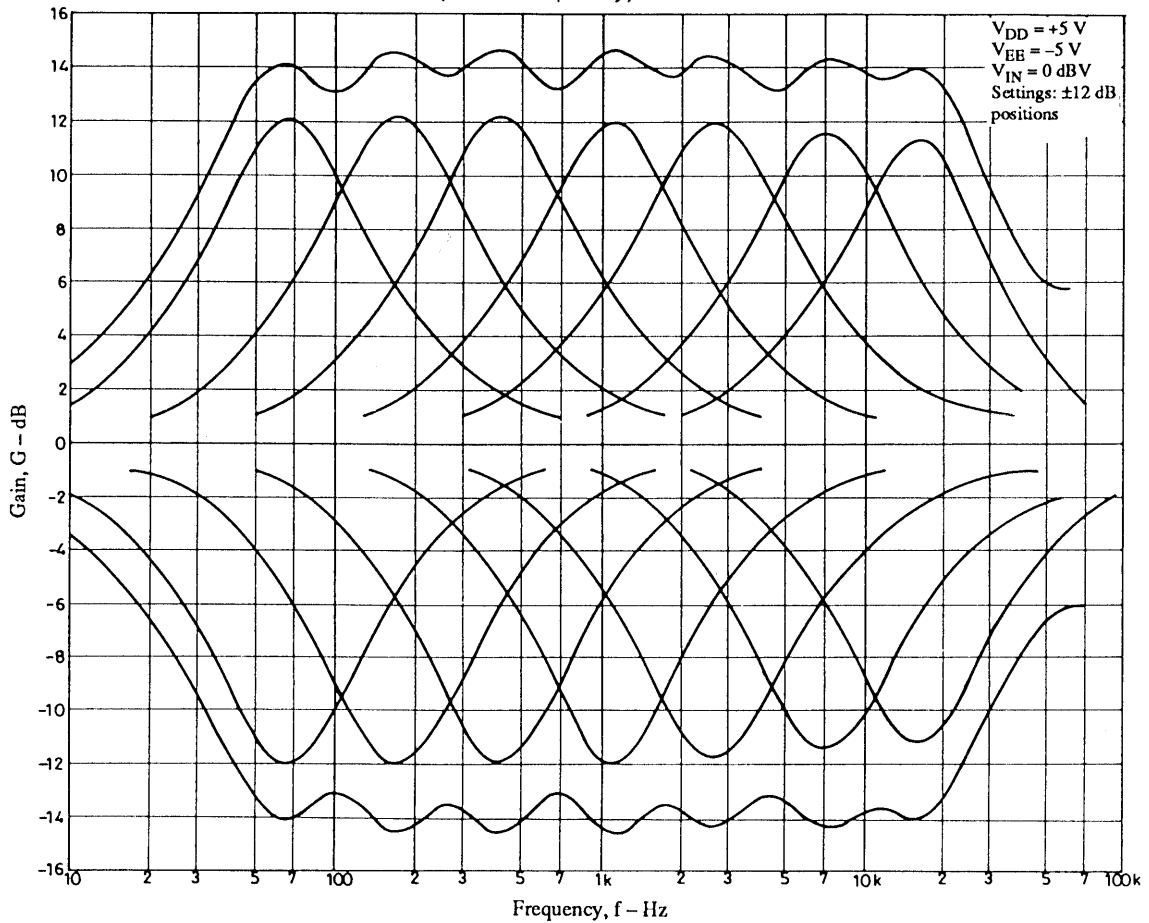
$$C2 = Q_0/2\pi F_0 R2 \approx 0.034 \text{ (}\mu\text{F)}$$

3. Sample Values for C1 and C2

Center frequency $F_0$ (Hz)	C1 (F)	C2 (F)
63	0.953 $\mu$	0.034 $\mu$
160	0.377 $\mu$	0.014 $\mu$
400	0.151 $\mu$	5390 p
1000	0.060 $\mu$	2156 p
2500	0.024 $\mu$	862 p
6300	9563 p	3422 p
16000	3765 p	1348 p

# LC7527E

fo (center frequency) characteristics



## Usage Notes

1. The states of the internal analog switches are undefined when power is first applied. System output should be muted until control data has been sent to the LC7527E.
2. To prevent the high frequency digital signals associated with data transfers over the CL, CI, and DI pins from generating interference in the analog signals, either guard those lines with a ground pattern or use shielded cables.

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