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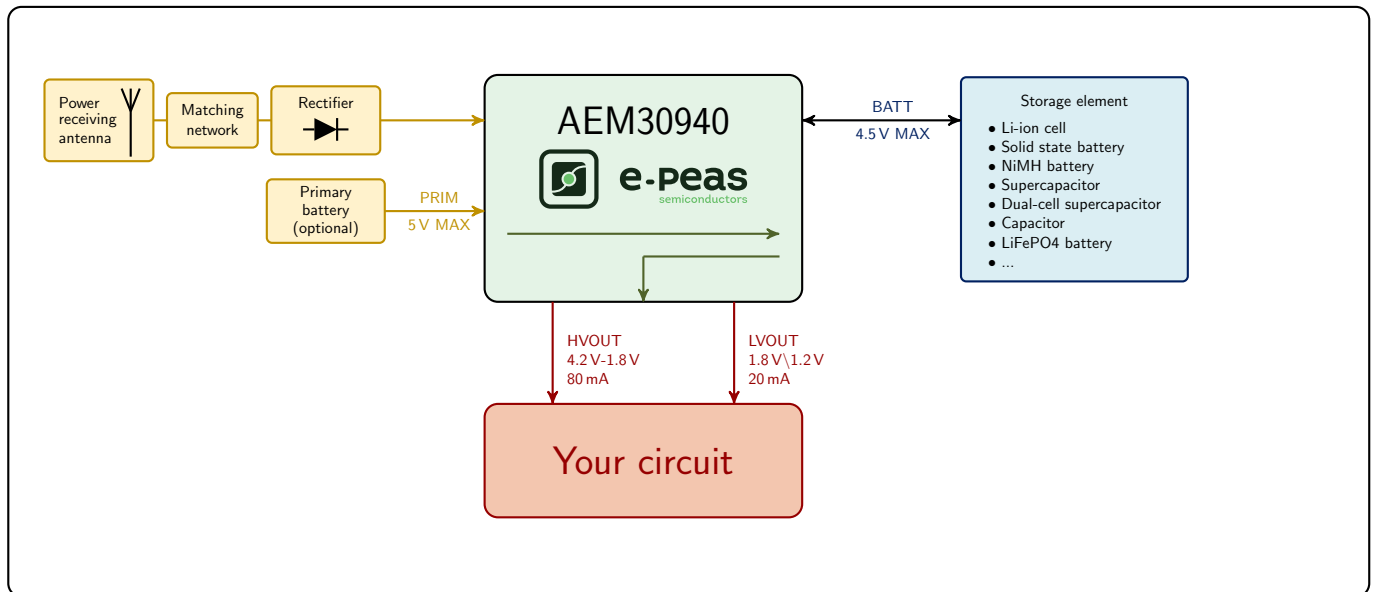


Figure 1: Simplified schematic view

1 Introduction

The AEM30940 is a full-featured energy efficient power management circuit able to charge a storage element (battery or supercapacitor, connected to **BATT**) from an energy source (connected to **SRC**) as well as to supply loads at different operating voltages through two power supplying LDO regulators (**LVOUT** and **HVOUT**).

The heart of the AEM30940 is a cascade of two regulated switching converters, namely the boost converter and the buck converter with high-power conversion efficiencies (See Page 18).

At first start-up, as soon as a required cold-start voltage of 380 mV and a scant amount of power of just 3 μ W available from the harvested energy source, the AEM coldstarts. After the cold start, the AEM can extract the power available from the source as long as the input voltage is comprised between 50 mV and 5 V.

Through three configuration pins (**CFG[2:0]**), the user can select a specific operating mode from a range of seven modes that cover most application requirements without any dedicated external component. Those operating modes define the LDO output voltages and the protection levels of the storage element. Note that a custom mode allows the user to define his own storage element protection levels and the output voltage of the high-voltage LDO (See Page 11).

The Maximum Power Point (MPP) ratio can be configured using two configuration pins (**SELMPP[1:0]**) (See Page 12).

Two logic control pins are provided (**ENLV** and **ENHV**) to dynamically activate or deactivate the LDO regulators that supply the low- and high-voltage load, respectively. The status pin **STATUS[0]** alerts the user that the LDOs are operational and can be enabled. This signal can also be used to enable an optional external regulator.

If the battery voltage gets depleted, the LDOs are power gated and the controller is no longer supplied by the storage element to protect it from further discharge. Around 600 ms before the shutdown of the AEM, the status pin **STATUS[1]** alerts the user for a clean shutdown of the system.

However, if the storage element gets depleted and an optional primary battery is connected on **PRIM**, the chip automatically uses it as a source to recharge the storage element before switching back to the ambient source. This guarantees continuous operation even under the most adverse conditions (See Page 10). **STATUS[1]** is asserted when the primary battery is providing power.

The status of the MPP controller is reported with one dedicated status pin (**STATUS[2]**). The status pin is asserted when a MPP calculation is being performed.

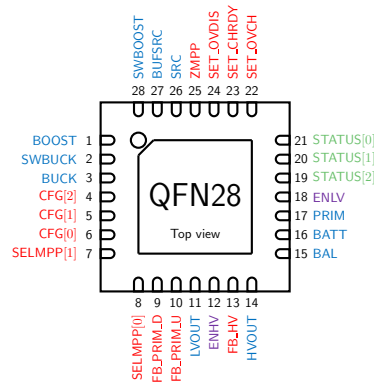


Figure 2: Pinout diagram QFN28

NAME	PIN NUMBER	FUNCTION	
Power pins			
BOOST	1	Output of the boost converter.	
SWBUCK	2	Switching node of the buck converter.	
BUCK	3	Output of the buck converter.	
LVOUT	11	Output of the low voltage LDO regulator.	
HVOUT	14	Output of the high voltage LDO regulator.	
BAL	15	Connection to mid-point of a dual-cell supercapacitor (optional). Must be connected to GND if not used.	
BATT	16	Connection to the energy storage element, battery or capacitor. Cannot be left floating.	
PRIM	17	Connection to the primary battery (optional). Must be connected to GND if not used.	
SRC	26	Connection to the harvested energy source.	
BUFSRC	27	Connection to an external capacitor buffering the boost converter input.	
SWBOOST	28	Switching node of the boost converter.	
Configuration pins			
CFG[2]	4	Used for the configuration of the threshold voltages for the energy storage element and the output voltage of the LDOs.	See Page 11
CFG[1]	5		
CFG[0]	6		
SELMPP[1]	7	Used for the configuration of the MPP ratio.	
SELMPP[0]	8		
FB_PRIM_D	9	Used for the configuration of the primary battery (optional). Must be connected to GND if not used.	
FB_PRIM_U	10		
FB_HV	13	Used the configuration of the high-voltage LDO in the custom mode (optional). Must be left floating if not used.	
SET_OVCH	22	Used for the configuration of the threshold voltages for the energy storage element in the custom mode (optional). Must be left floating if not used.	
SET_CHRDY	23		
SET_OVDIS	24		
ZMPPT	25	Used for the configuration of the ZMPPT (optional). Must be left floating if not used.	
Control pins			
ENHV	12	Enabling pin for the high-voltage LDO.	See Page 9
ENLV	18	Enabling pin for the low-voltage LDO.	
Status pins			
STATUS[2]	19	Logic output. Asserted when the AEM performs a MPP evaluation.	See Pages 8-10
STATUS[1]	20	Logic output. Asserted if the battery voltage falls below <i>Vovdis</i> or if the AEM is taking energy from the primary battery.	
STATUS[0]	21	Logic output. Asserted when the LDOs can be enabled.	
Other pins			
GND	Exposed Pad	Ground connection, should be solidly tied to the PCB ground plane.	

Table 1: Pins description

2 Absolute Maximum Ratings

Parameter	Rating
Vsrc	5.5 V
Operating junction temperature	-40 °C to +125 °C
Storage temperature	-65 °C to +150 °C

Table 2: Absolute maximum ratings

3 Thermal Resistance

Package	θ_{JA}	θ_{JC}	Unit
QFN28	38.3	2.183	°C/W

Table 3: Thermal data

ESD CAUTION



ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE
 These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

4 Typical Electrical Characteristics at 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power conversion						
PsrcCs	Source power required for cold start.	During cold start	3			μ W
Vsrc	Input voltage of the energy source.	During cold start	0.38		5	V
		After cold start	0.05		5	
Vboost	Output of the boost converter.	During normal operation	2.2		4.5	V
Vbuck	Output of the buck converter.	During normal operation	2	2.2	2.5	
Storage element						
Vbatt	Voltage on the storage element.	Rechargeable battery	2.2		4.5	V
		Capacitor	0		4.5	V
Tcrit	Time before shutdown after STATUS[1] has been asserted.		400	600	800	ms
Vprim	Voltage on the primary battery.		0.6		5	V
Vfb_prim_u	Feedback for the minimal voltage level on the primary battery.		0.15		1.1	V
Vovch	Maximum voltage accepted on the storage element before disabling the boost converter.	see Table 8	2.3		4.5	V
Vchrdy	Minimum voltage required on the storage element before enabling the LDOs after a cold start.	see Table 8	2.25		4.45	V
Vovdis	Minimum voltage accepted on the storage element before switching to primary battery or entering into a shutdown.	see Table 8	2.2		4.4	V
Low-voltage LDO regulator						
Vlv	Output voltage of the low-voltage LDO.	see Table 8	1.2		1.8	V
llv	Load current from the low-voltage LDO.		0		20	mA
High-voltage LDO regulator						
Vhv	Output voltage of the high-voltage LDO.	see Table 8	1.8		Vbatt - 0.3 V	V
lhv	Load current from the high-voltage LDO.		0		80	mA
Logic output pins						
STATUS[2:0]	Logic output levels on the status pins.	Logic high (VOH)	1.98	Vbatt		V
		Logic low (VOL)	-0.1		0.1	V

Table 4: Electrical characteristics

5 Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit	
External components						
CSRC	Capacitor decoupling the input source.	8	10	22	μF	
CBOOST	Capacitor of the boost converter.	10	22	25	μF	
LBOOST	Inductor of the boost converter.	4	10	25	μH	
CBUCK	Capacitor of the buck converter.	8	10	22	μF	
LBUCK	Inductor of the buck converter.	4	10	25	μH	
CLV	Capacitor decoupling the low-voltage LDO regulator.	8	10	14	μF	
CHV	Capacitor decoupling the high-voltage LDO regulator.	8	10	14	μF	
CBATT	Optional - Capacitor on BATT if no storage element is connected (see Page 12).	150			μF	
RT	Optional - Resistor for setting threshold voltage of the battery in custom mode. Equal to $R1 + R2 + R3 + R4$ (see Page 11).	1	10	100	$\text{M}\Omega$	
RV	Optional - Resistor for setting the output voltage of the high-voltage LDO in custom mode. Equal to $R5 + R6$ (see Page 11)	1	10	40	$\text{M}\Omega$	
RZMPP	Optional - Resistor for the ZMPPT configuration (see Page 12).	10		1M	Ω	
RP	Optional - Resistor to be used with a primary battery. Equal to $R7 + R8$ (see Page 12).	100		500	$\text{k}\Omega$	
Logic input pins						
ENHV	Enabling pin for the high-voltage LDO ¹ .	Logic high (VOH)	1.75	V _{buck}	V _{buck}	V
		Logic low (VOL)	-0.01	0	0.01	
ENLV	Enabling pin for the low-voltage LDO ² .	Logic high (VOH)	1.75	V _{buck}	V _{boost}	V
		Logic low (VOL)	-0.01	0	0.01	
SELMPP[1:0]	Configuration pins for the MPP evaluation (see Table 9).	Logic high (VOH)	Connect to BUCK			
		Logic low (VOL)	Connect to GND			
CFG[2:0]	Configuration pins for the storage element (see Table 8).	Logic high (VOH)	Connect to BUCK			
		Logic low (VOL)	Connect to GND			
STONBATT	Configuration pin to select the energy source during the cold start.	Logic high (VOH)	Connect to BATT			
		Logic low (VOL)	Connect to GND			

Table 5: Recommended operating conditions

Note 1: ENHV can be dynamically driven by a logic signal from the LV domain. For a static usage, connect to BUCK (High) or GND (Low).

Note 2: ENLV can be dynamically driven by a logic signal from the HV domain. For a static usage, connect to BUCK or BOOST (High) or GND (Low).

6 Functional Block Diagram

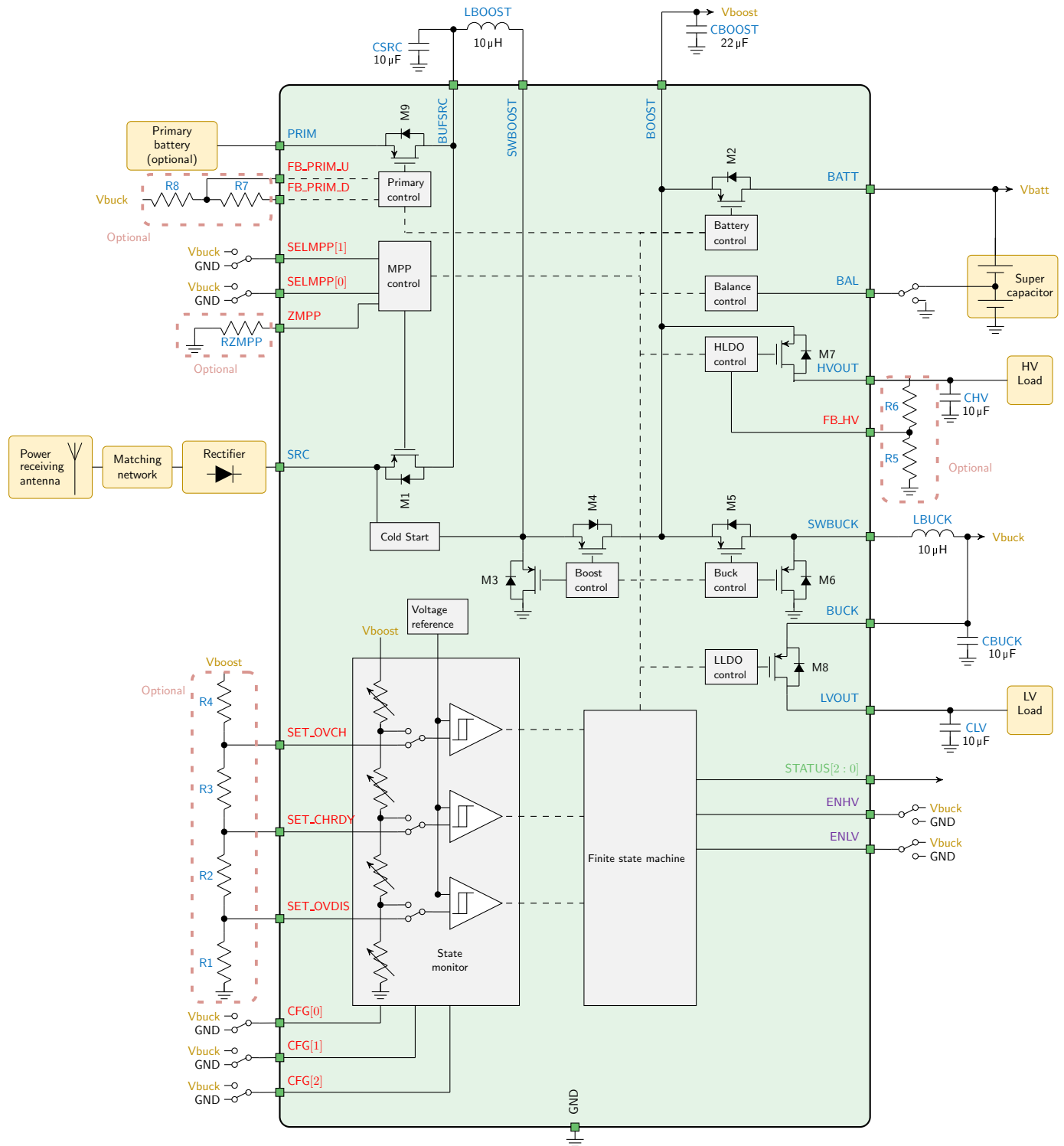


Figure 3: Functional block diagram

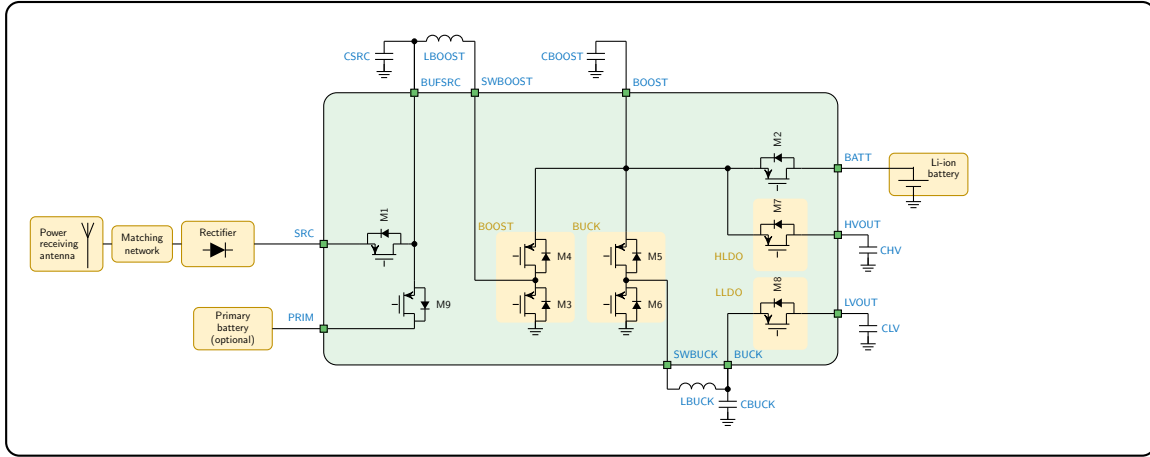


Figure 4: Simplified schematic view of the AEM30940

7 Theory of Operation

7.1 Deep sleep & Wake up modes

The **DEEP SLEEP MODE** is a state where all nodes are deeply discharged and there is no available energy to be harvested. As soon as the required cold-start voltage of 380 mV and a sparse amount of power of just 3 μ W becomes available on **SRC**, the **WAKE UP MODE** is activated. **Vboost** and **Vbuck** rises up to a voltage of 2.2 V. **Vboost** then rises alone up to **Vovch**.

At that stage, both LDOs are internally deactivated. Therefore, **STATUS[0]** is equal to 0 as shown in Figure 9 and Figure 10.

When **Vboost** reaches **Vovch**, two scenarios are possible: in the first scenario, a super-capacitor or a capacitor having a voltage lower than **Vchrdy** is connected to the **BATT** node. In the second scenario, a charged battery is connected to the **BATT** node.

Frequency [MHz]	Pin [dBm]	Pin [μ W]
863-868	-18.2	15.1
915-921	-18.5	14.1
925-960	-17.8	16.6
1805-1880	-16.4	22.9
2110-2170	-14	39.8
2400-2500	-9.5	112.2

Table 6: Minimum input power for the cold start (typical). Results obtained with the matching network and rectifier designed by e-peas

Supercapacitor as a storage element

If the storage element is a supercapacitor, the storage element may need to be charged from 0 V. The boost converter charges **BATT** from the input source and by modulating the conduc-

tance of M2. During the charge of the **BATT** node, both LDOs are deactivated and **STATUS[0]** is de-asserted. When **Vbatt** reaches **Vchrdy**, the circuit enters **NORMAL MODE**, **STATUS[0]** is asserted and the LDOs can be activated by the user using the **ENLV** and **ENHV** control pins as shown in Figure 9.

Battery as a storage element

If the storage element is a battery, but its voltage is lower than **Vchrdy**, then the storage element first needs to be charged until it reaches **Vchrdy**. Once **Vbatt** exceeds **Vchrdy**, or if the battery was initially charged above **Vchrdy**, the circuit enters **NORMAL MODE**. **STATUS[0]** is asserted and the LDOs can be activated by the user thanks to **ENLV** and **ENHV** as shown in Figure 10.

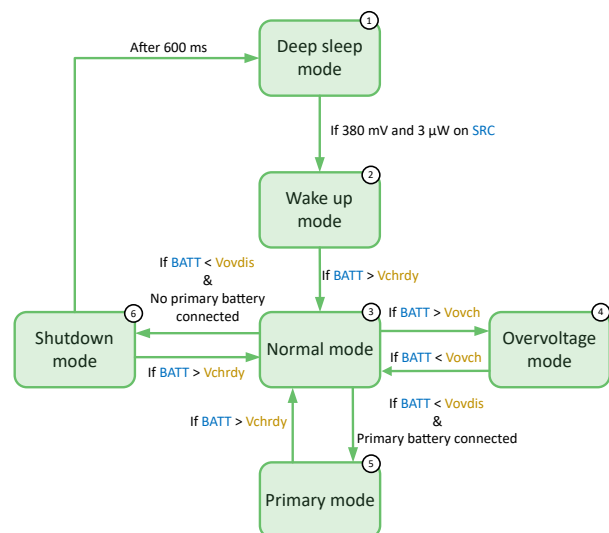


Figure 5: Diagram of the AEM30940 modes

7.2 Normal mode

Once the AEM enters **NORMAL MODE**, three scenarios are possible:

- There is enough power provided by the source to maintain V_{batt} above V_{ovdis} but V_{batt} is below V_{ovch} . In that case, the circuit remains **NORMAL MODE**.
- The source provides more power than the load consumes, and V_{batt} increases above V_{ovch} , the circuit enters into the **OVERVOLTAGE MODE**, as explained in the **Overvoltage mode** section.
- Due to a lack of power from the source, V_{batt} falls below V_{ovdis} . In this case, either the circuit enters **SHUTDOWN MODE** as explained in **Shutdown mode** section or, if a charged primary battery is connected on **PRIM**, the circuit enters **PRIMARY MODE** as explained in the **Primary mode** section.

Matching network and rectifier

To connect AC sources to the AEM30940, an external rectifier is required as well as a matching network in the case RF energy harvesting. The objective of the matching network is to modify the impedance relationship between the RF source and the rectifier in order to optimize the power transfer over a frequency band and an input power range. For RF applications, external high frequency rectifiers as well as matching networks are available ¹ for the following RF bands: 828 MHz, 915 MHz, 945 MHz (GSM900), 1.84 GHz (GSM1800), 2.11 GHz (3G), 2.45 GHz (WiFi).

Boost

The boost (or step-up) converter raises the voltage available at **BUFSRC** to a level suitable for charging the storage element, in the range of 2.2 V to 4.5 V, according to the system configuration. This voltage (V_{boost}) is available at the **BOOST** pin. The switching transistors of the boost converter are M3 and M4, with the switching node available externally at **SW-BOOST**. The reactive power components of this converter are the external inductor and capacitor **LBOOST** and **CBOOST**. Periodically, the MPP control circuit disconnects the source from the **BUFSRC** pin with the transistor M1 in order to measure the open-circuit voltage of the harvester on **SRC** and define the optimal level of voltage. **BUFSRC** is decoupled by the capacitor **CSRC**, which smooths the voltage against the current pulses induced by the boost converter.

The storage element is connected to the **BATT** pin, at a voltage V_{batt} . This node is linked to **BOOST** through the transistor M2. In **NORMAL MODE**, this transistor effectively shorts the battery to the **BOOST** node ($V_{batt} = V_{boost}$). When energy harvesting is occurring, the boost converter delivers a current that is shared between the battery and the loads. M2 is opened to disconnect the storage element when V_{batt} reaches V_{ovdis} . However, in such a scenario, the AEM30940 offers the possibility of connecting a primary battery to recharge V_{batt} up to the $V_{chr dy}$. The transistor M9 connects **PRIM** to **BUFSRC** and the transistor M1 is opened to disconnect the **SRC**

input pin as explained in the **Primary mode** section and shown in Figure 13.

Buck

The buck (or step-down) converter lowers the voltage from V_{boost} to a constant V_{buck} value of 2.2 V. This voltage is available at the **BUCK** pin. The switching transistors of the buck converter are M5 and M6, with the switching node available externally at **SWBUCK**. The reactive power components of the buck converter are the external inductor **LBUCK** and the capacitor **CBUCK**.

LDO outputs

Two LDOs are available to supply loads at different operating voltages:

Through M7, V_{boost} supplies the high-voltage LDO that powers its load through **HVOUT**. This regulator delivers a clean voltage (V_{hv}) with a maximum current of 80 mA on **HVOUT**. In the built-in configuration modes, an output voltage of 1.8 V, 2.5 V or 3.3 V can be selected. In the custom configuration mode, it is adjustable between 2.2 V and $V_{batt}-0.3$ V. The high-voltage output can be dynamically enabled or disabled with the logic control pin **ENHV**. The output is decoupled by the external capacitor **CHV**.

Through M8, V_{buck} supplies the low-voltage LDO that powers its load through **LVOUT**. This regulator delivers a clean voltage (V_{lv}) of 1.8 V or 1.2 V with a maximum current of 20 mA on **LVOUT**. The low-voltage output can be dynamically enabled or disabled with the logic control pin **ENLV**. The output is decoupled by the external capacitor **CLV**.

Status pin **STATUS[0]** alerts the user when the LDOs can be enabled as explained in the **Deep sleep & Wake up modes** section and in the **Shutdown mode** section. The table below shows the four possible configurations:

ENLV	ENHV	LV output	HV output
1	1	Enabled	Enabled
1	0	Enabled	Disabled
0	1	Disabled	Enabled
0	0	Disabled	Disabled

Table 7: LDOs configurations

7.3 Overvoltage mode

When V_{batt} reaches V_{ovch} , the charge is complete and the internal logic maintains V_{batt} around V_{ovch} with a hysteresis of a few mV as shown in Figure 11 to prevent damage to the storage element and to the internal circuitry. In this configuration, the boost converter is periodically activated to maintain V_{batt} and the LDOs are still available. Moreover, when the boost converter is not activated, the transistor M1 in Figure 4 is opened to prevent current from the source to the storage element when V_{src} is higher than V_{ovch} .

¹Contact support@e-peas.com for additional information

7.4 Primary mode

When V_{batt} drops below V_{ovdis} , the circuit compares the voltage on $PRIM$ with the voltage on FB_PRIM_U to determine whether a charged primary battery is connected on $PRIM$. The voltage on FB_PRIM_U is set thanks to two optional resistances as explained in the [Primary battery configuration](#) section. If the voltage on $PRIM$ divided by 4 is higher than the voltage on FB_PRIM_U , the circuit considers the primary battery as available and the circuit enters **PRIMARY MODE** as shown in Figure 13.

In that mode, transistor M1 is opened and the primary battery is connected to $BUFSRC$ through transistor M9 to become the source of energy for the AEM30940. The chip remains in this mode until V_{batt} reaches V_{chrdy} . When V_{batt} reaches V_{chrdy} , the circuit enters **NORMAL MODE**. As long as the chip is in **PRIMARY MODE**, $STATUS[1]$ is asserted.

If no primary battery is used in the application, $PRIM$, FB_PRIM_U and FB_PRIM_D must be tied to GND.

7.5 Shutdown mode

When V_{batt} drops below V_{ovdis} and no power is available from a primary battery, the circuit enters **SHUTDOWN MODE** as shown in Figure 12 to prevent deep discharge potentially leading to damage to the storage element and instability of the LDOs. The circuit asserts $STATUS[1]$ to warn the system that a shutdown will occur. Both LDO regulators remain enabled. If no primary battery is used, this allows the load, whether it is powered on $LVOUT$ or $HVOUT$, to be interrupted by the low-to-high transition of $STATUS[1]$, and to take all appropriate actions before power shutdown.

If energy at the input source is available and V_{batt} recovers to V_{chrdy} within T_{crit} (~ 600 ms), the AEM returns in **NORMAL MODE**. But if, after T_{crit} , V_{batt} does not reach V_{chrdy} , the circuit enters **DEEP SLEEP MODE**. The LDOs are deactivated and $BATT$ is disconnected from $BOOST$ to avoid damaging the battery due to the overdischarge. From now, the AEM will have to go through the wake-up procedure described in the [Deep sleep & Wake up modes](#) section.

7.6 Maximum power point tracking

During **NORMAL MODE**, **SHUTDOWN MODE** and a part of **WAKE UP MODE**, the boost converter is regulated thanks to

an internal MPPT (Maximum Power Point Tracking) module. V_{mpp} is the voltage level of the MPP, and depends on the input power available at the source. The MPPT module evaluates V_{mpp} as a given fraction of V_{oc} , the open-circuit voltage of the source. By temporarily disconnecting the source from $CSRC$ as shown in Figure 4 for 5.12 ms, the MPPT module receives from and maintains knowledge of V_{mpp} . This sampling occurs approximatively every 0.33 s.

With the exception of this sampling process, the voltage across the source, V_{src} , is continuously compared to V_{mpp} . When V_{src} exceeds V_{mpp} by a small hysteresis, the boost converter is switched on, extracting electrical charges from the source and lowering its voltage. When V_{src} falls below V_{mpp} by a small hysteresis, the boost converter is switched off, allowing the harvester to accumulate new electrical charges into $CSRC$, which restores its voltage. In this manner, the boost converter regulates its input voltage so that the electrical current (or flow of electrical charges) that enters the boost converter yields the best power transfer from the harvester under any ambient conditions. The AEM30940 supports any V_{mpp} level in the range from 0.05 V to 5 V. It offers a choice of four values for the V_{mpp}/V_{oc} fraction or to match the input impedance of the BOOST converter with an impedance connected to the ZMPP terminal through configuration pins $SELMPP[1:0]$ as shown in Table 9. The status of the MPPT controller is reported through one dedicated status pins ($STATUS[2]$). The status pin is asserted when a MPP calculation is being performed.

7.7 Balun for dual-cell supercapacitor

The balun circuit allows users to balance the internal voltage in a dual-cell supercapacitor in order to avoid damaging the super-capacitor because of excessive voltage on one cell. If BAL is connected to GND, the balun circuit is disabled. This configuration must be used if a battery, a capacitor or a single-cell supercapacitor is connected on $BATT$. If BAL is connected to the node between the cells of a supercapacitor, the balun circuit compensates for any mismatch of the two cells that could lead to over-charge of one of both cells. The balun circuit ensures that BAL remains close to $V_{batt}/2$. This configuration must be used if a dual-cell supercapacitor is connected on $BATT$.

8 System Configuration

Configuration pins			Storage element threshold voltages			LDOs output voltages		Typical use
CFG[2]	CFG[1]	CFG[0]	Vovch	Vchrdy	Vovdis	Vhv	Vlv	
1	1	1	4.12 V	3.67 V	3.60 V	3.3 V	1.8 V	Li-ion battery
1	1	0	4.12 V	4.04 V	3.60 V	3.3 V	1.8 V	Solid state battery
1	0	1	4.12 V	3.67 V	3.01 V	2.5 V	1.8 V	Li-ion/NiMH battery
1	0	0	2.70 V	2.30 V	2.20 V	1.8 V	1.2 V	Single-cell supercapacitor
0	1	1	4.50 V	3.67 V	2.80 V	2.5 V	1.8 V	Dual-cell supercapacitor
0	1	0	4.50 V	3.92 V	3.60 V	3.3 V	1.8 V	Dual-cell supercapacitor
0	0	1	3.63 V	3.10 V	2.80 V	2.5 V	1.8 V	LiFePO4 battery
0	0	0	Custom mode - Programmable through R1 to R6				1.8 V	

Table 8: Usage of CFG[2:0]

8.1 Battery and LDOs configuration

Through three configuration pins (CFG[2:0]), the user can set a particular operating mode from a range that covers most application requirements, without any dedicated external component as shown in Table 8. The three threshold levels are defined as:

- **Vovch** : Maximum voltage accepted on the storage element before disabling the boost converter,
- **Vchrdy** : Minimum voltage required on the storage element after a cold start before enabling the LDOs,
- **Vovdis** : Minimum voltage accepted on the storage element before considering the storage element as depleted.

See [Theory of Operation](#) section for more information about the purposes of these thresholds.

The two LDOs output voltages are called **Vhv** and **Vlv** for the high- and low-output voltages, respectively. In the built-in configuration mode, seven combinations of these voltage levels are hardwired and selectable through the CFG[2:0] configuration pins, covering most application cases. When a predefined configuration is selected, the resistor pins dedicated to a custom configuration should be left floating (SET_OVDIS, SET_CHRDY, SET_OVCH, FB_HV).

A custom mode allows the user to define the **Vovch**, **Vchrdy**, **Vovdis** and **Vhv** threshold voltages.

Custom mode

When CFG[2:0] are tied to GND, the custom mode is selected and all six configuration resistors shown in Figure 6, must be wired as follows:

Vovch, **Vchrdy** and **Vovdis** are defined thanks to R1, R2, R3 and R4. If we define the total resistor (R1 + R2 + R3 + R4) as **RT**, R1, R2, R3 and R4 are calculated as:

- $1\text{ M}\Omega \leq RT \leq 100\text{ M}\Omega$
- $R1 = RT(1\text{ V}/Vovch)$

- $R2 = RT(1\text{ V}/Vchrdy - 1\text{ V}/Vovch)$

- $R3 = RT(1\text{ V}/Vovdis - 1\text{ V}/Vchrdy)$

- $R4 = RT(1 - 1\text{ V}/Vovdis)$

Vhv is defined thanks to R5 and R6. If we define the total resistor (R5 + R6) as **RV**, R5 and R6 are calculated as:

- $1\text{ M}\Omega \leq RV \leq 40\text{ M}\Omega$

- $R5 = RV(1\text{ V}/Vhv)$

- $R6 = RV(1 - 1\text{ V}/Vhv)$

The resistors should have high values to make the additional power consumption negligible. Moreover, the following constraints must be adhered to ensure the functionality of the chip:

- $Vchrdy + 0.05\text{ V} \leq Vovch \leq 4.5\text{ V}$
- $Vovdis + 0.05\text{ V} \leq Vchrdy \leq Vovch - 0.05\text{ V}$
- $2.2\text{ V} \leq Vovdis$
- $Vhv \leq Vovdis - 0.3\text{ V}$

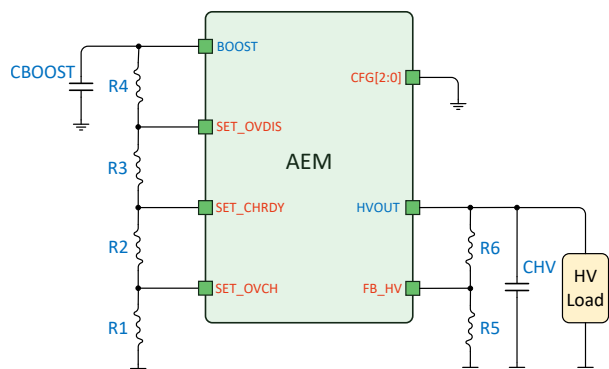


Figure 6: Custom configuration resistors

8.2 MPPT configuration

Two dedicated configuration pins, SELMPP[1:0], allow selecting the MPP tracking ratio based on the characteristic of the input power source.

SELMPP[1]	SELMPP[0]	Vmpp/Voc
0	0	50 %
0	1	65 %
1	0	80 %
1	1	ZMPP

Table 9: Usage of SELMPP[1:0]

8.3 Primary battery configuration

To use the primary battery, it is mandatory to determine V_{prim_min} , the voltage of the primary battery at which it has to be considered as empty. During the evaluation of V_{prim_min} , the circuit connects FB_PRIM_D to GND. The circuit uses a resistive divider between BUCK and FB_PRIM_D to define the voltage on FB_PRIM_U as V_{prim_min} divided by 4. When V_{prim_min} is not evaluated, FB_PRIM_D is left floating to avoid quiescent current on the resistive divider. If we define the total resistor ($R7 + R8$) as R_P , $R7$ and $R8$ are calculated as:

- $100\text{ k}\Omega \leq R_P \leq 500\text{ k}\Omega$
- $R7 = \left(\frac{V_{prim_min}}{4} * R_P\right) / 2.2\text{ V}$
- $R8 = R_P - R7$

Note that FB_PRIM_U and FB_PRIM_D must be tied to GND if no primary battery is used.

8.4 ZMPPT configuration

Instead of working at a ratio of the open-circuit voltage, the AEM30940 can regulate the input impedance of the BOOST converter so that it matches a constant impedance connected to the ZMPP pin (RZMPP). In this case, the AEM30940 regulates V_{src} at a voltage equals to the product of the ZMPP impedance and the current available at the SRC input.

- $10\ \Omega \leq RZMPP \leq 1\text{ M}\Omega$

8.5 No-battery configuration

If the harvested energy source is permanently available and covers the application purposes or if the application does not need to store energy when the harvested energy source is not available, the storage element may be replaced by an external capacitor CBATT of minimum 150 μF .

8.6 Storage element information

The energy storage element of the AEM30940 can be a rechargeable battery, a supercapacitor or a large capacitor (minimum 150 μF). It should be chosen so that its voltage does not fall below V_{ovdis} even during occasional peaks of the load current. If the internal resistance of the storage element cannot sustain this voltage limit, it is advisable to buffer the battery with a capacitor.

The BATT pin that connects the storage element must never be left floating. If the application expects a disconnection of the battery (e.g. because of a user removable connector), the PCB should include a capacitor of at least 150 μF . The leakage current of the storage element should be small as leakage currents directly impact the quiescent current of the subsystem.

External inductors information

The AEM30940 operates with two standard miniature inductors of 10 μH . LBOOST and LBUCK must respectively sustain a peak current of at least 250 mA and 50 mA and a switching frequency of at least 10 MHz. Low equivalent series resistance (ESR) favors the power conversion efficiency of the boost and buck converters.

External capacitors information

The AEM30940 operates with four identical standard miniature ceramic capacitors of 10 μF and one miniature ceramic capacitor of 22 μF . The leakage current of the capacitors should be small as leakage currents directly impact the quiescent current of the subsystem.

CSRC

This capacitor acts as an energy buffer at the input of the boost converter. It prevents large voltage fluctuations when the boost converter is switching. The recommended value is 10 μF +/- 20 %.

CBUCK

This capacitor acts as an energy buffer for the buck converter. It also reduces the voltage ripple induced by the current pulses inherent to the switched mode of the converter. The recommended value is 10 μF +/- 20 %.

CBOOST

This capacitor acts as an energy buffer for the boost converter. It also reduces the voltage ripple induced by the current pulses inherent to the switched mode of the converter. The recommended value is 22 μF +/- 20 %.

CHV and CLV

These capacitors ensure a high-efficiency load regulation of the high-voltage and low-voltage LDO regulators. Closed-loop stability requires the value to be in the range of 8 μF to 14 μF .

9 Typical Application Circuits

9.1 Example circuit 1

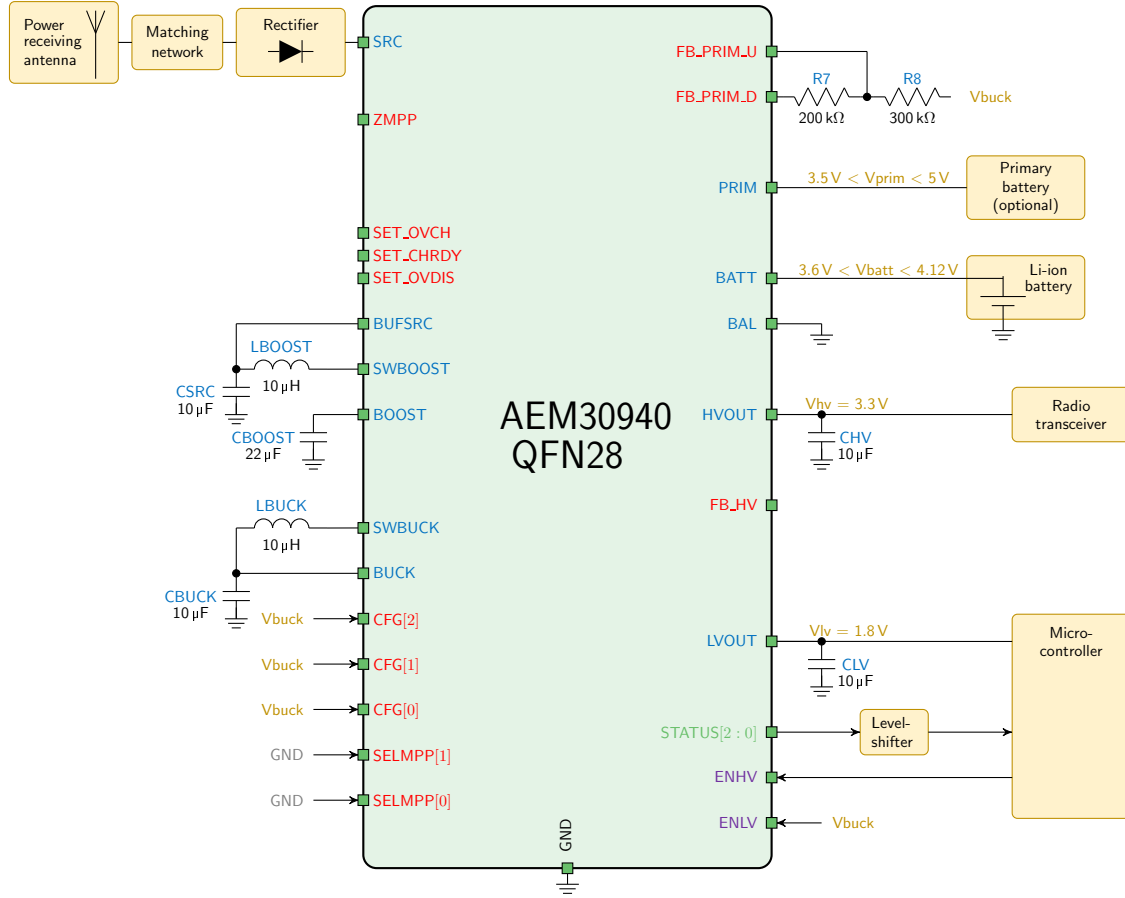


Figure 7: Typical application circuit 1

The energy source is a RF source, and the storage element is a standard Li-ion battery cell. The radio communication makes use of a transceiver that operates from a 3.3 V supply. A micro-controller supplied by a 1.8 V supply controls the application.

This circuit uses a pre-defined operating mode, typical of systems that use standard components for radio and energy storage.

The operating mode pins are connected to:

- $CFG[2:0] = 111$

Referring to Table 8, in this mode, the threshold voltages are:

- $Vovch = 4.12 \text{ V}$
- $Vchrdy = 3.67 \text{ V}$
- $Vovdis = 3.60 \text{ V}$

Moreover, the LDOs output voltages are:

- $Vhv = 3.3 \text{ V}$
- $Vlv = 1.8 \text{ V}$

A primary battery is also connected as a back-up solution. The minimal level allowed on this battery is set at 3.5 V. Following equations on Page 12:

- $RP = 0.5 \text{ M}\Omega$
- $R7 = \left(\frac{3.5 \text{ V}}{4} * 0.5 \text{ M}\Omega\right) / 2.2 \text{ V} = 200 \text{ k}\Omega$
- $R8 = 0.5 \text{ M}\Omega - 200 \text{ k}\Omega = 300 \text{ k}\Omega$

The MPP configuration pins $SELMPP[1:0]$ are tied to GND (logic low), selecting an MPP ratio of 50 %.

The $ENLV$ enable pin for the low-voltage LDO is tied to $BUCK$. The microcontroller will be enabled when $Vbatt$ and $Vboost$ exceed $Vchrdy$ as the low-voltage regulator supplies it.

The application software can enable or disable the radio transceiver with a GPIO connected to $ENHV$.

9.2 Example circuit 2

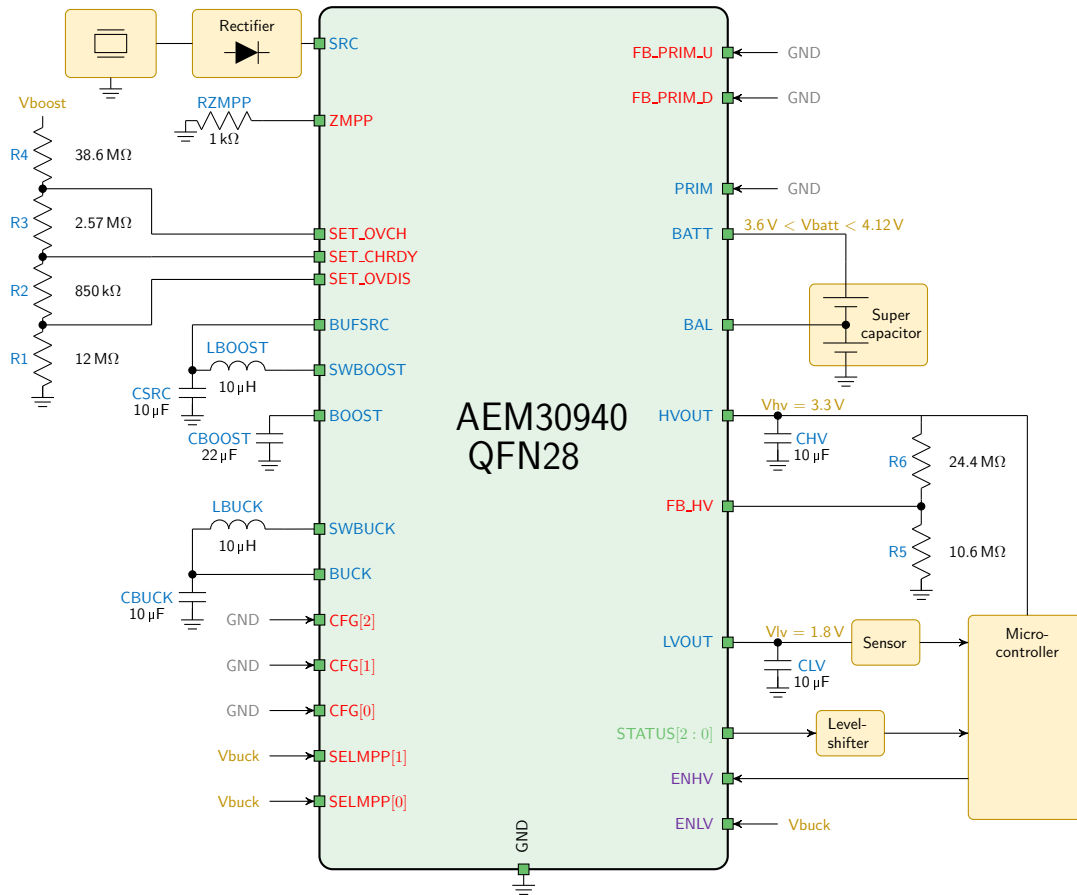


Figure 8: Typical application circuit 2

The energy source is an piezo source, and the storage element is a dual-cell supercapacitor. The supercapacitor can be completely depleted during the cold start.

Moreover, **BAL** is connected to the dual-cell supercapacitor to compensate for any mismatch between the two cells and in that way protect the supercapacitor.

A micro-controller pilots and collects information from a sensor. The operating mode pins are connected to:

- $CFG[2:0] = 000$

The user wants a custom configuration with **Vovch**, **Vchrdy** and **Vovdis** at 4.5 V, 4.2 V and 3.5 V, respectively. The user choose 54 MΩ for **RT**. Following the equation in page 11:

- $R1 = 54 \text{ M}\Omega \left(\frac{1 \text{ V}}{4.5 \text{ V}} \right) = 12 \text{ M}\Omega$
- $R2 = 54 \text{ M}\Omega \left(\frac{1 \text{ V}}{4.2 \text{ V}} - \frac{1 \text{ V}}{4.5 \text{ V}} \right) = 850 \text{ k}\Omega$
- $R3 = 54 \text{ M}\Omega \left(\frac{1 \text{ V}}{3.5 \text{ V}} - \frac{1 \text{ V}}{4.2 \text{ V}} \right) = 2.57 \text{ M}\Omega$

- $R4 = 54 \text{ M}\Omega \left(1 - \frac{1 \text{ V}}{3.5 \text{ V}} \right) = 38.6 \text{ M}\Omega$

In the custom mode, the **Vlv** equals 1.8 V and the application software can enable or disable the sensor with a GPIO connected to **ENLV**.

On **Vhv**, the user wants a 3.3 V voltage. As shown in page 11, the user chooses a resistor **RV** equal to 35 MΩ

- $R5 = 35 \text{ M}\Omega \left(\frac{1 \text{ V}}{3.3 \text{ V}} \right) = 10.6 \text{ M}\Omega$
- $R6 = 35 \text{ M}\Omega \left(1 - \frac{1 \text{ V}}{3.3 \text{ V}} \right) = 24.4 \text{ M}\Omega$

The **ENHV** enable pin for the high-voltage LDO is tied to **BUCK**. The microcontroller is enabled when **Vbatt** and **Vboost** exceeds **Vchrdy** as the high-voltage regulator supplies it.

The MPP configuration pins **SELMPP[1:0]** are tied to **BUCK** (logic high), selecting the ZMPPT configuration to match a 1 KΩ impedance.

No primary battery is connected and the **PRIM**, **FB_PRIM_U** and **FB_PRIM_D** pins are tied to **GND**.

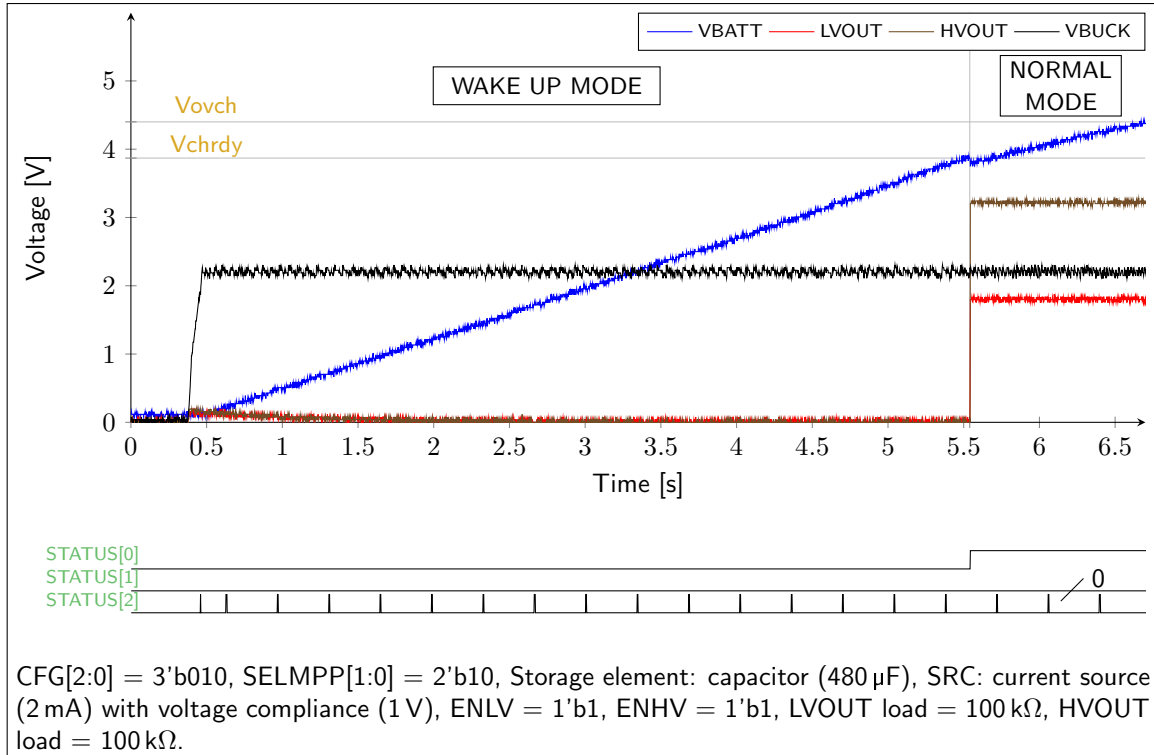


Figure 9: Cold start with a capacitor connected to BATT

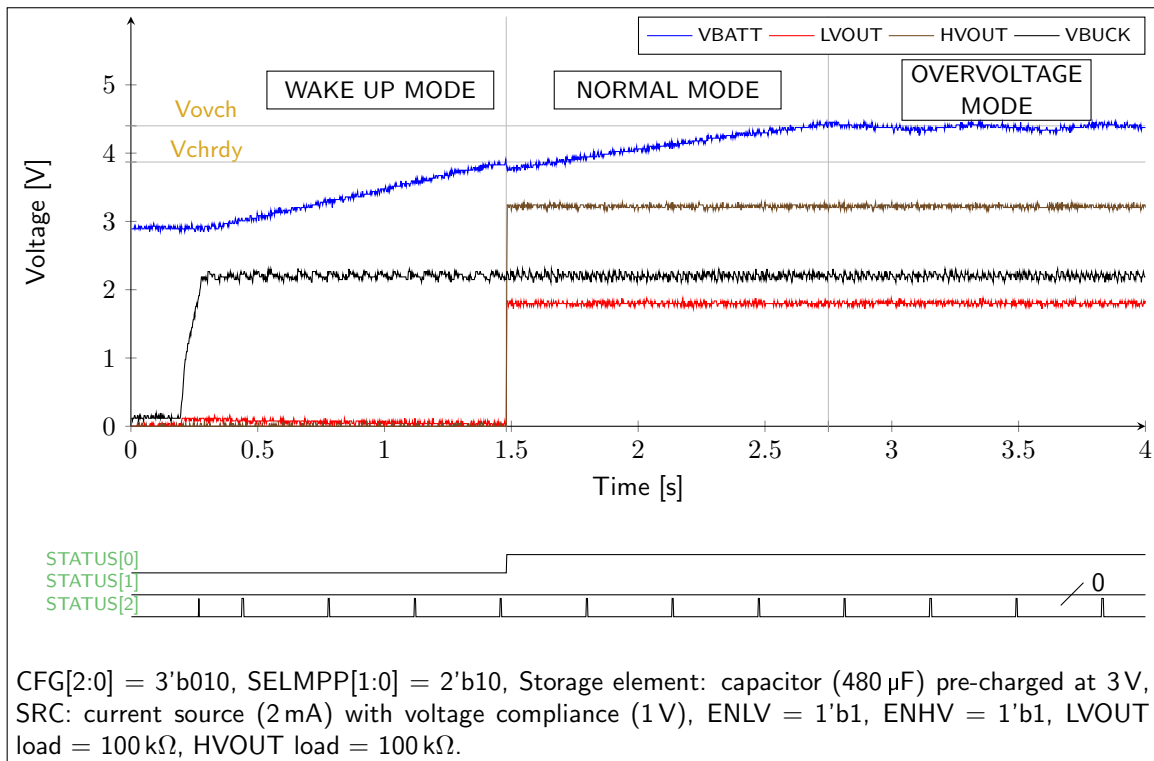


Figure 10: Cold start with a battery connected to BATT

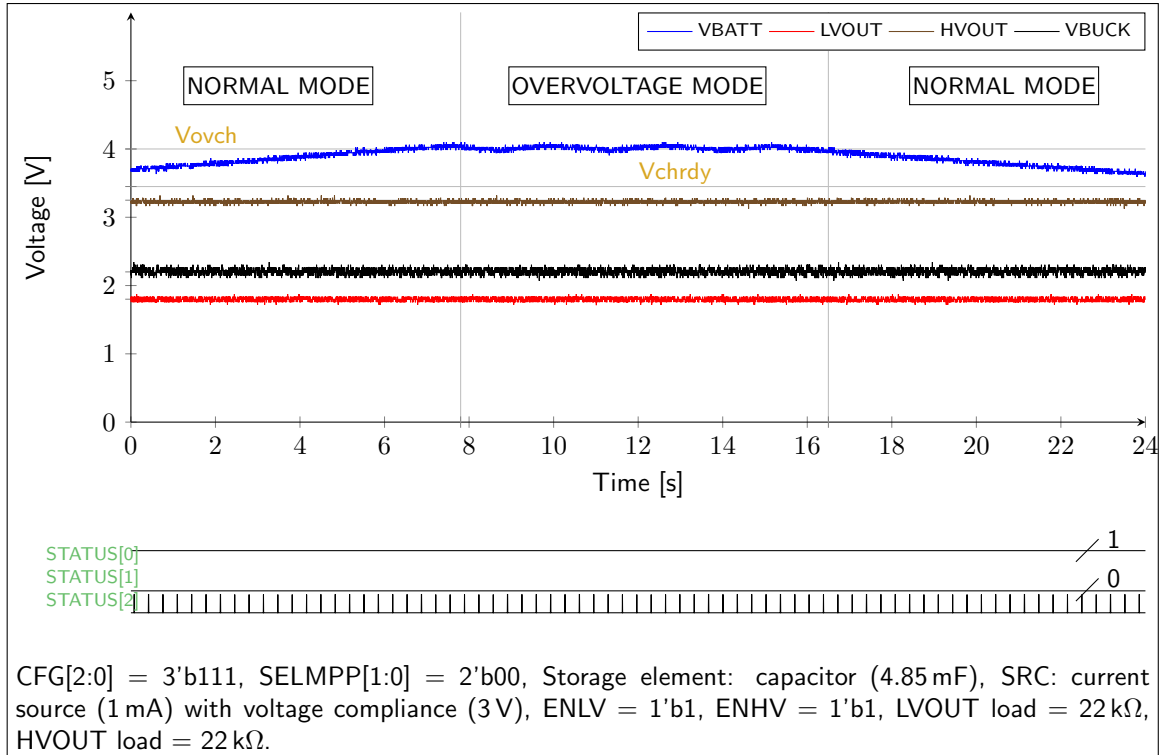


Figure 11: Overtolerance mode

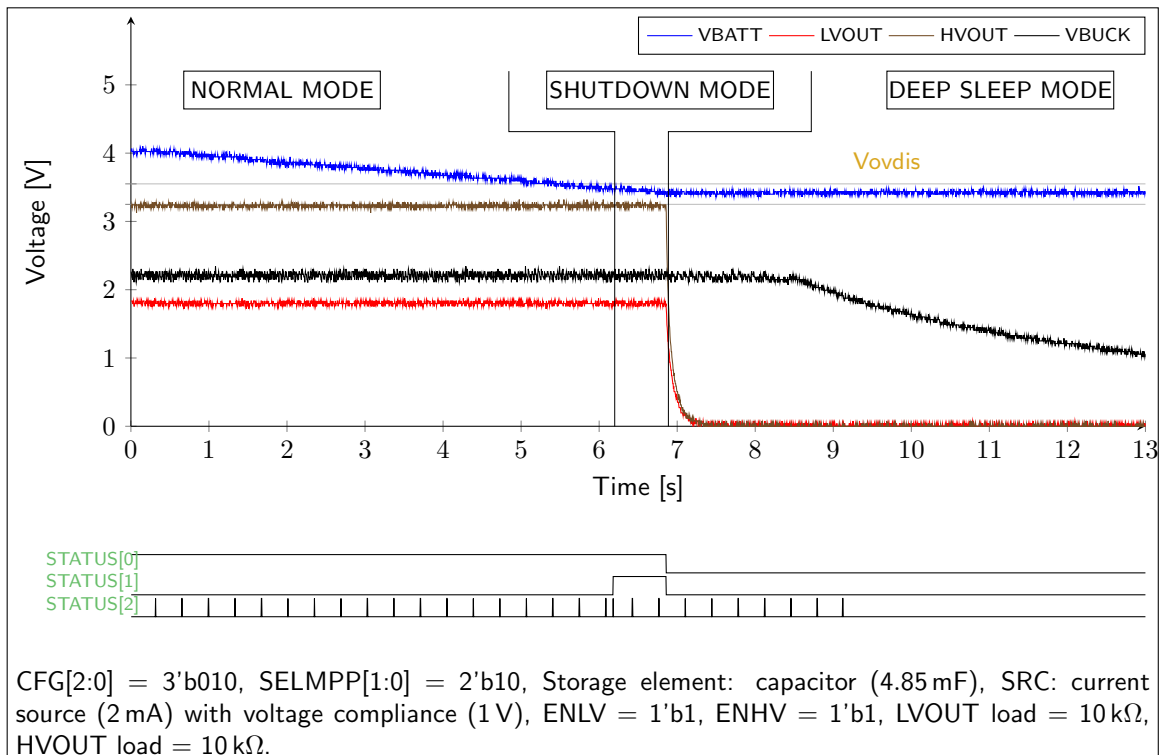


Figure 12: Shutdown mode (without primary battery)

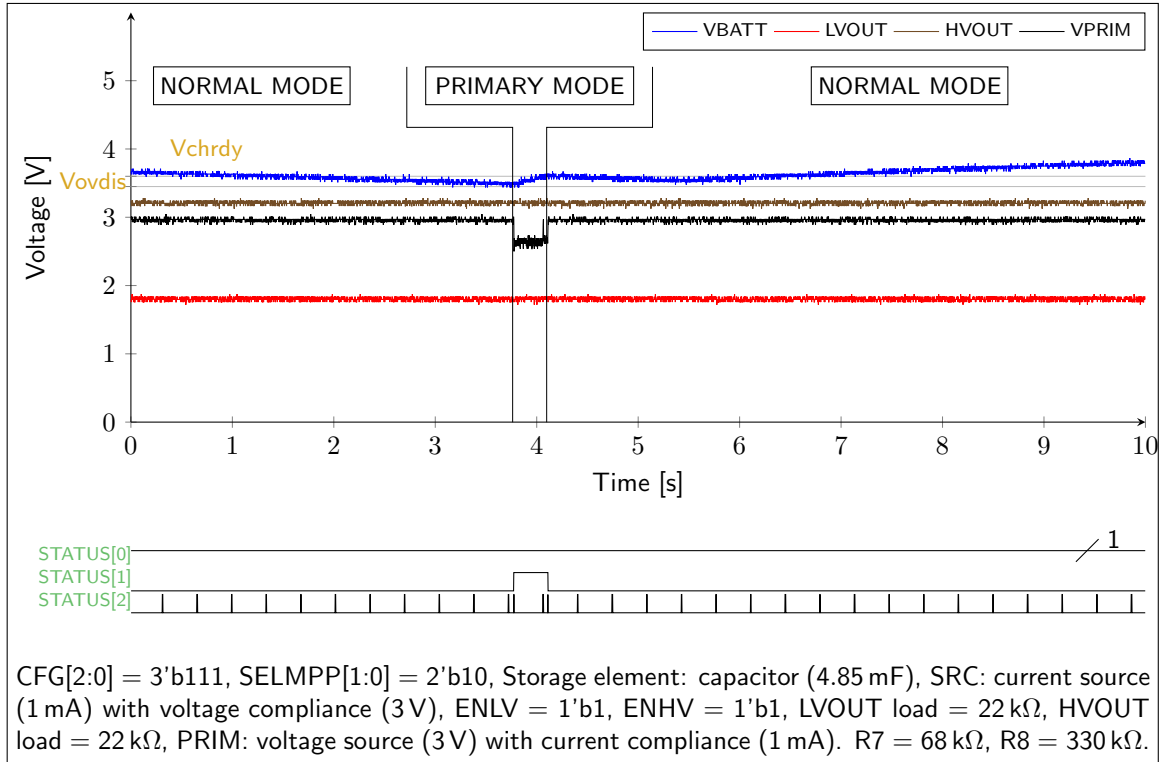


Figure 13: Switch to primary battery if the battery is overdischarged



10 Performance Data

10.1 BOOST conversion efficiency

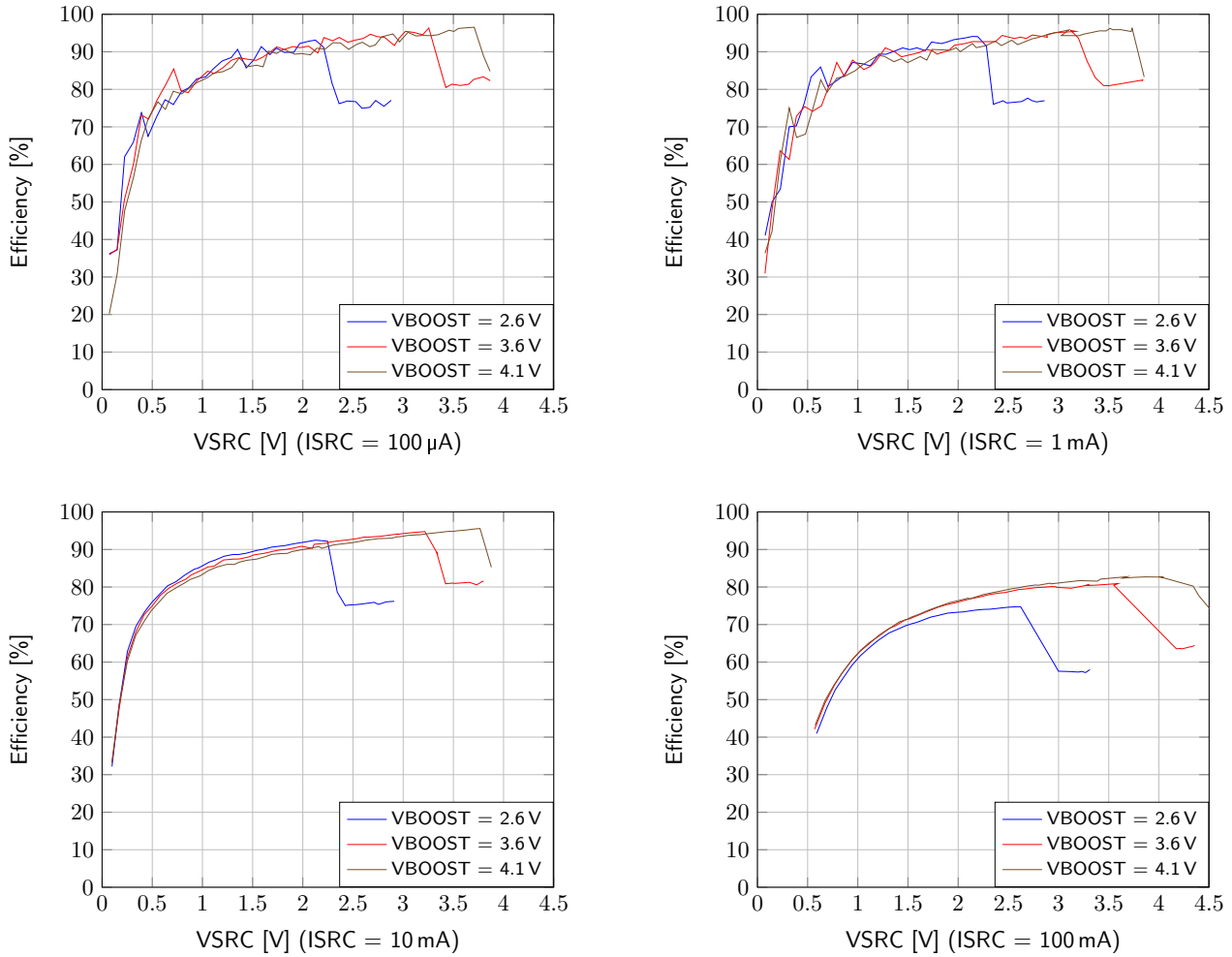


Figure 14: Boost efficiency for Isrc at 100 μ A, 1 mA, 10 mA and 100 mA

10.2 Quiescent current

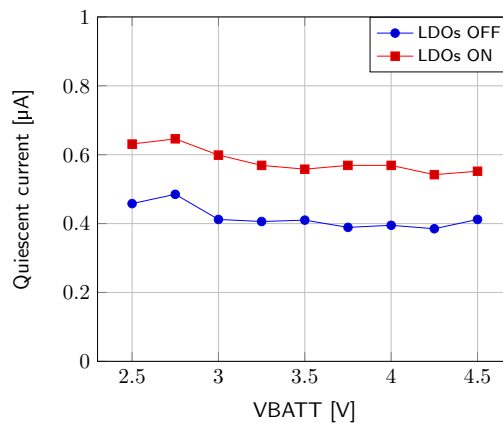


Figure 15: Quiescent current with LDOs on and off

10.3 High-voltage LDO regulation

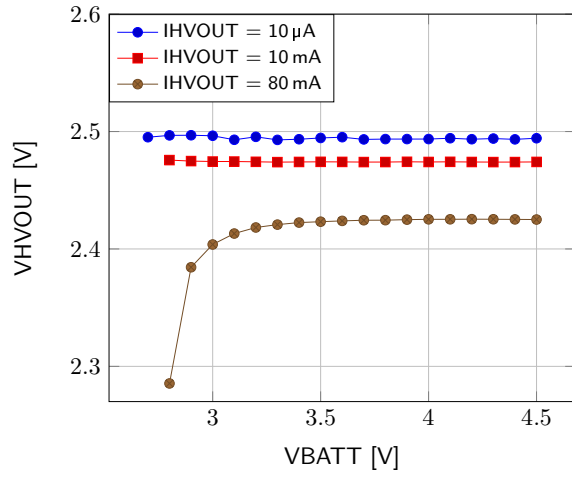
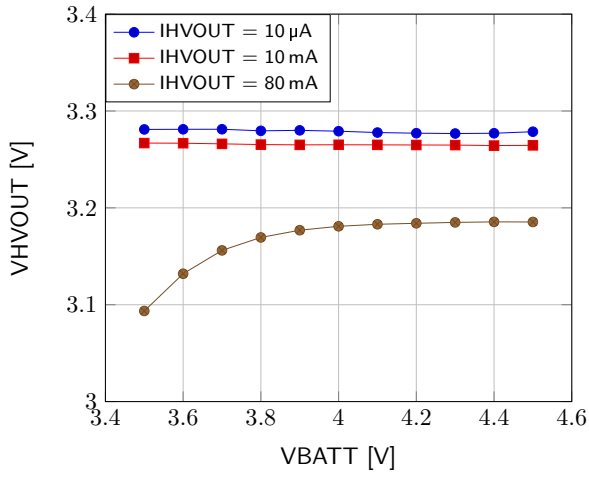


Figure 16: HVOUT at 3.3 V and 2.5 V

10.4 Low-voltage LDO regulation

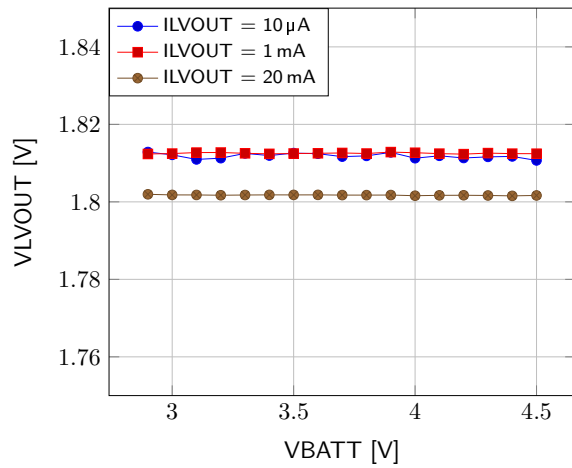
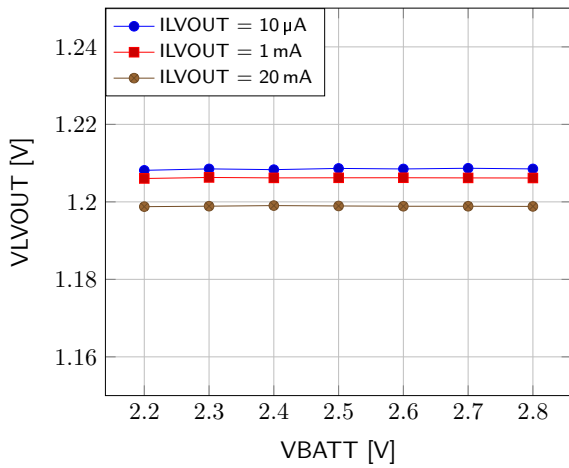


Figure 17: LVOUT at 1.2 V and 1.8 V

10.5 High-voltage LDO efficiency

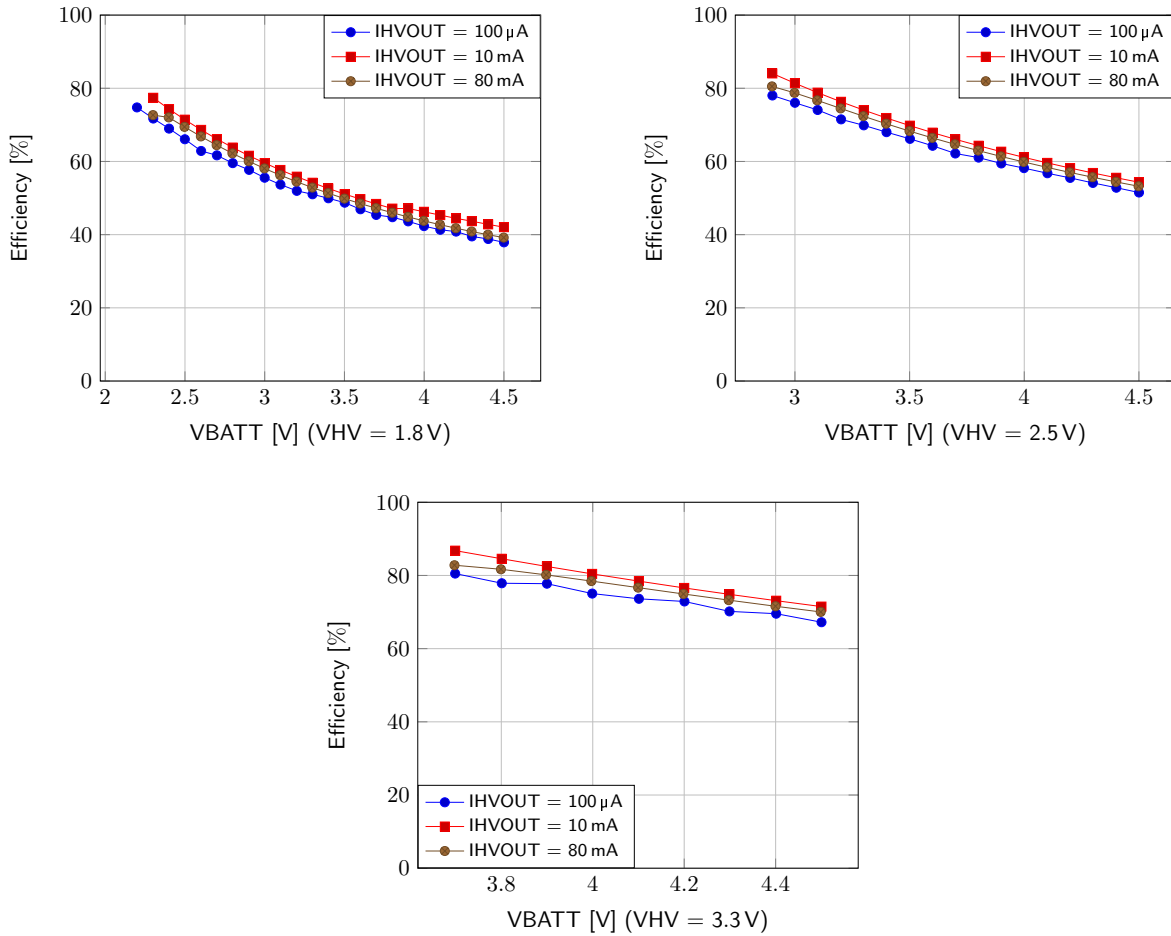


Figure 18: HVOUT efficiency at 1.8 V, 2.5 V and 3.3 V

The theoretical efficiency of a LDO can be simply calculated as $\frac{V_{out}}{V_{in}}$ if quiescent current can be neglected with regards to the output current. In the case of the high-voltage LDO, the theoretical efficiency is equal to $\frac{V_{hv}}{V_{batt}}$.

10.6 Low-voltage LDO efficiency

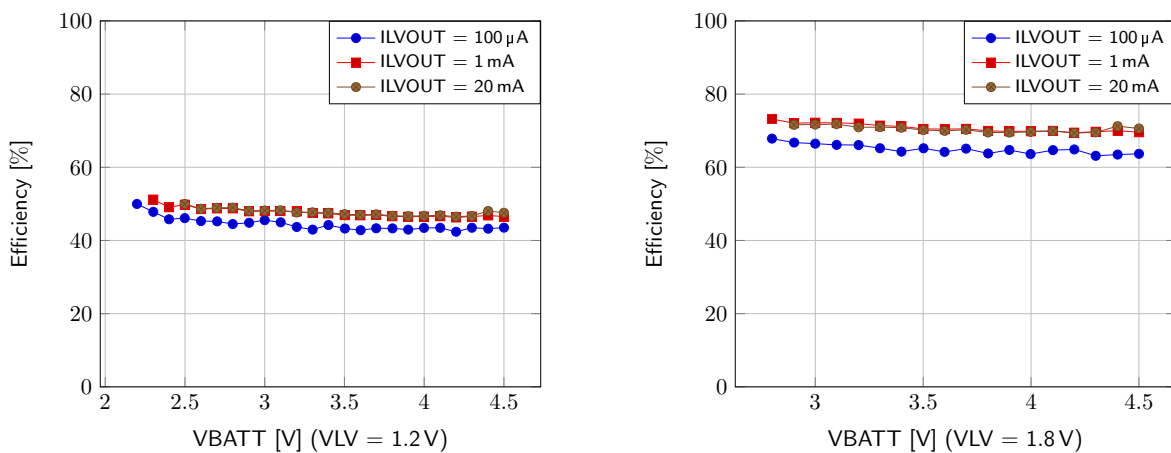


Figure 19: Efficiency of BUCK cascaded with LVOUT at 1.2 V and 1.8 V

The theoretical efficiency of the low-voltage LDO is equal to $\frac{V_{lv}}{V_{buck}}$. Starting from the battery, the efficiency of the buck converter has to be taken into account (see Figure 4). The efficiency between V_{batt} and V_{lv} is therefore equal to $\eta_{buck} \frac{V_{lv}}{V_{buck}}$.

11 Schematic

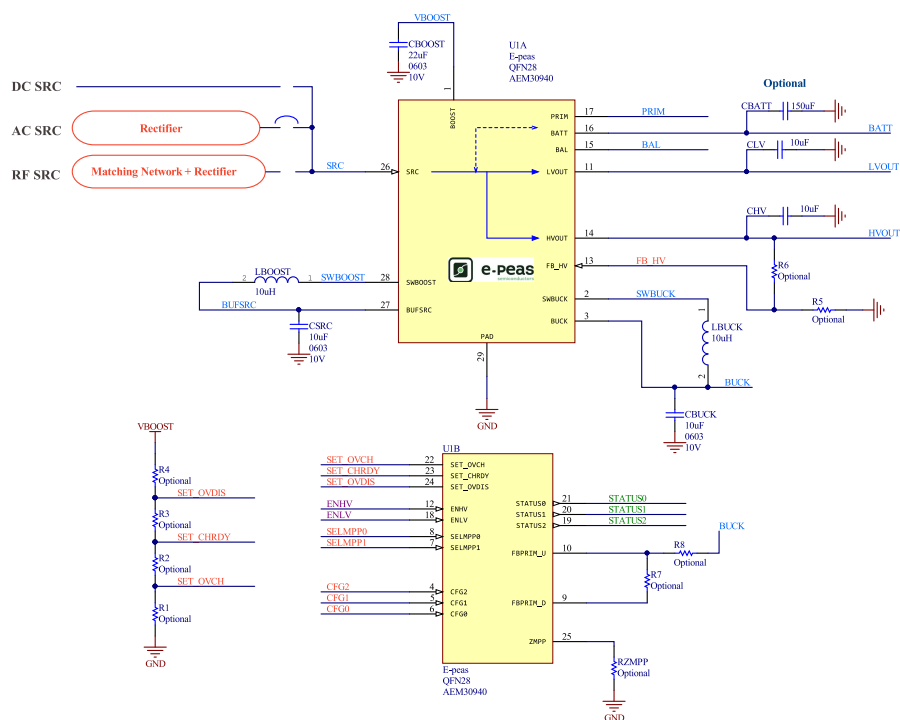


Figure 20: Schematic example

Designator	Description	Quantity	Supplier	Link
CBOOST	Ceramic Cap 22 μ F, 10 V, 20 %, X5R 0603	1	Farnell	http://be.farnell.com/2426957
CBUCK	Ceramic Cap 10 μ F, 10 V, 20 %, X5R	1	Farnell	http://be.farnell.com/2309028
CHV	Ceramic Cap 10 μ F, 10 V, 20 %, X5R	1	Farnell	http://be.farnell.com/2309028
CLV	Ceramic Cap 10 μ F, 10 V, 20 %, X5R	1	Farnell	http://be.farnell.com/2309028
CSRC	Ceramic Cap 10 μ F, 10 V, 20 %, X5R	1	Farnell	http://be.farnell.com/2309028
LBOOST	Power Inductor 10 μ H - 0,55 A - LPS4012	1	Farnell	http://be.farnell.com/2408076
LBUCK	Power Inductor 10 μ H - 0,25 A	1	Farnell	http://be.farnell.com/2215635
U1	AEM30940 - Symbol QFN28	1		order at sales@e-peas.com

Table 10: BOM example for AEM30940 and its required passive components

12 Layout

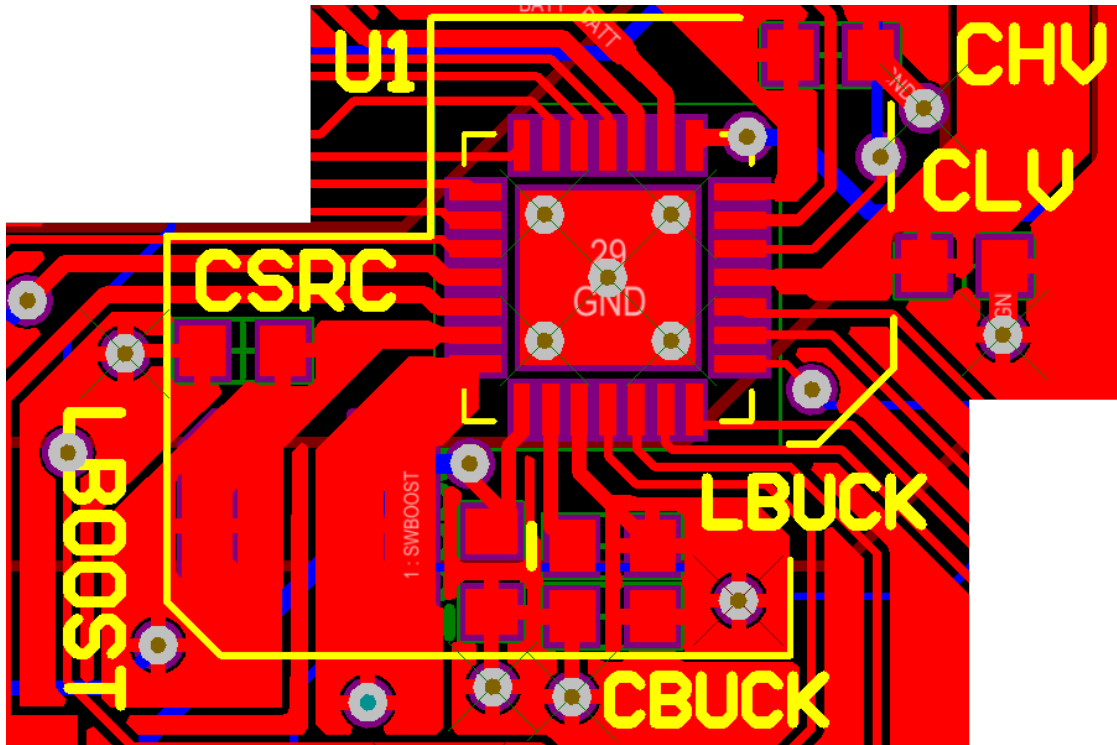


Figure 21: Layout example for the AEM30940 and its passive components

Note: Schematic, symbol and footprint for the e-peas component can be ordered by contacting the e-peas support: support@e-peas.com

13 Package Information

13.1 Plastic quad flatpack no-lead (QFN28 5x5mm)

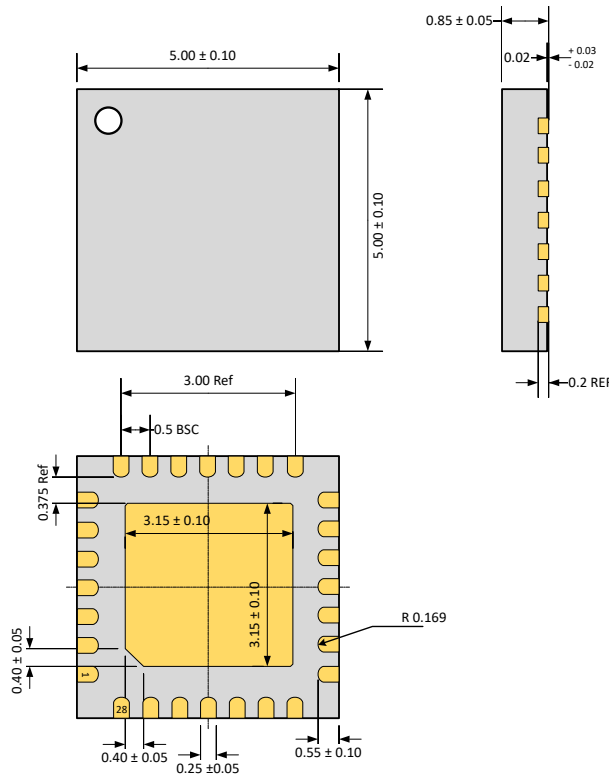


Figure 22: QFN28 5x5mm

13.2 Board layout

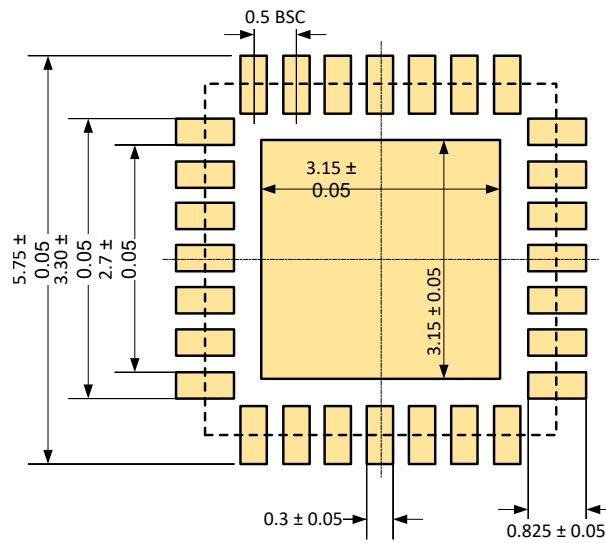


Figure 23: Board layout