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SP97504

HIGH SPEED FOUR BIT EXPANDABLE A TO D CONVERTER

The SP97504 is a fast 4-bit ECL A-D converter, expandable up to 8 bits without additional encoding circuitry. It has been designed to maintain high accuracy at high analog input frequencies.

It can convert at sample rates from DC to 110MHz, with analog inputs above Nyquist frequencies. All output levels are ECL compatible.

The latch function to the device provides on-chip sampling which allows the converter to operate without an external sample and hold. Data is clocked through the device in master/slave fashion, ensuring that all outputs are synchronous.

The SP97504 operates from a +5V, -7V supply.

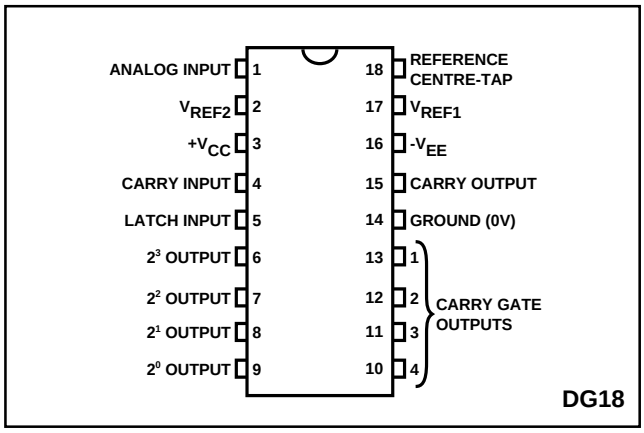

Fig.1 Pin connections - top view

FEATURES

- Operating Temperature Range -30°C to +85°C
- No External Components for 4-Bit Conversion
- 110MHz Conversion Rate
- On-Chip Encoding for Expansion to 8 Bits
- No External Sample and Hold Needed
- Bit Size 10-100mV
- Over 100MHz Full Power Bandwidth
- 10ps Aperture Uncertainty Time
- 8-Bit Accuracy (When Expanded)

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V
Negative supply voltage	-7.5V
Storage temperature range	-65°C to +150°C
Junction operating temperature	<175°C
Lead temperture (soldering 60 sec)	300°C

ORDERING INFORMATION

SP97504 DG (Industrial - Ceramic DIL package)

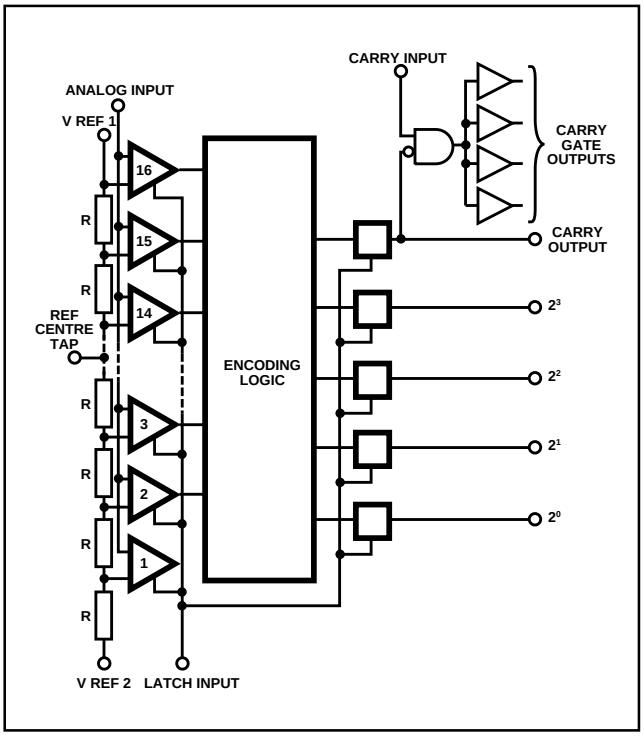

Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{amb} = 25°C, V_{CC} = +5V ± 0.25V, V_{EE} = -7V ± 0.25V, R_L = 100Ω to -2V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Analog input current	I_B		30	100	µA	V_{IN} = 0V
Analog input capacitance	C_{IN}		10		pF	
Common mode range	V_{CM}	-2		+2	V	
Maximum input slew rate			1000		V/µs	
Latch input capacitance	C_{IN}		2		pF	
Positive supply current	I_{CC}		72	92	mA	
Negative supply current	I_{EE}		75	96	mA	
Reference resistor chain			25		Ω	Total
Reference bit size		10		100	mV	
Comparator offset voltage	V_{OS}	-5		+5	mV	
Total power dissipation	P_{DISS}		935	1230	mW	All outputs loaded
Input and output logic levels						
Logic high	V_{OH}	-0.930		-0.720	V	For 100Ω load
Logic low	V_{OL}	-1.90		-1.620	V	to -2V
Minimum latch set-up time	t_S		1.5	2	ns	10mV overdrive
Data uncertain			5		ns	<1mV overdrive
Latch to output propagation delay						
Latch enable to output high	t_{pd} + (E)		6	8	ns	} 10mV overdrive
Latch enable to output low	t_{pd} - (E)		5	8	ns	
Carry input to carry gate	t_{pd} (C)		3	5	ns	
O/P delay						
Maximum sample rate	$F_{C\ MAX}$	100	110		MHz	
Aperture uncertainty time	ta		10		ps	

THERMAL CHARACTERISTICS

θ_{JA}	90°C/W
θ_{JC}	20°C/W

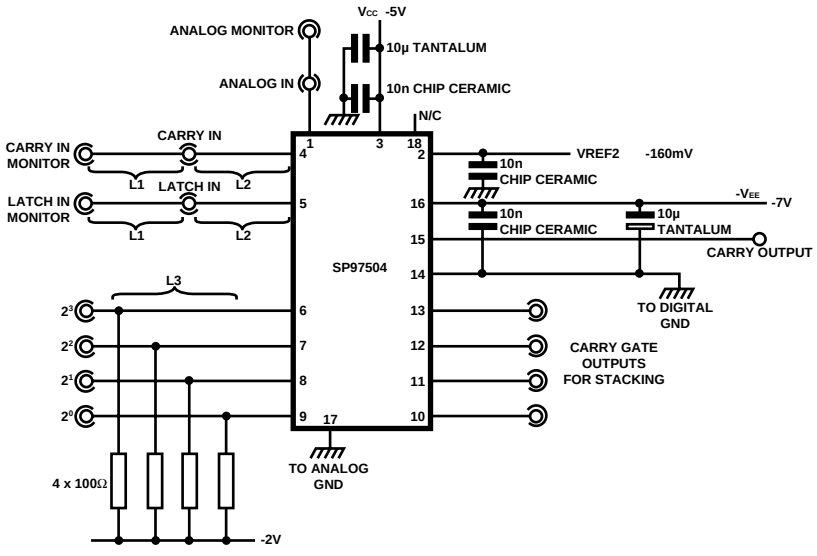

Fig.3 High frequency test circuit

PERFORMANCE CURVES

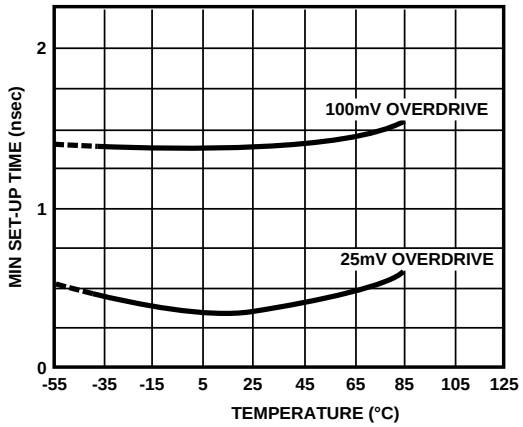

Fig.4 Set-up time as a function of temperature

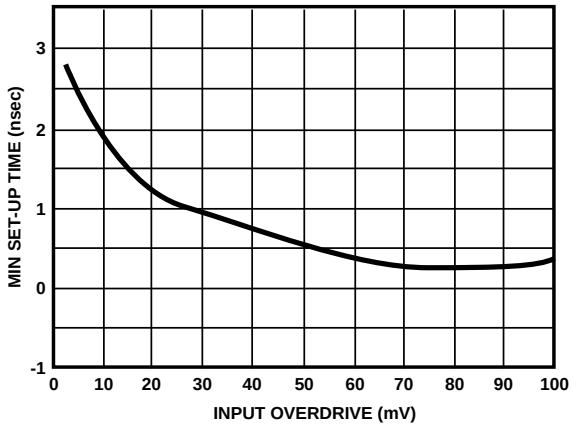

Fig.5 Set-up time as a function of overdrive

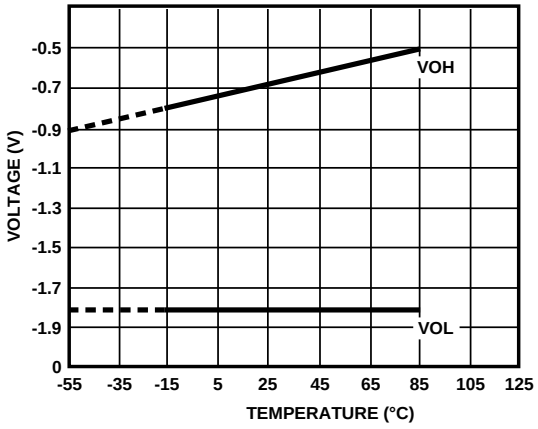

Fig.6 Output logic levels as a function of temperature

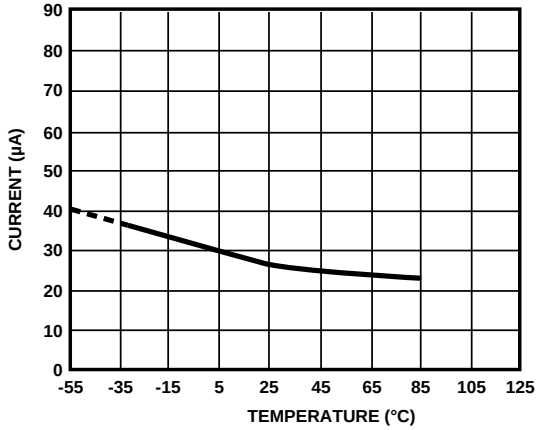

Fig.7 Analog input current as a function of temperature

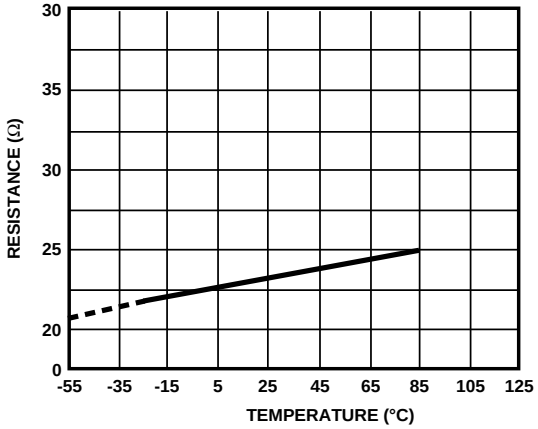

Fig.8 Network resistance as a function of temperature

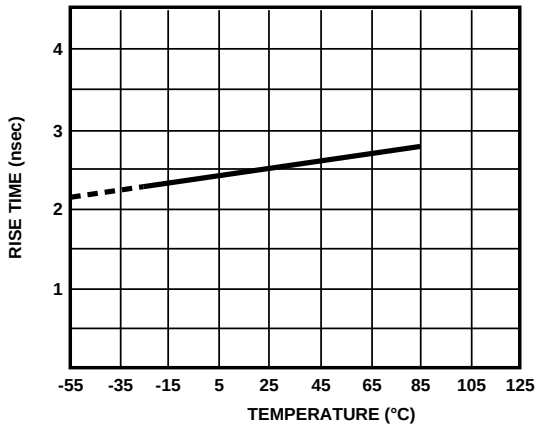

Fig.9 MSB output edge speeds as a function of temperature

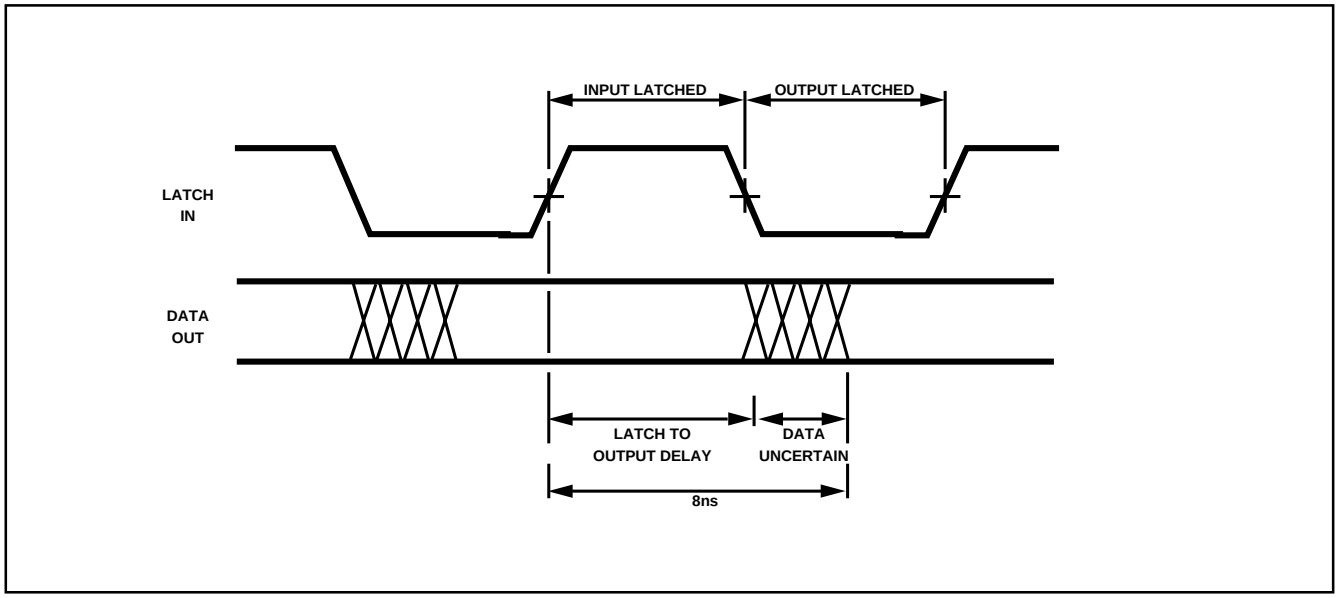

Fig.10 Timing diagram

OPERATING NOTES

1. Carry output (pin 15) is high when the analog input exceeds the top reference voltage (pin 17)

Then the carry gate outputs (pins 10 to 13) go low regardless of carry input (pin 4), when the analog input is between V_{REF} and V_{REF2} and the carry output is low. The carry gate output will be high if the carry input is also high. Similarly if the carry input is low then the carry gate outputs will be low.

2. When used in an ambient temperature in excess of 65°C the SP97504 must be provided with an external heatsink or forced air cooling. This will ensure that the junction temperature does not exceed 175°C.

APPLICATION NOTES

1. The SP97504 is ideally suited to subranging systems as it maintains good accuracy at low reference voltages. This enables the second rank to be driven at higher speed from the subtracting Op-Amp
2. For applications that require low bit error rates at high frequency, the clock signal should be adjusted for 60% ECL low, 40% ECL high mark to space ratio.
3. The SP97504 is ideally suited to applications in communication systems that incorporate multi-level coding (quadrature amplitude modulation).
4. The SP97504 requires a fast edge speed clock. Rise and fall times of <4ns are recommended.

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