

HN58V256A Series HN58V257A Series

Preliminary

32768-word x 8-bit Electrically Erasable and Programmable CMOS ROM

HITACHI

Rev. 0.0
Mar. 15, 1995

The Hitachi HN58V256A and HN58V257A are a electrically erasable and programmable EEPROM's organized as 32768-word x 8-bit. Employing advanced MNOS memory technology and CMOS process and circuitry technology. They also have a 64-byte page programming function to make their write operations faster.

Features

- Single 2.7 to 5.5 V supply
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (64 bytes): 10 ms max
- Fast access time: 120 ns max
- Low power dissipation: 20 mW/MHz, typ
(active)
110 μ W max (standby)
- Ready/Busy ($\diamond$)*1
- Data polling and Toggle bit
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by $\overline{RES}$ pin ($\diamond$)*1

Notes: 1. All through this datasheet, the mark ($\diamond$) indicates the function supported by only the HN58V257A series (32 pin package).

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.



ADE-203-357(Z)

HITAS049

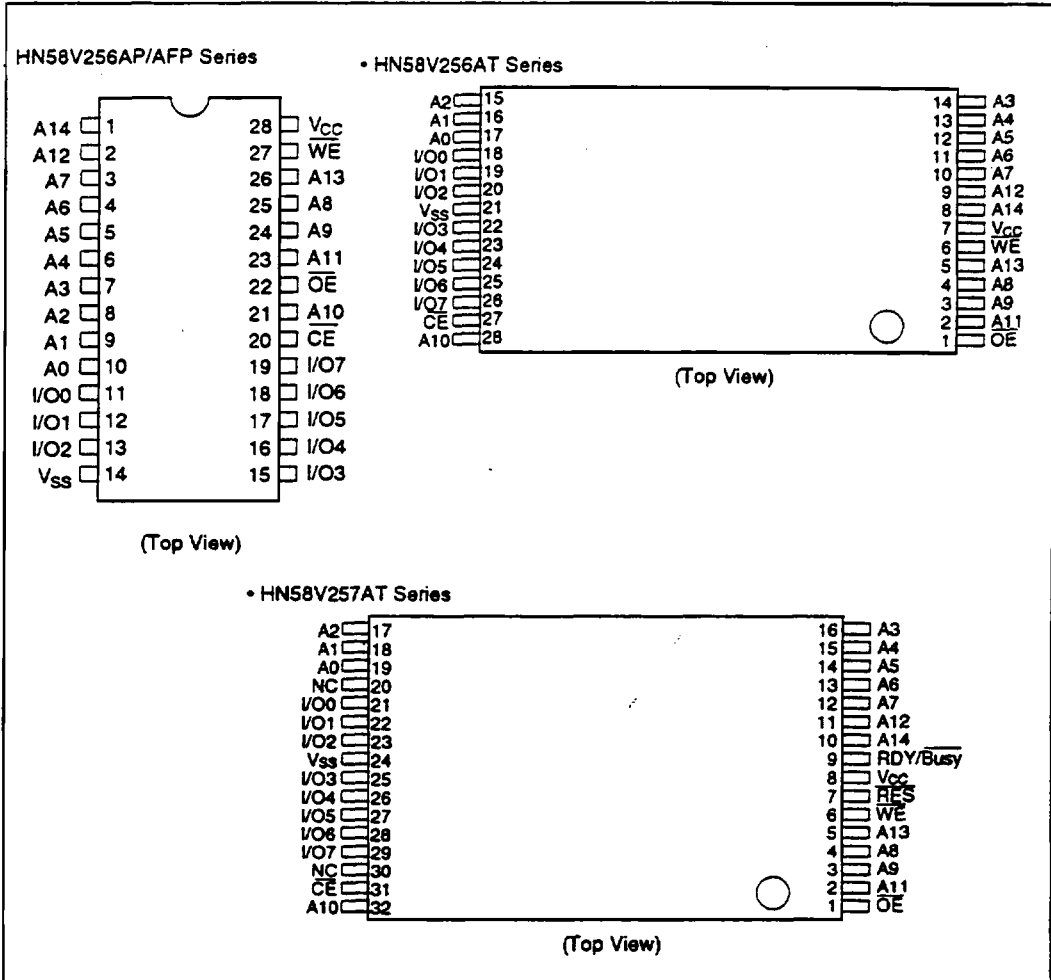
HN58V256A, HN58V257A Series

Ordering Information

Type No.	Operating Voltage	Temperature Range	Access Time	Package	Compatible Type No. ¹
HN58V256AP-12/-15	2.7 to 5.5 V	0 to 70°C	120/150 ns	600 mil 28-pin plastic DIP(DP-28)	HN58C256P-20
HN58V256AFP-12/-15	2.7 to 5.5 V	0 to 70°C	120/150 ns	400 mil 28-pin plastic SOP (FP-28D)	HN58C256FP-20
HN58V256AFPI-12/-15	2.7 to 5.5 V	-40 to 85°C			HN58C256FPI-20
HN58V256AT-12/-15	2.7 to 5.5 V	0 to 70°C	120/150 ns	28-pin plastic TSOP (—) ²	
HN58V256AT-12SR /-15SR	2.7 to 5.5 V	-20 to 85°C			
HN58V257AT-12/-15	2.7 to 5.5 V	0 to 70°C	120/150 ns	8 × 14 mm 32-pin plastic TSOP (TFP-32DA)	HN58C257T-20 HN58V257T-35
HN58V257AT-12SR /-15SR	2.7 to 5.5 V	-20 to 85°C			HN58C257T-20SR HN58V257T-35SR

Notes: 1. This type No. can be replaced by the corresponding A-version. (ex. HN58C256P to HN58V256AP)
 2. Package type and dimension are under development.

Pin Arrangement

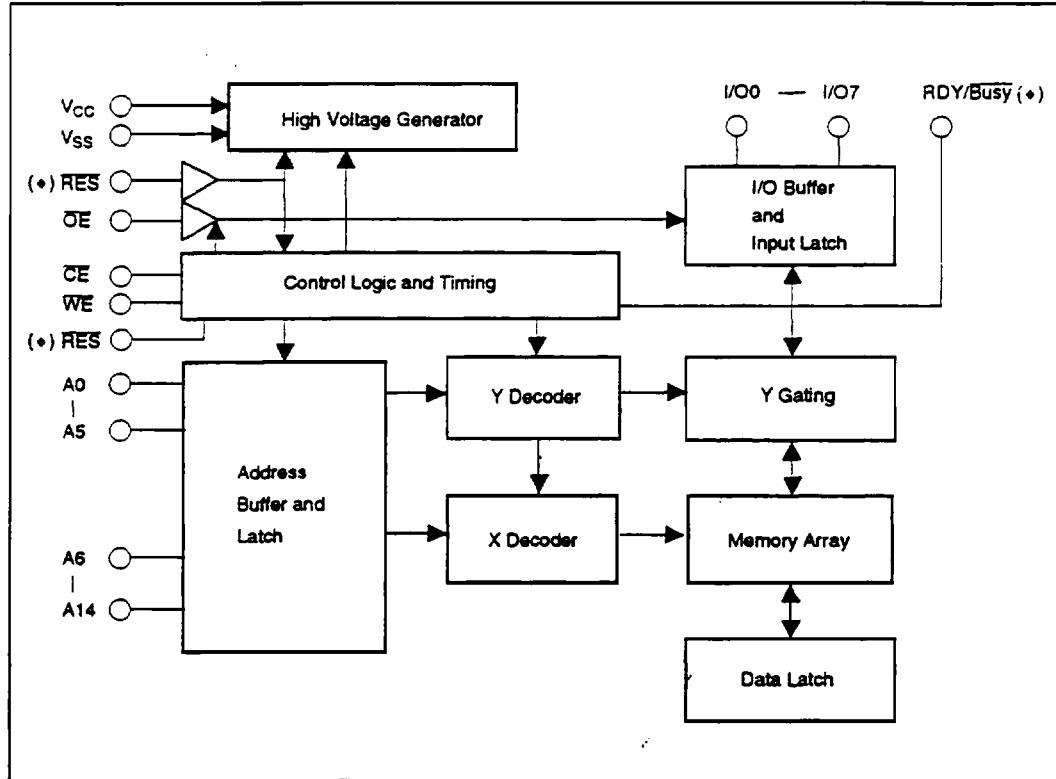


Pin Description

Pin name	Function
A0 to A14	Address
I/O0 to I/O7	Input/output
OE	Output enable
CE	Chip enable

Pin name	Function
WE	Write enable
V _{CC}	Power (+2.7 - 5.5 V)
V _{SS}	Ground
RDY/Busy (♦)	Ready busy
RES (♦)	Reset

Block Diagram



Mode Selection

Pin Mode	CE	OE	WE	RES ^(•)	RDY/Busy ^(•)	I/O
Read	V _{IL}	V _{IL}	V _{IH}	V _H ^{*1}	High-Z	Dout
Standby	V _{IH}	x ^{*2}	x	x	High-Z	High-Z
Write	V _{IL}	V _{IH}	V _{IL}	V _H	High-Z to V _{OL}	Din
Deselect	V _{IL}	V _{IH}	V _{IH}	V _H	High-Z	High-Z
Write Inhibit	x	x	V _{IH}	x	—	—
	x	V _{IL}	x	x	—	—
Data Polling	V _{IL}	V _{IL}	V _{IH}	V _H	V _{OL}	Data out (I/O7)
Program reset	x	x	x	V _{IL}	High-Z	High-Z

Note: 1. Refer to the recommended DC operating condition.
2. x : Don't care

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Device Group ^{*4}
Supply voltage ^{*1}	V _{CC}	-0.6 to +7.0	V	A, B, C
Input voltage ^{*1}	V _{in}	-0.5 ^{*2} to +7.0	V	A, B, C
Operating temperature range ^{*3}	T _{opr}	0 to +70	°C	A
		-20 to 85	°C	B
		-40 to 85	°C	C
Storage temperature range	T _{stg}	-55 to +125	°C	A, B, C

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Device Group ^{*4}
Supply voltage	V _{CC}	2.7	3.0	5.5	V	A, B, C
Input voltage	V _{IL}	-0.3 ^{*5}	—	0.6	V	A, B, C
	V _{IH}	2.4 ^{*6}	—	V _{CC} + 0.3 ^{*7}	V	A, B, C
	V _H (*)	V _{CC} - 0.5	—	V _{CC} + 1.0	V	A, B, C
Operating temperature	T _{opr}	0	—	70	°C	A
		-20	—	85	°C	B
		-40	—	85	°C	C

- Notes:
1. With respect to V_{SS}.
 2. V_{in} min : -3.0 V for pulse width ≤ 50 ns.
 3. Including electrical characteristics and data retention.
 4. Group A includes HN58V256AP/AFP, HN58V257AT and HN58V256AT.
Group B includes HN58V256AT-SR and HN58V257AT-SR.
Group C includes HN58V256AFPI.
 5. V_{IL} min: -1.0 V for pulse width ≤ 50 ns.
 6. V_{IH} min for V_{CC} = 3.6 to 5.5 V is 3.0 V.
 7. V_{IH} max: V_{CC} + 1.0 V for pulse width ≤ 50 ns.

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DC Characteristics

Supply voltage range (V_{CC}), temperature range (T_{opr}) and input voltage ($V_{IH}/V_{IL}/V_H$) are referred to the table of Recommended DC Operating Conditions.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2 ¹	μA	$V_{CC} = 5.5 V$, $V_{in} = 5.5 V$
Output leakage current	I_{LO}	—	—	2	μA	$V_{CC} = 5.5 V$, $V_{out} = 5.5/0.4 V$
VCC current (standby)	I_{CC1}	—	—	20	μA	$\overline{CE} = V_{CC}$
	I_{CC2}	—	—	1	mA	$\overline{CE} = V_{IH}$
VCC current (active)	I_{CC3}	—	—	8	mA	$I_{out} = 0 mA$, Duty = 100%, Cycle = 1 μs at $V_{CC} = 3.6 V$
	—	—	—	12	mA	$I_{out} = 0 mA$, Duty = 100%, Cycle = 1 μs at $V_{CC} = 5.5 V$
	—	—	—	20	mA	$I_{out} = 0 mA$, Duty = 100%, Cycle = 120 ns at $V_{CC} = 3.6 V$
	—	—	—	30	mA	$I_{out} = 0 mA$, Duty = 100%, Cycle = 120 ns at $V_{CC} = 5.5 V$
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2.1 mA$
Output high voltage	V_{OH}	$V_{CC} \times 0.8$	—	—	V	$I_{OH} = -400 \mu A$

Note: 1. I_{LI} on RES : 100 μA max (♦)

Capacitance ($T_a = 25^\circ C$, $f = 1 MHz$)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	C_{in}^{*1}	—	—	6	pF	$V_{in} = 0 V$
Output capacitance	C_{out}^{*1}	—	—	12	pF	$V_{out} = 0 V$

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics

Supply voltage (V_{CC}) and temperature range (T_{opr}) are referred to the table of 'Recommended DC Operating Conditions'.

Test Conditions

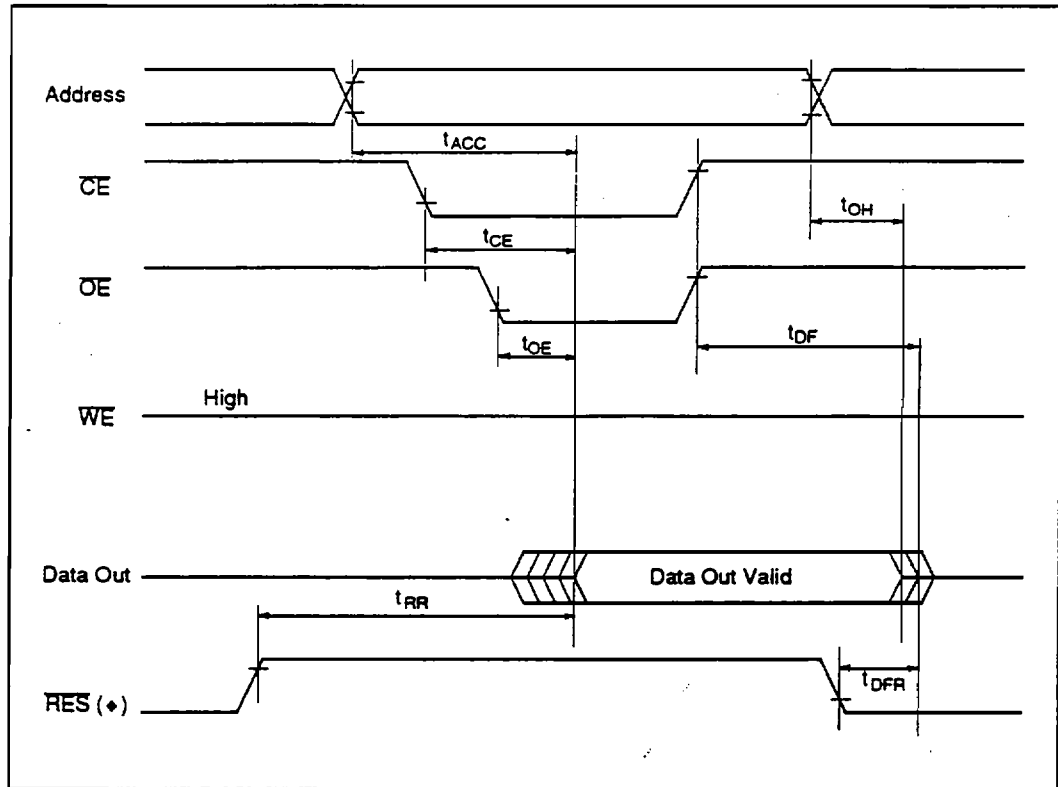
- Input pulse levels : 0 V to 3.0 V
0 V to V_{CC} ($\overline{RES}$ pin)
- Input rise and fall time : ≤ 20 ns
- Input timing reference levels : 0.8, 1.8 V
- Output load : 1TTL Gate +100 pF
- Output reference levels : 1.5 V, 1.5 V

Read Cycle

Parameter	Symbol	-12		-15		Unit	Test conditions
		Min	Max	Min	Max		
Address to output delay	t_{ACC}	—	120	—	150	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{CE}$ to output delay	t_{CE}	—	120	—	150	ns	$\overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{OE}$ to output delay	t_{OE}	10	60	10	60	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$
Address to output hold	t_{OH}	0	—	0	—	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{OE}$ ($\overline{CE}$) high to output float*1	t_{DF}	0	40	0	40	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{RES}$ low to output float*1(♦)	t_{DFR}	0	350	0	350	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
$\overline{RES}$ to output delay(♦)	t_{RR}	0	600	0	600	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$

Note: 1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.

Read Timing Waveform



HN58V256A, HN58V257A Series

Write Cycle

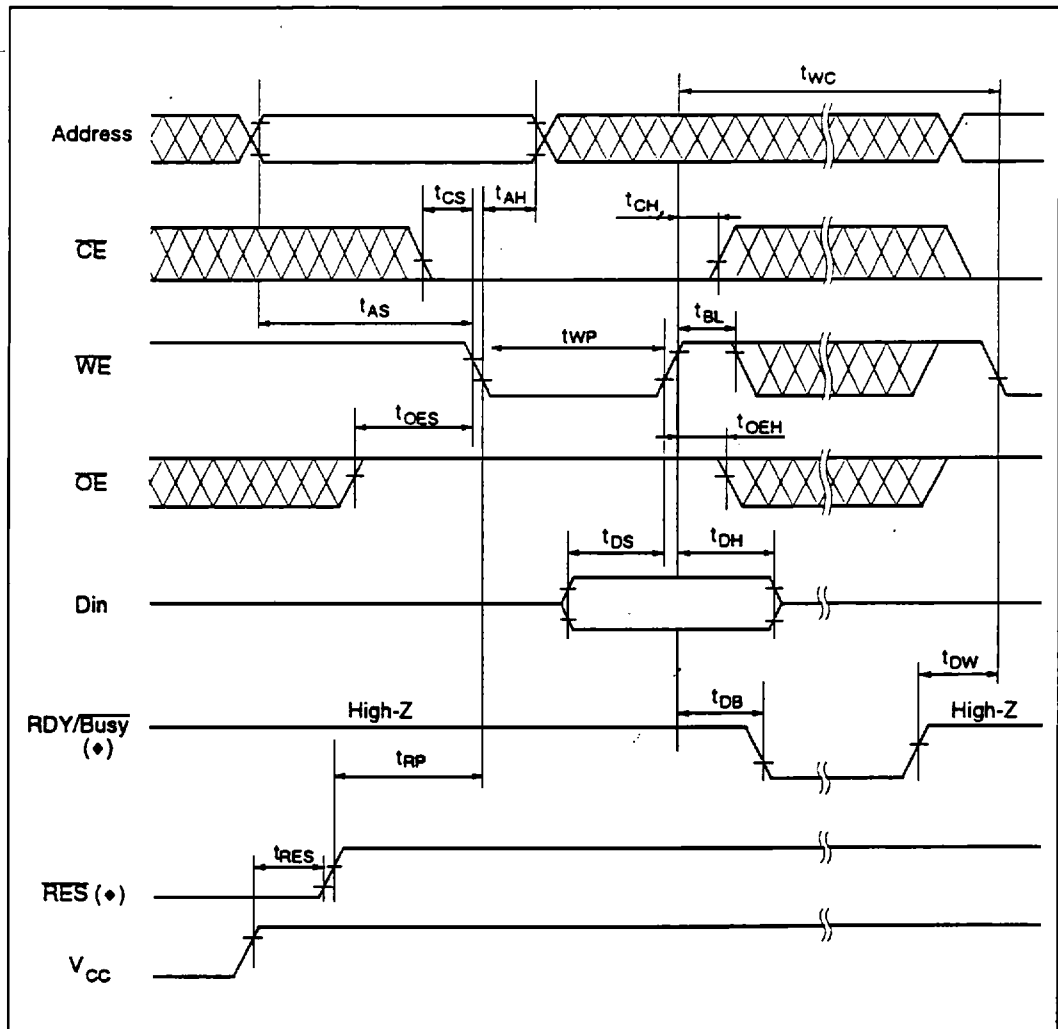
Parameter	Symbol	Min*1	Typ	Max	Unit	Test conditions
Address setup time	t _{AS}	0	—	—	ns	
Address hold time	t _{AH}	50	—	—	ns	
CE to write setup time (WE controlled)	t _{CS}	0	—	—	ns	
CE hold time (WE controlled)	t _{CH}	0	—	—	ns	
WE to write setup time (CE controlled)	t _{WS}	0	—	—	ns	
WE hold time (CE controlled)	t _{WH}	0	—	—	ns	
OE to write setup time	t _{OES}	0	—	—	ns	
OE hold time	t _{OEH}	0	—	—	ns	
Data setup time	t _{DS}	50	—	—	ns	
Data hold time	t _{DH}	0	—	—	ns	
WE pulse width (WE controlled)	t _{WP}	200	—	—	ns	
CE pulse width (CE controlled)	t _{CW}	200	—	—	ns	
Data latch time	t _{DL}	100	—	—	ns	
Byte load cycle	t _{BLC}	0.3	—	30	μs	
Byte load window	t _{BL}	100	—	—	μs	
Write cycle time	t _{WC}	—	—	10 ⁻²	ms	
Time to device busy	t _{DB}	120	—	—	ns	
Write start time	t _{DW}	0 ⁻³	—	—	ns	
Reset protect time (♦)	t _{RP}	100	—	—	μs	
Reset high time (♦)	t _{RES}	1	—	—	μs	

Note: 1. Use this device in longer cycle than this value.

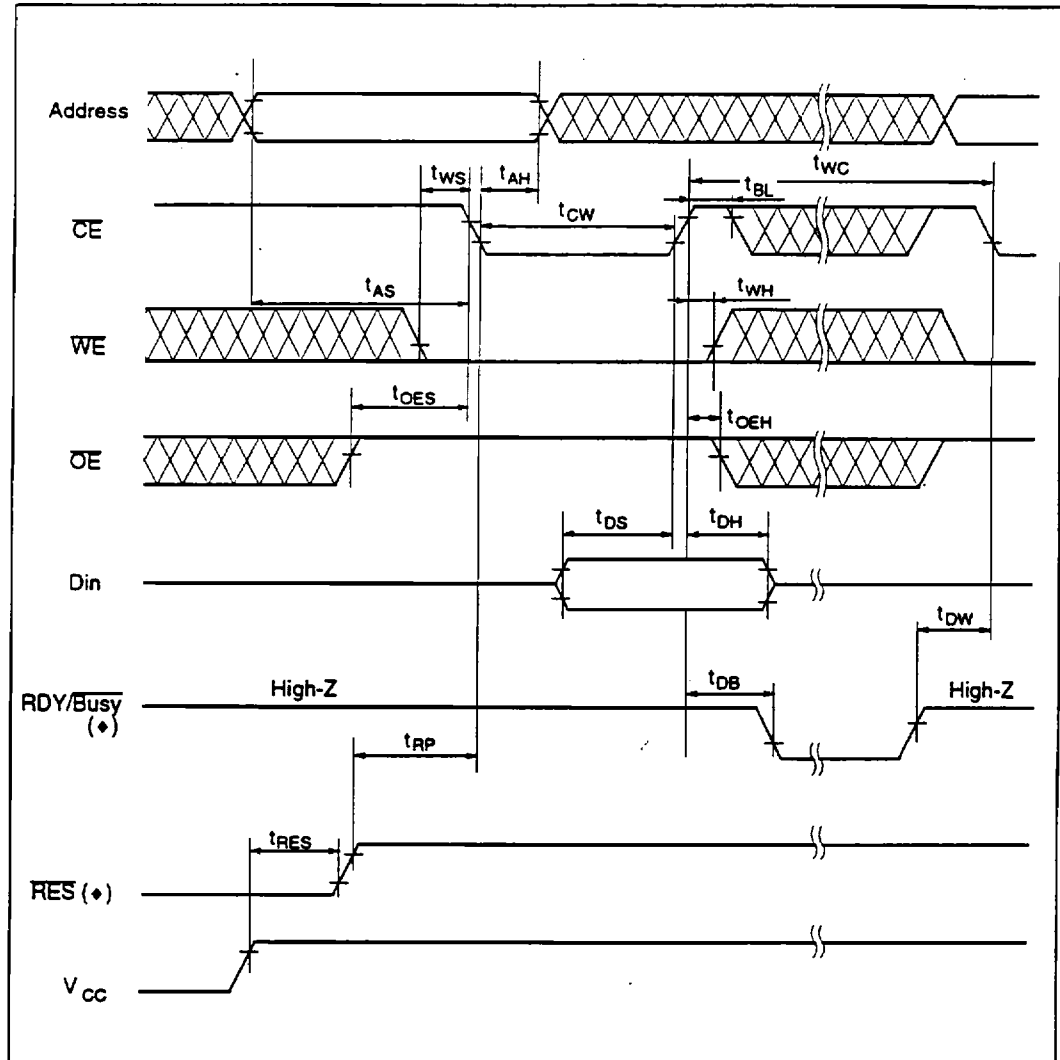
2. t_{WC} must be longer than this value unless polling techniques or RDY/Busy (♦) are used. This device automatically completes the internal write operation within this value.

3. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/Busy (♦) are used.

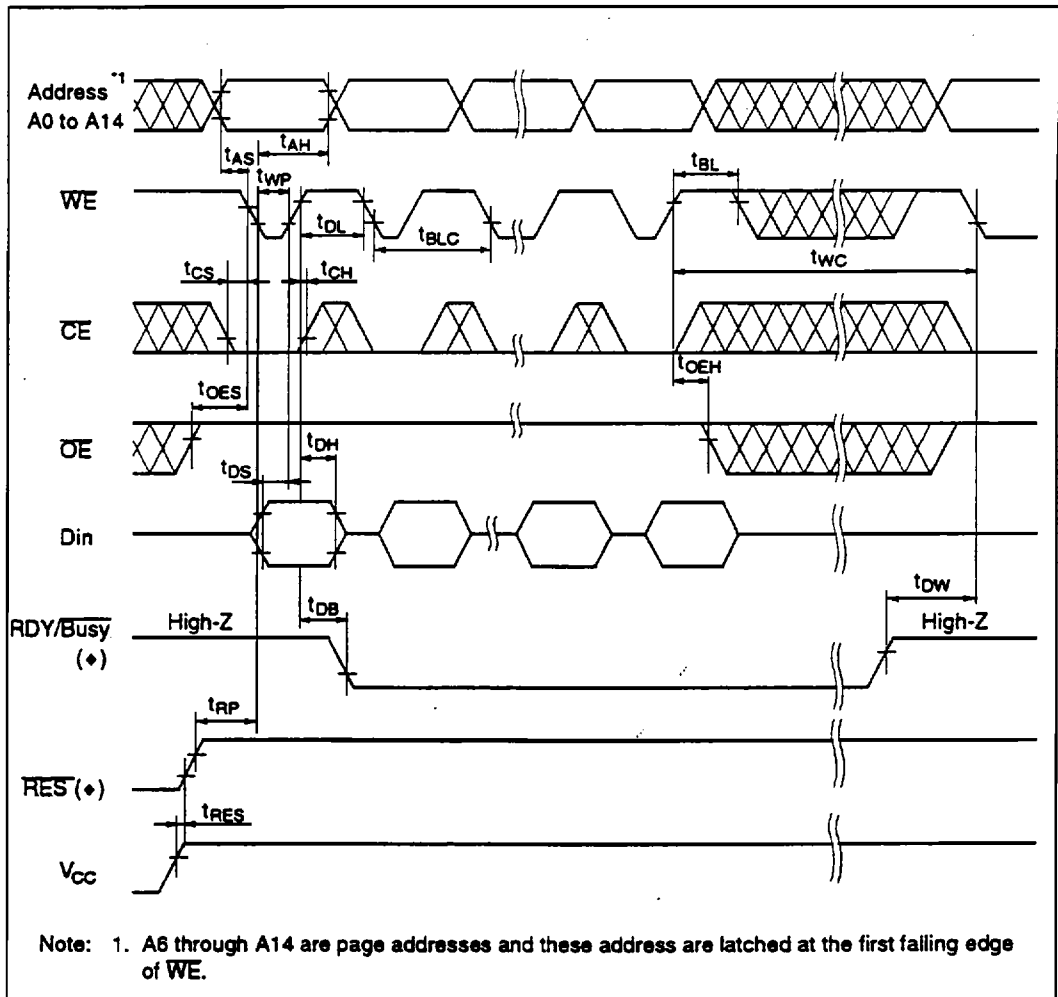
Byte Write Timing Waveform(1) ($\overline{WE}$ Controlled)



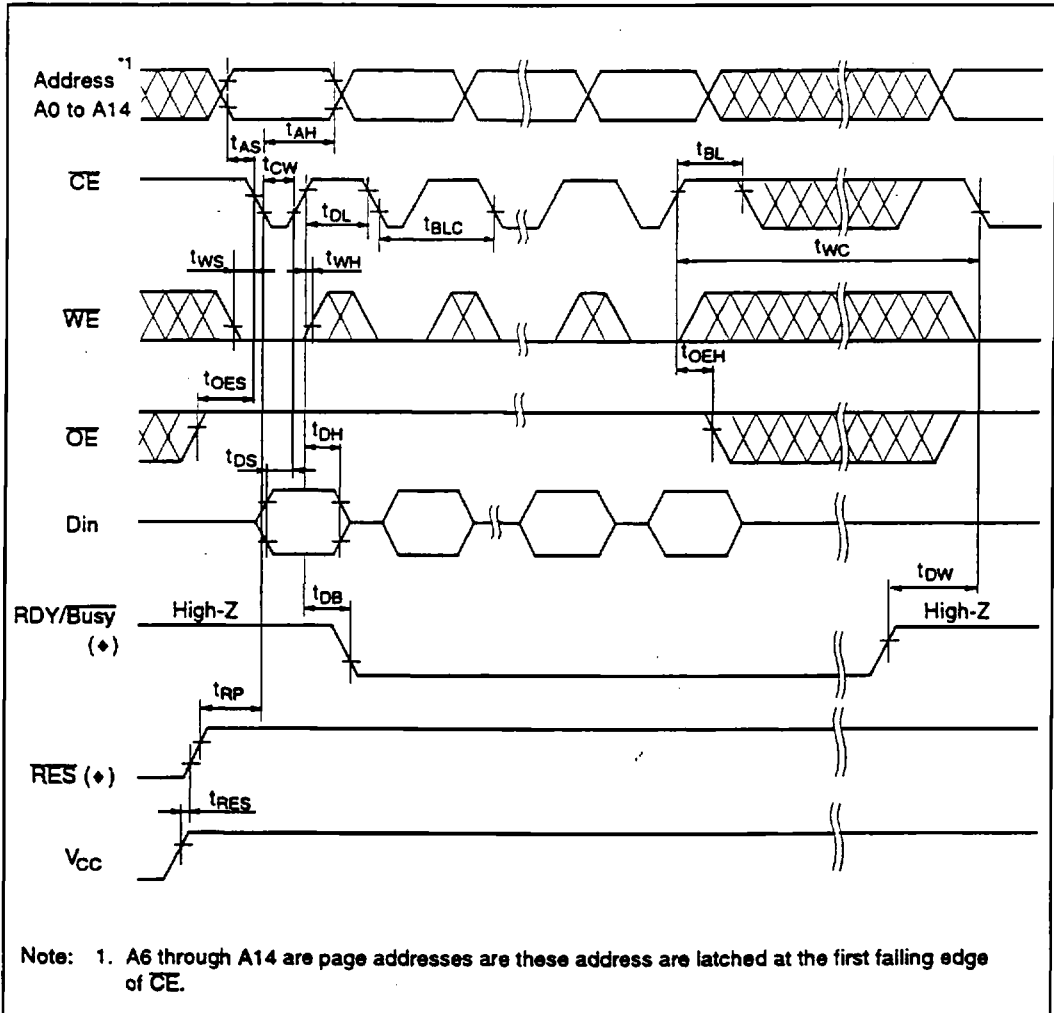
Byte Write Timing Waveform(2) ($\overline{\text{CE}}$ Controlled)



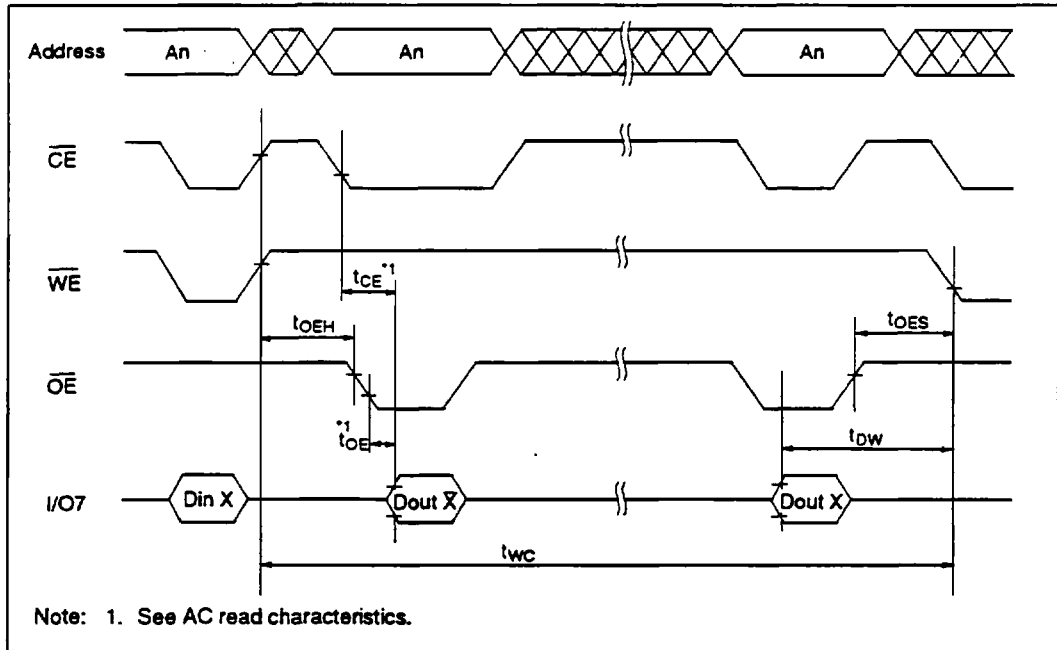
Page Write Timing Waveform(1) (WE Controlled)



Page Write Timing Waveform(2) ($\overline{CE}$ Controlled)



Data Polling Timing Waveform

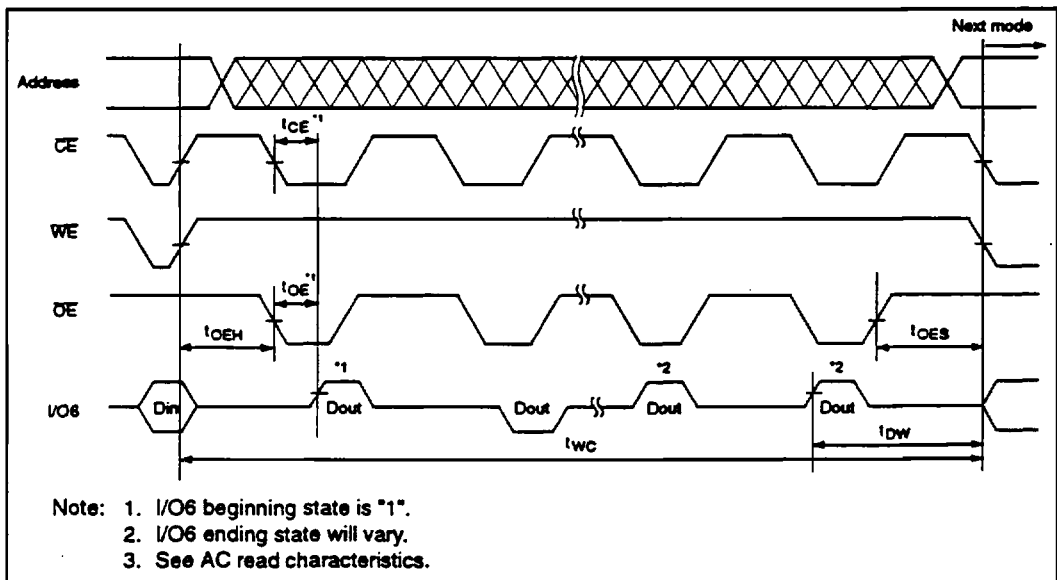


Toggle bit

This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming

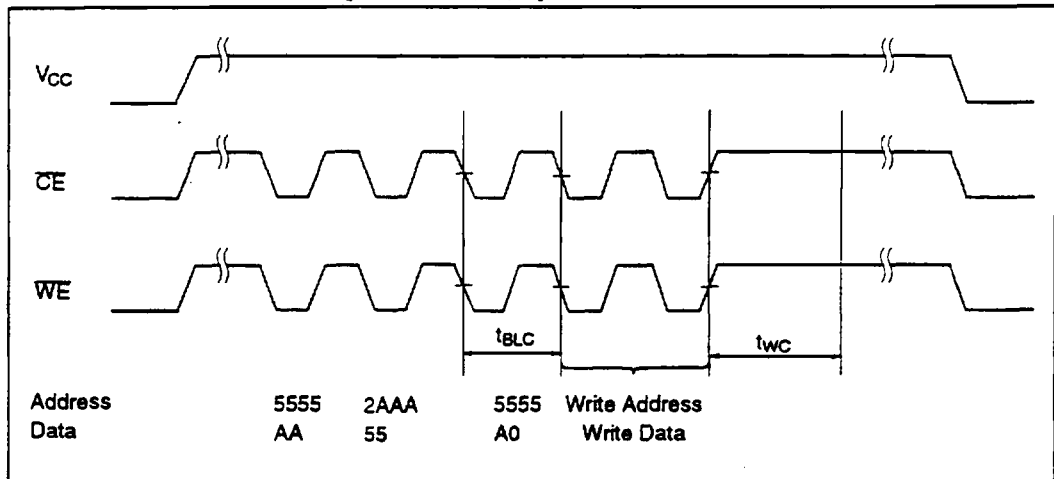
cycle, I/O6 will change from "1" to "0" (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

Toggle bit Waveform

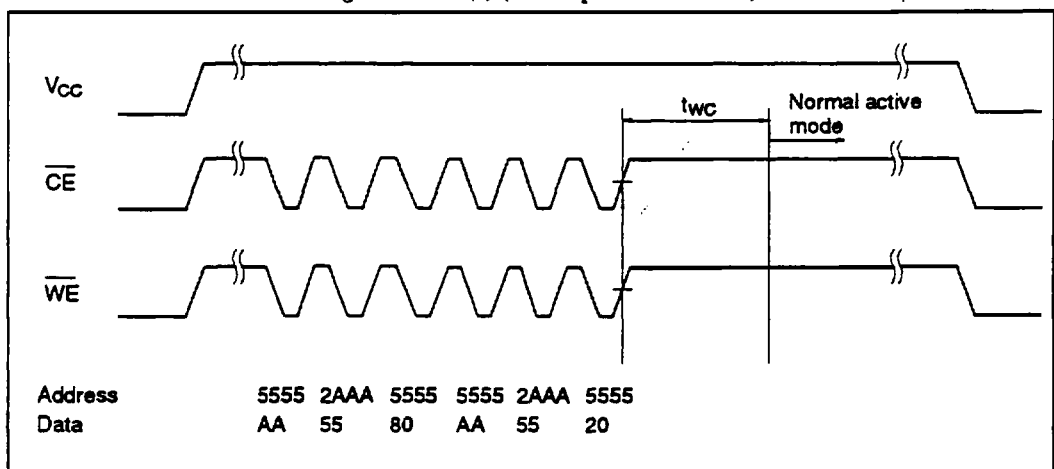


HN58V256A, HN58V257A Series

Software Data Protection Timing Waveform(1) (in protection mode)



Software Data Protection Timing Waveform(2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 μ s from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. When $\overline{CE}$ or $\overline{WE}$ is kept high for 100 μ s after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

Data Polling

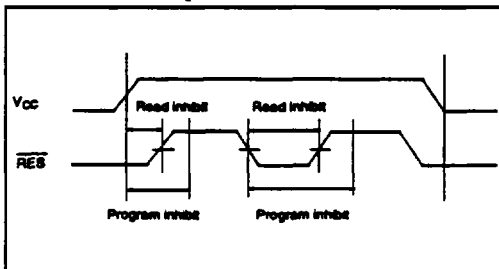
Data polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/Busy Signal (♦)

RDY/Busy signal also allows status of the EEPROM to be determined. The RDY/Busy signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/Busy signal changes state to high impedance.

RES Signal (♦)

When $\overline{RES}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during read and programming because it doesn't provide a latch function.



$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

Write/Erase Endurance and Data Retention Time

The endurance is 10^5 cycles in case of the page programming and 10^4 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

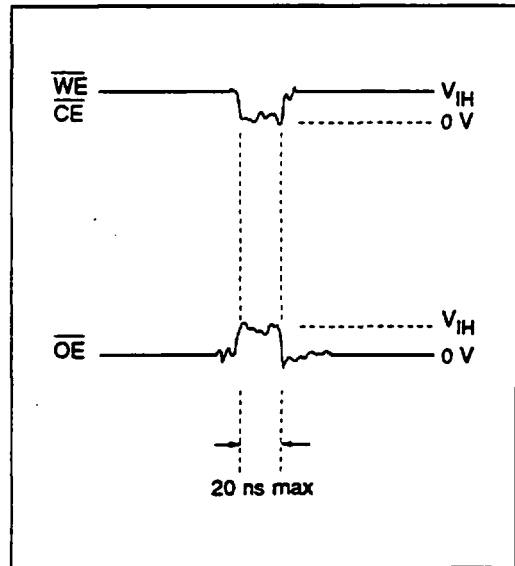
Data Protection

1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.

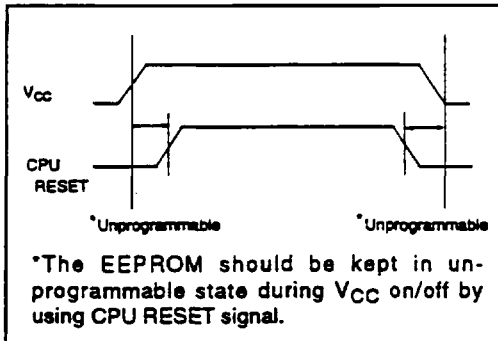
To prevent this phenomenon, this device has a noise cancelation function that cuts noise if its width is 20 ns or less in programming mode.

Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data protection at V_{CC} on/off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.



(1) Protection by $\overline{CE}$, $\overline{OE}$, $\overline{WE}$

To realize the unprogrammable state, the input level of control pins must be held as shown in the table below.

$\overline{CE}$	V_{CC}	x	x
$\overline{OE}$	x	V_{SS}	x
$\overline{WE}$	x	x	V_{CC}

x: Don't care.

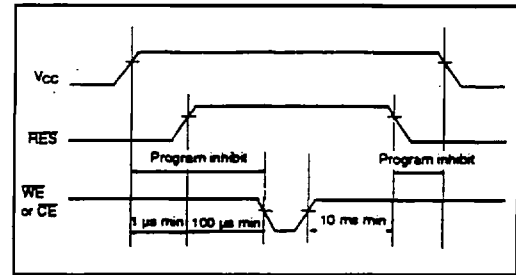
V_{CC} : Pull-up to V_{CC} level.

V_{SS} : Pull-down to V_{SS} level.

(2) Protection by $\overline{RES}$ (♦)

The unprogrammable state can be realized by that the CPU's reset signal inputs directly to the EEPROM's $\overline{RES}$ pin. $\overline{RES}$ should be kept V_{SS} level during V_{CC} on/off.

The EEPROM breaks off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.



3. Software data protection

To prevent unintentional programming caused by noise generated by external circuits, This device has the software data protection function. In software data protection mode, 3 bytes of data must be input before write data as follows. And these bytes can switch the non-protection mode to the protection mode.

Address	Data
5555	AA
↓	↓
2AAA	55
↓	↓
5555	A0
↓	↓
Write address	Write data } Normal data input

Software data protection mode can be canceled by inputting the following 6 bytes. After that, this device turns to the non-protection mode and can write data normally. But when the data is input in the canceling cycle, the data cannot be written.

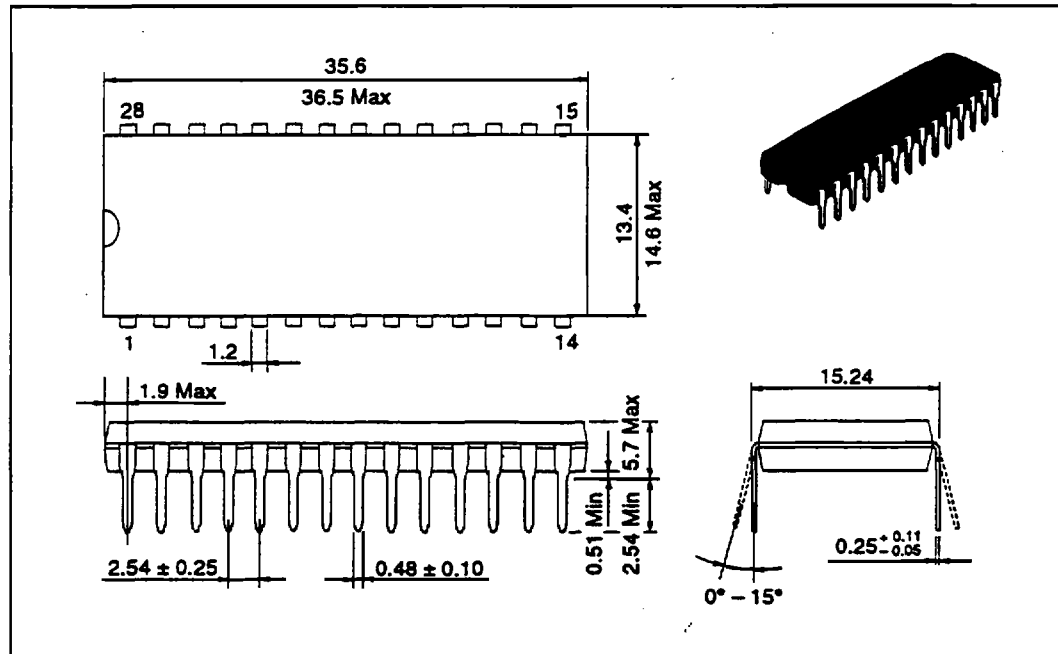
Address	Data
5555	AA
↓	↓
2AAA	55
↓	↓
5555	80
↓	↓
5555	AA
↓	↓
2AAA	55
↓	↓
5555	20

The software data protection is not enabled at the shipment.

Package Dimensions

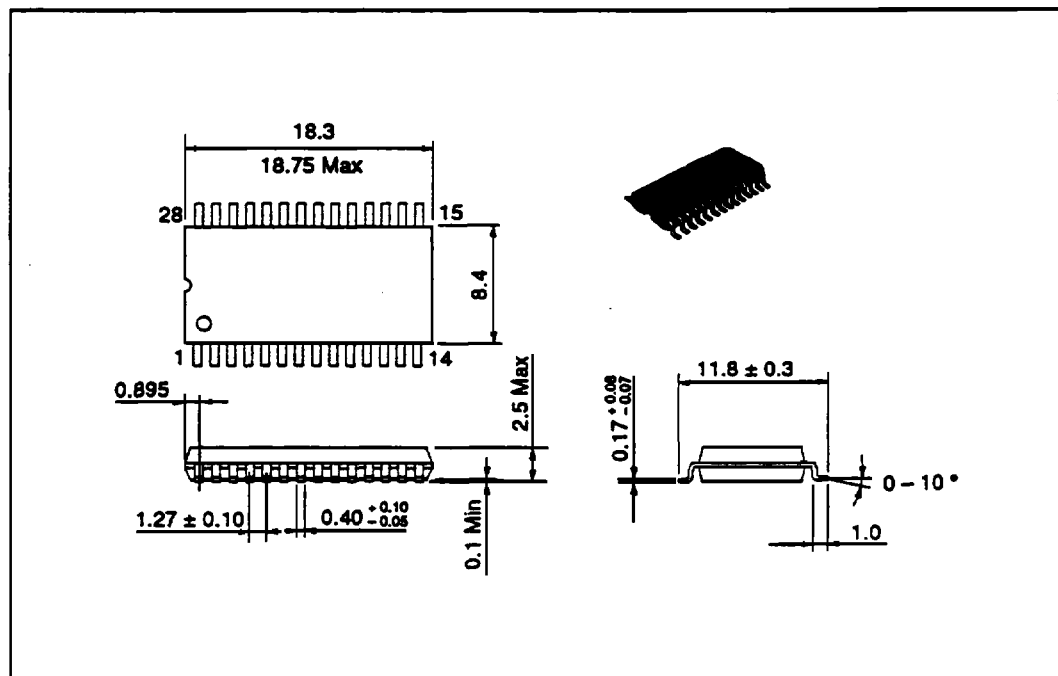
HN58V256AP Series (DP-28)

Unit : mm



HN58V256AFP Series (FP-28D)

Unit : mm

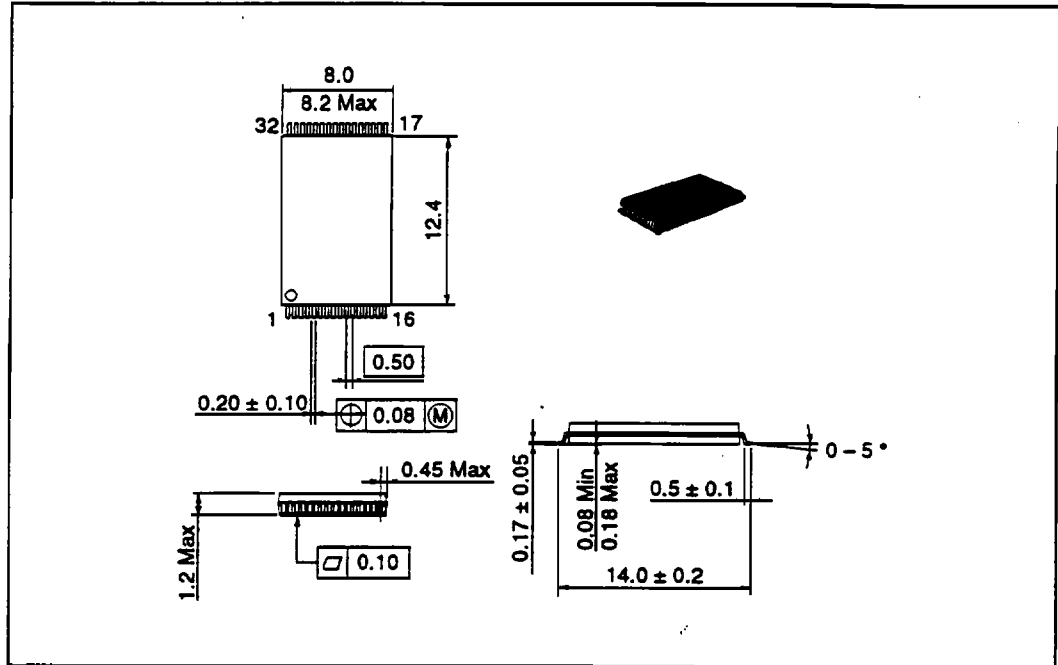


HN58V256A, HN58V257A Series

Package Dimensions

HN58V257AT Series (TFP-32DA)

Unit : mm



HN58V256AT Series (—)

Unit : mm

(To be determined)

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HN58V256A, HN58V257A Series

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Mar. 15, 1995	Initial issue	<i>M. Terasawa</i>	<i>T. Muto</i>

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