HARRIS Semiconductor

COMPLETE DATA SHEET COMING SOON!

CD54HC175F3A, CD54HCT175F3A

June 1997 File Number 3796

Quad D-Type Flip-Flop with Reset

The CD54HC175F3A and CD54HCT175F3A are high-speed quad D-type flip-flops with individual D inputs and Q, $\overline{Q}$ complementary outputs. The devices are fabricated using silicon-gate CMOS technology. They have the low power consumption advantage of standard CMOS ICs and the ability to drive 10 LSTTL devices.

Information at the D input is transferred to the Q and $\overline{Q}$ outputs on the positive-going edge of the clock pulse. All four flip-flops are controlled by a common clock (CP) and a common reset ($\overline{MR}$). Resetting is accomplished by a low voltage level independent of the clock. All four Q outputs are reset to a logic 0 and all four $\overline{Q}$ outputs to a logic 1.

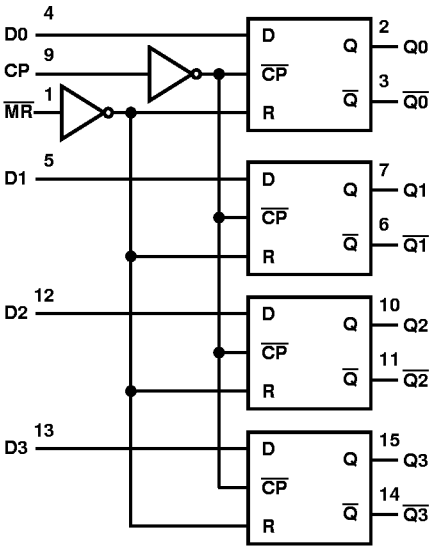
HCT INPUT LOAD TABLE

INPUT	UNIT LOAD (NOTE 1)
$\overline{MR}$	1.0
D	0.15
CP	0.6

NOTE:

1. Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 360µA Max at +25°C.

Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage, V_{CC}
- Voltages Referenced to GND . . . . . -0.5V to +7.0V

DC Input Voltage Range, All Inputs, V_{IN} . . . . . -0.5V to V_{CC} +0.5V

DC Output Voltage Range, All Outputs, V_{OUT} . . -0.5V to V_{CC} +0.5V

DC Input Diode Current, I_{IK}
- For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA

DC Output Diode Current, I_{OK}
- For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA

DC Drain Current, Per Output, I_O, For -0.5V < V_O < V_{CC} + 0.5V
- Standard Output . . . . . ±25mA
- Bus Driver Output . . . . . ±35mA

DC V_{CC} or GND Current, I_{CC}
- Standard Output . . . . . ±50mA
- Bus Driver Output . . . . . ±70mA

Power Dissipation Per Package, P_D
- T_A = -55°C to +100°C (Package F) 500mW
- T_A = +100°C to +125°C (Package F) . . . . . .Derate Linearly at 8mW/°C to 300mW

Operating Temperature Range, T_A
- Package Type F . . . . . -55°C to +125°C

Storage Temperature, T_{STG} . . . . . -65°C to +150°C

Lead Temperature (During Soldering)
- At Distance 1/16in. ± 1/32in. (1.59mm ± 0.79mm)
- From Case For 10s Max . . . . . +265°C
- Unit Inserted Into a PC Board (Min Thickness 1/16in., 1.59mm)
- With Solder Contacting Lead Tips Only . . . . . +300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Supply Voltage Range, V_{CC}
- T_A = Full Package Temperature Range
- CD54HC Types . . . . . 2V to 6V
- CD54HCT Types . . . . . 4.5V to 5.5V

DC Input or Output Voltage, V_{IN}, V_{OUT} . . . . . 0V to V_{CC}

Operating Temperature Range, T_A . . . . . -55°C to +125°C

Input Rise and Fall Times, t_R, t_F
- at 2V . . . . . 0ns to 1000ns
- at 4.5V . . . . . 0ns to 500ns
- at 6V . . . . . 0ns to 400ns

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.