HARRIS

IRF634, IRF635
IRF636, IRF637

N-Channel Power MOSFETs
Avalanche Energy Rated

August 1991

Features

- **8.1A and 6.5A, 250V - 275V**
- **$r_{DS}(on)$ = 0.45Ω and 0.68Ω**
- **Single Pulse Avalanche Energy Rated**
- **SOA is Power-Dissipation Limited**
- **Nanosecond Switching Speeds**
- **Linear Transfer Characteristics**
- **High Input Impedance**
- **275/250V DC Rating - 120V AC Line System Operation**

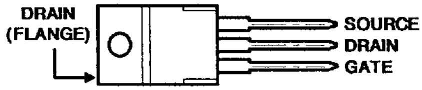
Description

The IRF634, IRF635, IRF636, and IRF637 are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

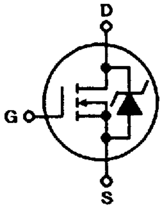
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF634	IRF635	IRF636	IRF637	UNITS
Drain-Source Voltage (1) .... V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) .... V_{DGR}	250	250	275	275	V
Continuous Drain Current					
T_C = +25°C .... I_D	8.1	6.5	8.1	6.5	A
T_C = +100°C .... I_D	5.1	4.1	5.1	4.1	A
Pulsed Drain Current (3) .... I_{DM}	32	26	32	26	A
Gate-Source Voltage .... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C .... P_D	75	75	75	75	W
Linear Derating Factor	0.6	0.6	0.6	0.6	W/°C
Single Pulse Avalanche Energy Rating (4) .... E_{AS}	180	180	180	180	mJ
Operating and Storage Junction Temperature Range .... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) .... T_L	300	300	300	300	°C

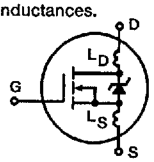
NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width $\leq$ 300μs, Duty Cycle $\leq$ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 4.5mH, R_{GS} = 25Ω, I_{PEAK} = 8.1A. See Figures 14 & 15.

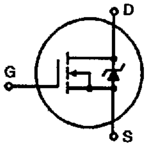
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2168.1**

Electrical Characteristics $T_C = 25^oC$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Drain-Source Breakdown Voltage IRF636, IRF637	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu A$	275	-	-	V
IRF634, IRF635			250	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	$V_{GS} = 20V$	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	$V_{GS} = 20V$	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, $V_{GS} = 0V$	-	-	250	µA
		V_{DS} = Max Rating x 0.8, $V_{GS} = 0V$, $T_J = +125^oC$	-	-	1000	µA
On-State Drain Current (Note 2) IRF634, IRF636	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, $V_{GS} = 10V$	8.1	-	-	A
IRF635, IRF637			6.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF634, IRF636	$r_{DS(ON)}$	$V_{GS} = 10V, I_D = 4.1A$	-	0.32	0.45	Ω
IRF635, IRF637			-	0.48	0.68	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} = 2 \times V_{GS}$ 0V, $I_D = 4.1A$	2.9	4.3	-	S(℧)
Input Capacitance	C_{ISS}	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz$ See Figure 10	-	600	-	pF
Output Capacitance	C_{OSS}		-	180	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	52	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 125V, I_D \simeq 8.1A, R_G = 12\Omega$ See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	9.1	14	ns
Rise Time	t_r		-	23	35	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	31	47	ns
Fall Time	t_f		-	19	29	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	$V_{GS} = 10V, I_D = 8.1A, V_{DS} = 0.8$ Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	24	35	nC
Gate-Source Charge	Q_{gs}		-	5.1	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	12	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.5	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	80	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	8.1	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	32	A
Diode Forward Voltage (Note 2)	V_{SD}	$T_J = +25^oC, I_S = 8.1A, V_{GS} = 0V$	-	-	2.0	V
Reverse Recovery Time	t_{rr}	$T_J = +25^oC, I_F = 8.1A, dI_F/dt = 100A/\mu s$	92	180	390	ns
Reverse Recovered Charge	Q_{RR}	$T_J = +25^oC, I_F = 8.1A, dI_F/dt = 100A/\mu s$	0.63	1.3	2.7	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES:
1. $T_J = +25^oC$ to $+150^oC$
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
3. *Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)*
4. $V_{DD} = 50V$, Start $T_J = +25^oC$, $L = 4.5mH$, $R_{GS} = 25\Omega$, $I_{PEAK} = 8.1A$ (See Figures 14 & 15)

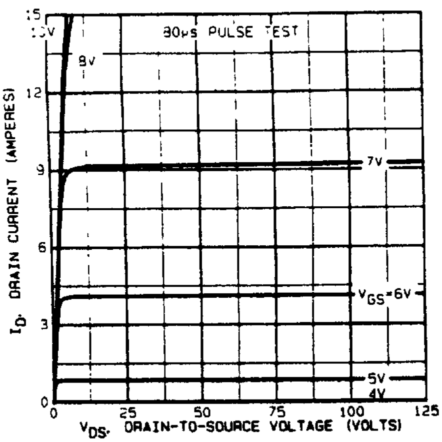


Fig. 1 — Typical Output Characteristics

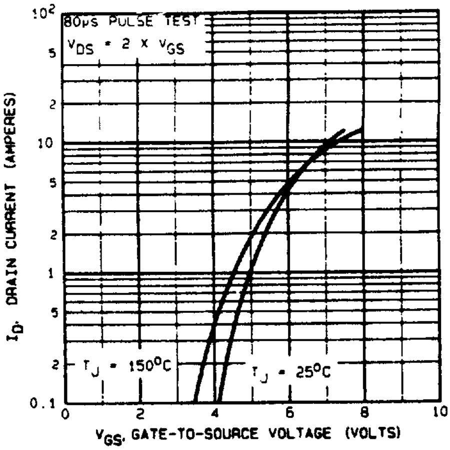


Fig. 2 — Typical Transfer Characteristics

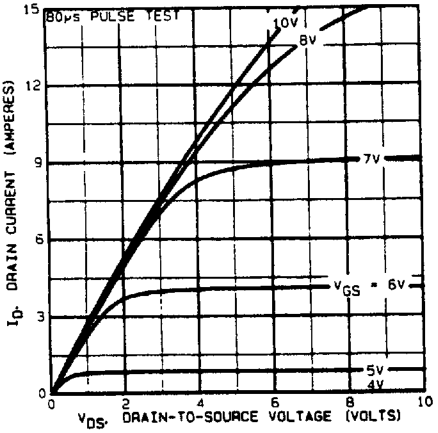


Fig. 3 — Typical Saturation Characteristics

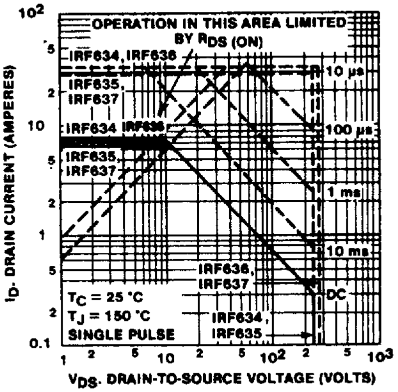


Fig. 4 — Maximum Safe Operating Area

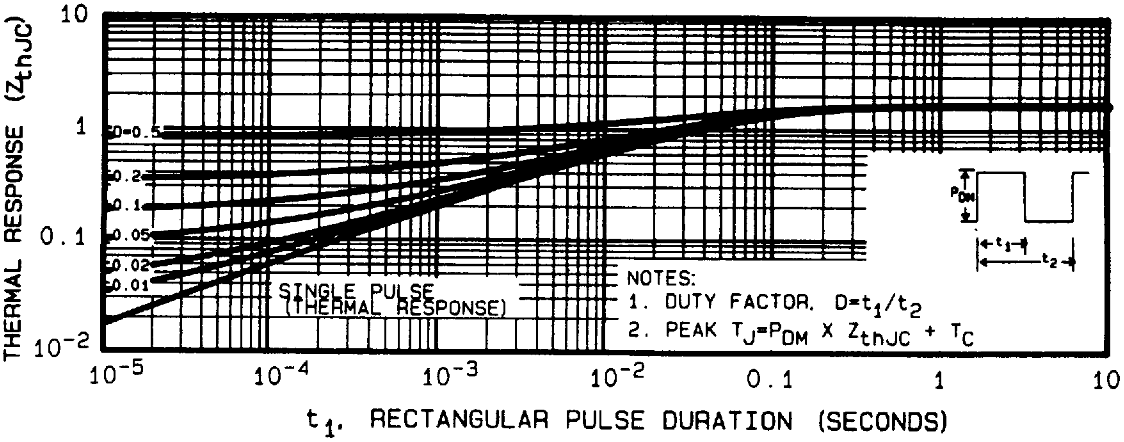


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

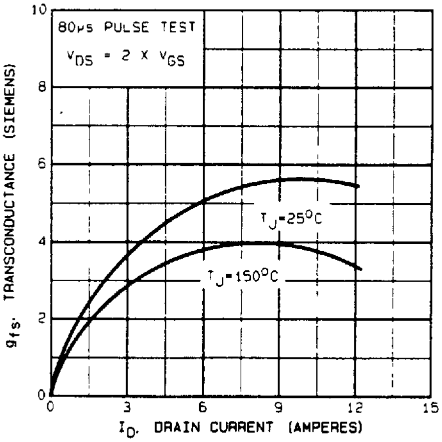


Fig. 6 — Typical Transconductance Vs. Drain Current

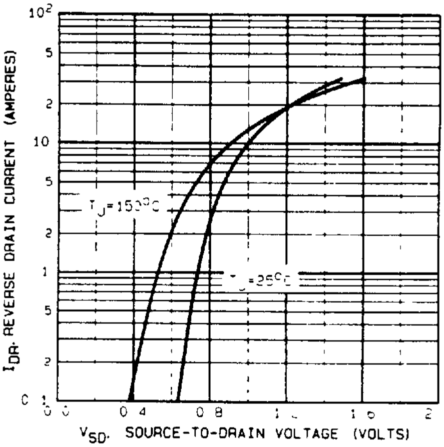


Fig. 7 — Typical Source-Drain Diode Forward Voltage

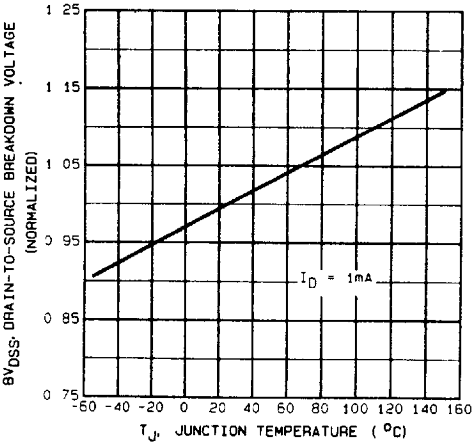


Fig. 8 — Breakdown Voltage Vs. Temperature

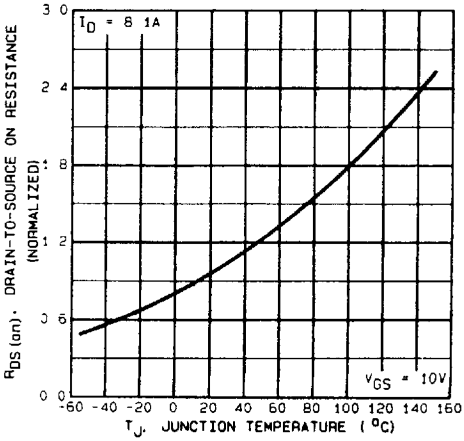


Fig. 9 — Normalized On-Resistance Vs. Temperature

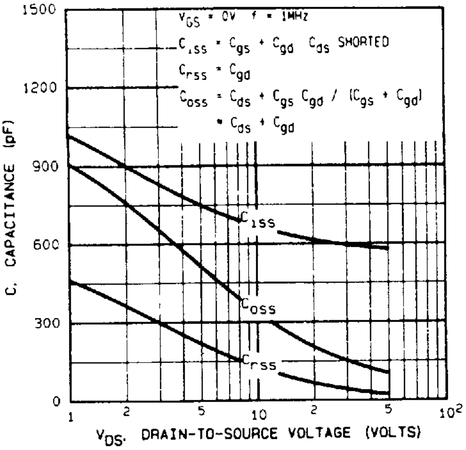


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

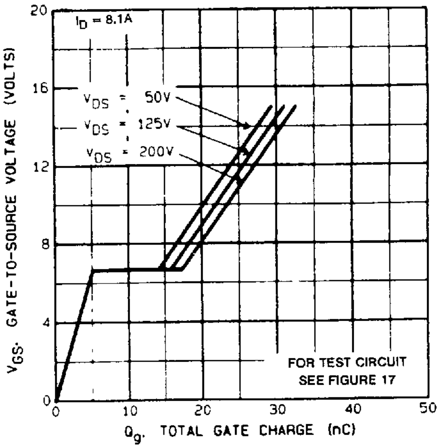


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

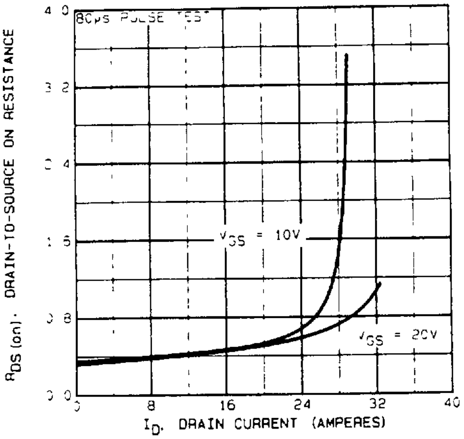


Fig. 12 — Typical On-Resistance Vs. Drain Current

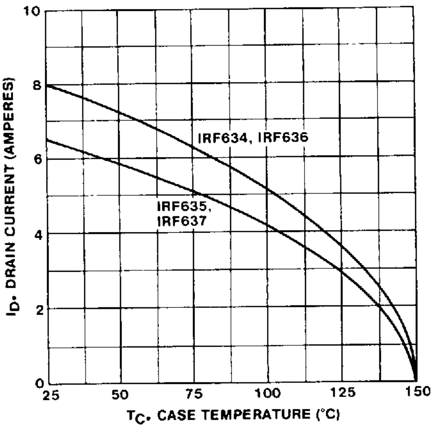


Fig. 13 — Maximum Drain Current Vs. Case Temperature

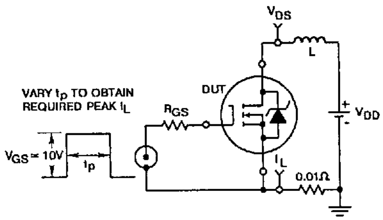


Fig. 14 — Unclamped Energy Test Circuit

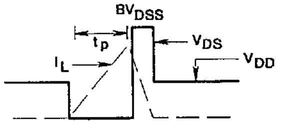


Fig. 15 — Unclamped Energy Waveforms

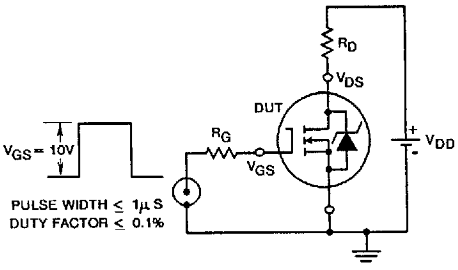


Fig. 16 — Switching Time Test Circuit

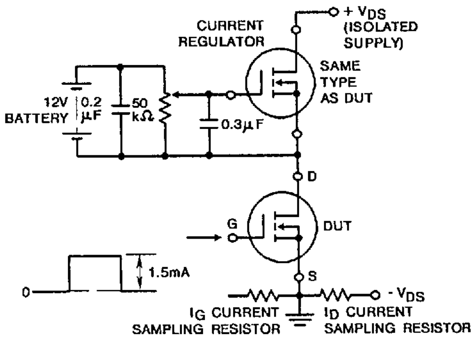


Fig. 17 — Gate Charge Test Circuit