

# OKI Semiconductor

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## MSM6882-3/6882-5

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2400/1200 bps Single Chip MSK Modem

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### GENERAL DESCRIPTION

The MSM6882-3/6882-5 is a single chip MSK (Minimum Shift Keying) modem which is fabricated by Oki's low power consumption CMOS silicon gate technology.

The demodulator receives the data to be transmitted (SD) synchronized with the transmit timing clock (ST) generated by the on-chip clock generator. The signal, which is modulated by MSK method, is output.

The demodulator converts the received MSK signal to the received data (RD) by means of a delay detection technique after limiting the band of the received MSK signal. This signal is input to the digital PLL and the re-generated timing clock (RT) is output from the demodulator, synchronized with the RD.

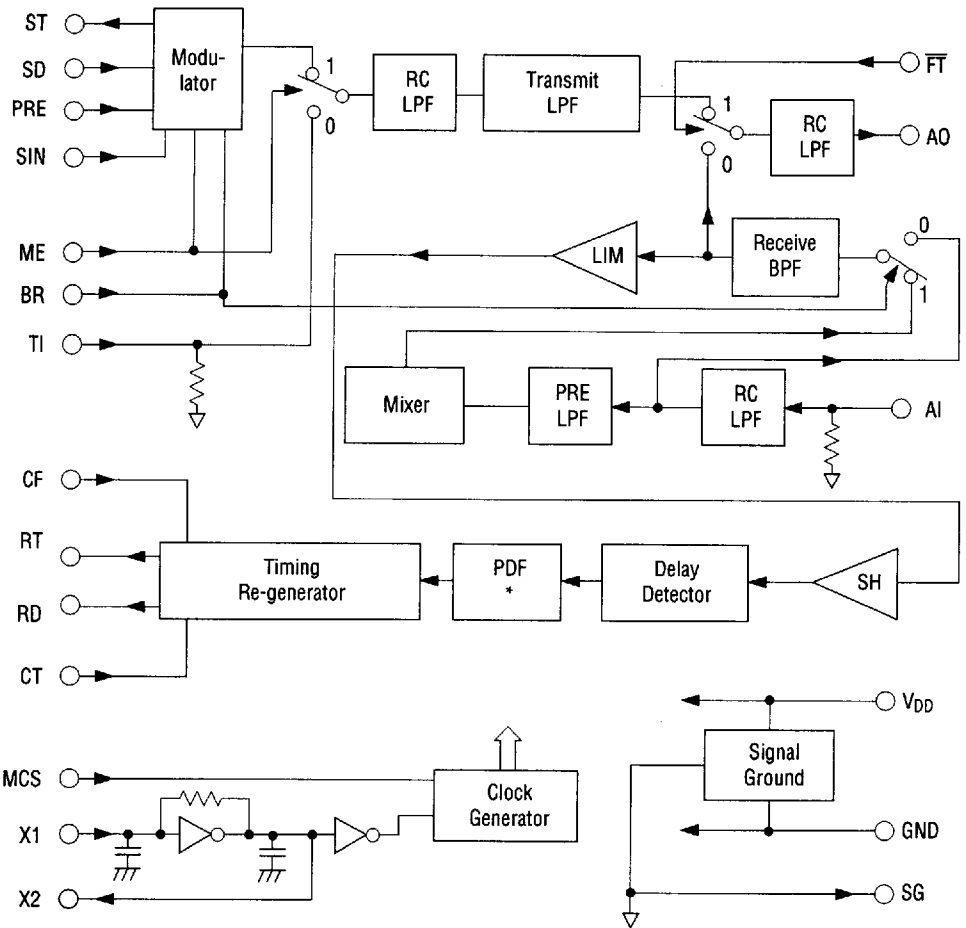
### FEATURES

- Signal power supply: +3.6 V (MSM6882-3)  
+5 V (MSM6882-5)
- On-chip SCF (Switched Capacitor Filter)
- The transmit filter can be also used as voice splatter filter.
- The receive timing re-generator has two different lock-in time performance options to be chosen from.
- Bit rate 2400/1200 bps
- CCIR Rec. 623
- The modulation method can be selected from COS-FFSK and SIN-FFSK.
- Built-in crystal oscillation circuit.
- Package options:

22-pin plastic DIP	(DIP22-P-400)	(Product name: MSM6882-3RS)
		(Product name: MSM6882-5RS)
24-pin plastic SOP	(SOP24-P-430-VK)	(Product name: MSM6882-3GS-VK)
		(Product name: MSM6882-5GS-VK)

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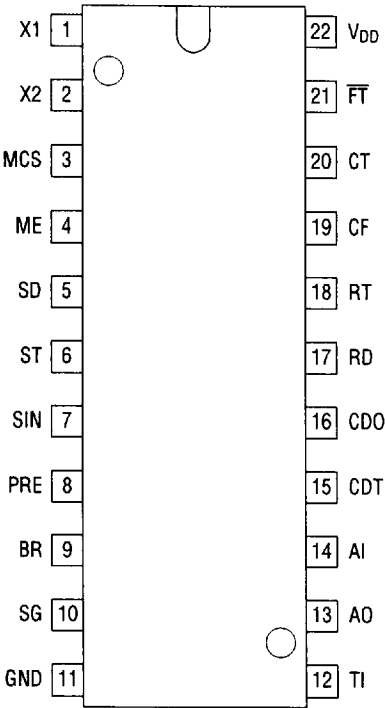
# BLOCK DIAGRAM



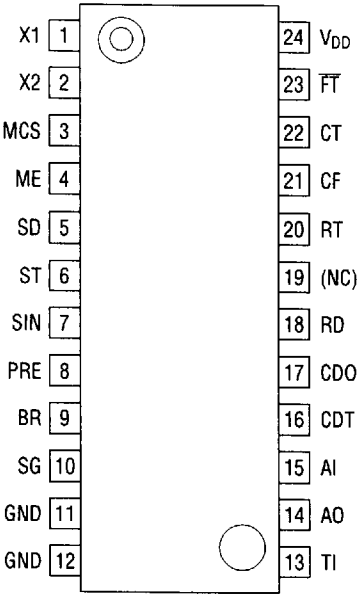
\* Post Detection Filter

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PIN CONFIGURATION (TOP VIEW)



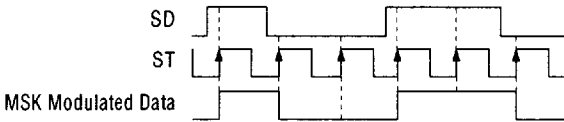
22-Pin Plastic DIP

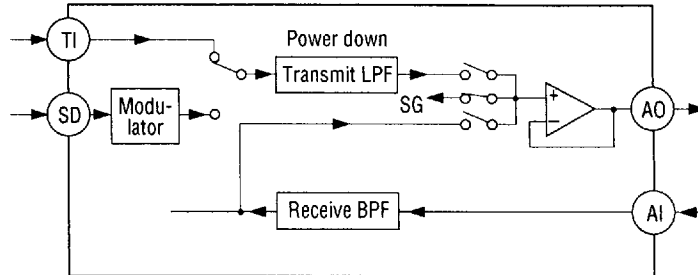


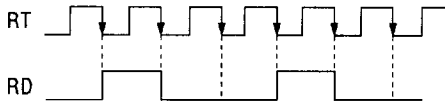
24-Pin Plastic SOP

NC : No connect pin

PIN DESCRIPTION

Name	Description																					
X1	Crystal connection pins. A 3.6864 MHz or a 7.3728 MHz crystal shall be connected.																					
X2	When an external clock is applied for MSM6882's oscillation source, it has to be input to X2. In this case, X2 has to be AC-compled by the capacitor of 200 pF. X1 shall be left open.																					
MCS	Master clock selection. <table><tr><td>MCS</td><td>Crystal or External Clock</td></tr><tr><td>0</td><td>3.6864 MHz</td></tr><tr><td>1</td><td>7.3728 MHz</td></tr></table>	MCS	Crystal or External Clock	0	3.6864 MHz	1	7.3728 MHz															
MCS	Crystal or External Clock																					
0	3.6864 MHz																					
1	7.3728 MHz																					
ME	Modulator enable. When a "high" is input on this pin, MSK modulator output is connected to the input of transmit LPF. When a "low" is input on this pin, TI is connected to the input of transmit LPF.																					
SD	Send data input. The data on this pin is synchronized with the positive edge of ST and input to MSK modulator as an actual transmit data. <div></div>																					
ST	This timing signal is used to latch serial input data on the SD pin. The frequency of ST coincides with the transmission bit rate.																					
SIN	Modulation method selection. Data put on this pin selects either SINE FAST FSK or COSINE FAST FSK. <table><tr><td>Data (2400 bps)</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>Sine Fast FSK</td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>Cosine Fast FSK</td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table>	Data (2400 bps)	0	1	0	0	1	1	Sine Fast FSK							Cosine Fast FSK						
Data (2400 bps)	0	1	0	0	1	1																
Sine Fast FSK																						
Cosine Fast FSK																						
PRE	Pre-amble or data transmission selection. When a "low" is input on this pin, the data put on the SD pin is output on the AO pin. When a "high" is input on this pin, the data put on the SD pin is neglected and pre-amble data is output. Data put on PRE is latched on the rising edge of ST. Pre-amble means to modulate as 010101...pattern.																					

Name	Description																																				
BR	Baud rate selection.																																				
	<table><tr><th rowspan="2">Master Clock (MHz)</th><th rowspan="2">MCS</th><th rowspan="2">BR</th><th rowspan="2">Bit Rate (bps)</th><th colspan="2">Carrier Freq. (Hz)</th></tr><tr><th>Mark</th><th>Space</th></tr><tr><td rowspan="2">7.3728</td><td>1</td><td>1</td><td>2400</td><td>1200</td><td>2400</td></tr><tr><td>1</td><td>0</td><td>1200</td><td>1200</td><td>1800</td></tr><tr><td>3.6864</td><td>0</td><td>0</td><td>1200</td><td>1200</td><td>1800</td></tr><tr><td rowspan="2">3.6864</td><td>1</td><td>1</td><td>1200</td><td>600</td><td>1200</td></tr><tr><td>1</td><td>0</td><td>600</td><td>600</td><td>900</td></tr></table>	Master Clock (MHz)	MCS	BR	Bit Rate (bps)	Carrier Freq. (Hz)		Mark	Space	7.3728	1	1	2400	1200	2400	1	0	1200	1200	1800	3.6864	0	0	1200	1200	1800	3.6864	1	1	1200	600	1200	1	0	600	600	900
	Master Clock (MHz)					MCS	BR	Bit Rate (bps)	Carrier Freq. (Hz)																												
		Mark	Space																																		
	7.3728	1	1	2400	1200	2400																															
		1	0	1200	1200	1800																															
	3.6864	0	0	1200	1200	1800																															
3.6864	1	1	1200	600	1200																																
	1	0	600	600	900																																
SG	Built-in analog signal ground. The DC voltage is approximately half of $V_{DD}$ , so the analog signal interfaces of AI, AO and TI with peripheral circuits which must be implemented by AC-coupling. To make this voltage source impedance lower and ensure the device performance of this device, more than 0.1 $\mu$ F bypass capacitors should be connected from SG to GND and from SG to $V_{DD}$ .																																				
GND	Ground. (0 V)																																				
Ti	Voice signal input. The signal input to this pin can be sent out to AO through the transmit LPF, the characteristics of which, gives the splatter filter for voice band signal. When this function is used, digital "0" must be input to ME. Ti is biased to SG through internal resistor.																																				
AO	Transmit analog signal output. The data put on ME and $\overline{FT}$ can set the status of AO as follows.																																				
	<table><tr><th><math>\overline{FT}</math></th><th>ME</th><th>Transmit LPF</th><th>State of AO</th></tr><tr><td>"1"</td><td>"1"</td><td rowspan="2">Power On</td><td>MSK Signal</td></tr><tr><td>"1"</td><td>"0"</td><td>Voice Signal</td></tr><tr><td>"0"</td><td>"1"</td><td rowspan="2">Power Down</td><td>The Output of Receive BPF</td></tr><tr><td>"0"</td><td>"0"</td><td>No-signal (SG level)</td></tr></table> 	$\overline{FT}$	ME	Transmit LPF	State of AO	"1"	"1"	Power On	MSK Signal	"1"	"0"	Voice Signal	"0"	"1"	Power Down	The Output of Receive BPF	"0"	"0"	No-signal (SG level)																		
$\overline{FT}$	ME	Transmit LPF	State of AO																																		
"1"	"1"	Power On	MSK Signal																																		
"1"	"0"		Voice Signal																																		
"0"	"1"	Power Down	The Output of Receive BPF																																		
"0"	"0"		No-signal (SG level)																																		
The state when $\overline{FT}$ and ME = "0" is shown above. When the input digital data on $\overline{FT}$ changes to "1" from "0", AO remains to be connected to SG during about 2 ms and after that, and AO is switched to transmit LPF. This delay time prevents AO from outputting meaningless signal during transient time from power down to on of LPF.																																					

Name	Description																	
AI	Receive analog signal input. AI is biased internally to SG with about 100 kΩ same as TI.																	
CDT	Device test. This pin should be connected to GND.																	
CDO	Device test. This pin should be opened.																	
RD	Demodulated serial data output. This data is synchronized with the re-generated timing clock RT.																	
RT	Receive data timing clock output. This signal is re-generated by internal digital PLL. Synchronizing to negative edge of RT, RD is output. <div></div>																	
CF	Receive data timing clock is re-generated by digital PLL of which phase correcting speed can be selected with CF. When a digital "1" is put on CF and phase difference between receive data timing and RT is more than 22.5 degree, phase correcting speed is high. In this case, as the phase difference enters within 22.5 degrees, that speed changes to low immediately. When digital "0" is input to CF, phase correcting speed of PLL remains low regardless of the phase difference. Usually, CF is connected to digital "1".																	
CT	PLL's lock-in characteristics can be selected with CT. When digital "1" is put on CT, PLL requires max. 50 bit alternative data pattern. On the other hand, when digital "0" is input to CT, PLL can be locked in below 18 bit data. <div><table><tr><th>CF</th><th>CT</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr><tr><td>1</td><td>0</td><td>—</td><td>—</td><td>18</td><td rowspan="2">bit</td></tr><tr><td>1</td><td>1</td><td>—</td><td>—</td><td>50</td></tr></table></div>	CF	CT	MIN	TYP	MAX	UNIT	1	0	—	—	18	bit	1	1	—	—	50
CF	CT	MIN	TYP	MAX	UNIT													
1	0	—	—	18	bit													
1	1	—	—	50														
FT	Control signal for the internal connection of AO. Refer to column AO. When digital "0" is input to this pin, transmit LPF enters in power down mode, but the output buffer operational amplifier remains active. In this case, AO is at SG level.																	
VDD	Power supply. MSM6882-3: 3.6 V MSM6882-5: 5 V This device is sensitive to supply noises as switched capacitor techniques are utilized. A bypass capacitor of more than 2.2 μF between VDD and GND is indispensable to ensure the performance.																	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V <sub>DD</sub>	Ta = 25°C With respect to GND	-0.3 to 7.0	V
Input Voltage *1	V <sub>I</sub>		-0.3 to V <sub>DD</sub> + 0.3	
Operating Temperature	T <sub>op</sub>	—	-25 to 70	°C
Storage Temperature	T <sub>STG</sub>	—	-55 to 150	

\*1 MCS, ME, SD, SIN, PRE, BR, TI, AI, CDT, CF, CT, FT

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit	
Power Supply Voltage		V <sub>DD</sub>	With respect to GND		*1	3.0	3.6	4.0	V
		*2			4.5	5	5.5		
		GND	—		—	0	—		
Operating Temperature		T <sub>op</sub>	—		−25	25	70	°C	
Crystal Resonant Frequency		f <sub>X</sub> ' <sub>TAL</sub>	MCS = "1"		7.3721	7.3728	7.3735	MHz	
			MCS = "0"		3.6860	3.6864	3.6868		
Data Speed		T <sub>S</sub>	MCS = "1", BR = "1"		—	2400	—	bit/sec	
			BR = "0"		—	1200	—		
C1		—	—		—	2.2	—	μF	
C2		—	—		—	0.1	—		
C3		—	—		—	0.047	—		
C4		—	R <sub>LX</sub> ≥ 40 kΩ		—	0.047	—		
C5		—	—		—	0.047	—		
C6		—	—		—	0.1	—		
Crystal	Oscillation Frequency	—	—		—	7.3728	—	MHz	
	Frequency Deviation	—	25 ±5°C		−100	—	+100	ppm	
	Temperature Characteristics	—	At −30°C to +70°C		−100	—	+100		
	Equivalent Series Resistance	—	—		—	—	50	Ω	
	Load Capacitance	—	—		—	16	—	pF	
Crystal	Oscillation Frequency	—	—		—	3.6864	—	MHz	
	Frequency Deviation	—	25 ±5°C		−100	—	+100	ppm	
	Temperature Characteristics	—	At −30°C to +70°C		−100	—	+100		
	Equivalent Series Resistance	—	—		—	—	100	Ω	
	Load Capacitance	—	—		—	16	—	pF	

\*1 MSM6882-3

\*2 MSM6882-5

ELECTRICAL CHARACTERISTICS

DC Characteristics

(MSM6882-3:  $V_{DD} = 3\text{ V to }4\text{ V}$ ,  $T_a = -25^{\circ}\text{C to }70^{\circ}\text{C}$ )  
(MSM6882-5:  $V_{DD} = 5\text{ V} \pm 0.5\text{ V}$ ,  $T_a = -25^{\circ}\text{C to }70^{\circ}\text{C}$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current *1	I <sub>DD</sub>	Normal Operating Mode FT = "1"	—	4	8	mA
			—	5.5	11	
	I <sub>DDs</sub>	Power Down Mode FT = "0"	—	3.5	7	
			—	5.0	10	
Input Leakage Current *2	I <sub>IL</sub>	V <sub>IN</sub> = 0 V	−10	—	10	μA
	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>DD</sub>	−10	—	10	
Input Voltage *2	V <sub>IL</sub>	*1	0	—	0.6	V
					0.8	
	V <sub>IH</sub>	*1	1.8	—	V <sub>DD</sub>	
			2.2			
Output Voltage *1 *3	V <sub>OL1</sub>	I <sub>OL</sub> = 10 μA/1.6 mA	0	—	0.3	
					0.4	
	V <sub>OH1</sub>	I <sub>OH</sub> = 10 μA/400 μA	0.8V <sub>DD</sub>	—	V <sub>DD</sub>	

\*1 Upper is specified for the MSM6882-3, lower for the MSM6882-5

\*2 MCS, ME, SD, SIN, PRE, BR, CF, CT,  $\overline{FT}$

\*3 ST, RD, RT

Digital Interface Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Data Set-up Time	$t_S$	See Fig.1	300	—	—	ns
Input Data Hold Time	$t_H$		300	—	—	ns
Output Data Delay Time	$t_D$	See Fig.2	-300	—	300	ns



Analog Interface Characteristics

Transmit signal output (AO)

(MSM6882-3:  $V_{DD} = 3\text{ V to }4\text{ V}$ ,  $T_a = -25^{\circ}\text{C to }70^{\circ}\text{C}$ )  
(MSM6882-5:  $V_{DD} = 5\text{ V} \pm 0.5\text{ V}$ ,  $T_a = -25^{\circ}\text{C to }70^{\circ}\text{C}$ )

Parameter		Symbol	Condition			Min.	Typ.	Max.	Unit
Carrier Frequency	1200 bps	f <sub>M1</sub>	FT = "1"	BR = "0"	SD = "1"	1199	1200	1201	Hz
		f <sub>S1</sub>			SD = "0"	1799	1800	1801	
	2400 bps	f <sub>M2</sub>	ME = "1"	BR = "1"	SD = "1"	1199	1200	1201	
		f <sub>S2</sub>			SD = "0"	2399	2400	2401	
Carrier Level *1		V <sub>OX</sub>	R <sub>L</sub> ≥ 40 kΩ		FT = "1"	−7	−3	−1	dBm *2
Output Amplitude *1		V <sub>OPP</sub>			CL ≤ 40 pF		ME = "1"	−3	
					FT = "1"	1.4	2.0	—	V <sub>p-p</sub>
					ME = "0"	2.2	3.0	—	
Output Resistance		R <sub>OX</sub>	—			—	50	—	Ω
Output Load Resistance		R <sub>LX</sub>	—			40	—	—	kΩ
Output Load Capacitance		C <sub>LX</sub>	—			—	—	40	pF
Output DC Voltage		V <sub>OSX</sub>	—			0.48V <sub>DD</sub>	0.50V <sub>DD</sub>	0.52V <sub>DD</sub>	V

Voice signal input (TI)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Voltage Gain	GT	$V_{AO}/V_{TI}$	$\overline{FT} = "1"$ ME = "0"	-2	0	+2	dB
Input Signal Level	*1	$V_{TI}$		—	—	-4	dBm
						0	*2
Input Resistance	$R_{TI}$	$f_{TI} \leq 4\text{ kHz}$		40	100	300	kΩ

Built-in signal ground (SG)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DC Voltage	$V_{SG}$	Without DC Load	$0.48V_{DD}$	$0.50V_{DD}$	$0.52V_{DD}$	V

Receive signal input (AI)

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit	
Input Resistance		R <sub>AI</sub>	f <sub>AI</sub> ≤ 4 kHz		40	100	300	kΩ	
Receive Signal Level		V <sub>IR1</sub>	—		BR = "0"	−30	—	0	dBm *2
		V <sub>IR2</sub>			BR = "1"	−24	—	0	
Bit Error Rate	1200 bps	BER	S/N at AI SIN = "1"	S/N	7 dB	—	2 × 10 <sup>−3</sup>	—	
					11 dB	—	2 × 10 <sup>−5</sup>	—	
	2400 bps				10 dB	—	2 × 10 <sup>−3</sup>	—	
					14 dB	—	2 × 10 <sup>−5</sup>	—	

\*1 Upper is specified for the MSM6882-3, lower for the MSM6882-5  
\*2 0 dBm = 0.775 Vrms

Re-generated receive data timing clock output (RT)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
Data Bit Number for PLL' Lock-in	N <sub>PLL1</sub>	CF = "1"	CT = "0"	*3	—	—	18	bit
	N <sub>PLL2</sub>		CT = "1"		—	—	50	

\*3 Data bit number to lock-in within 22.5 degree

TIMING DIAGRAM

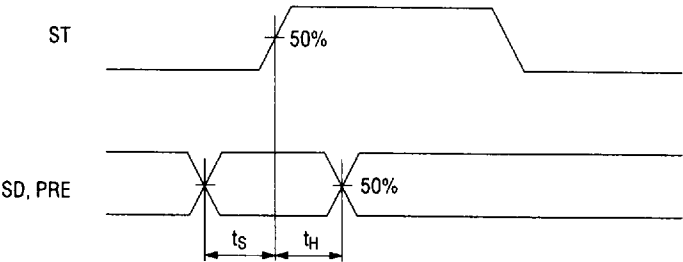


Figure 1 Input Data Timing

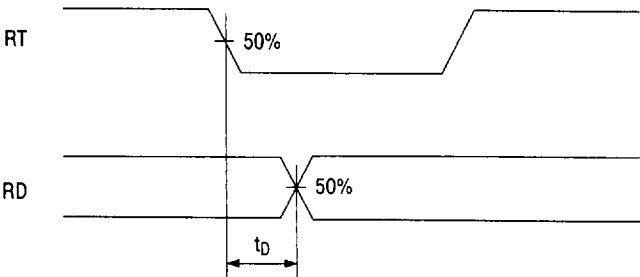
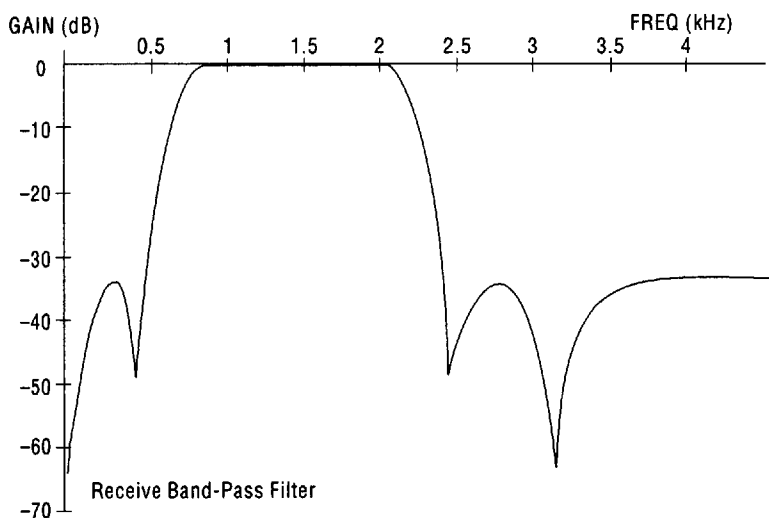
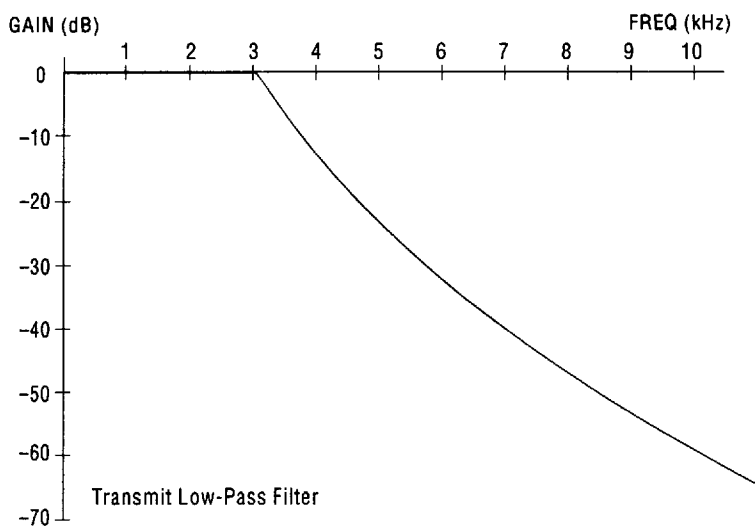


Figure 2 Output Data Timing

## BUILT-IN FILTER FREQUENCY CHARACTERISTICS



Note: When BR = "1", frequency converter circuit (MIXER) is prepared before the receive BPF. Therefore, 1200 Hz input signal is converted to 3600 Hz at BPF output for example.

APPLICATION CIRCUIT

