SIGNAL PROCESSING TECHNOLOGIES

HDAC10181A/B

8-BIT, HIGH SPEED D/A CONVERTERS

FEATURES

- **275 MWPS Conversion Rate - A Version**
- **165 MWPS Conversion Rate - B Version**
- RS-343-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10KH, 100K ECL Compatible
- Single Power Supply
- Stable On-chip Bandgap Reference
- Registered Data And Video Controls
- Differential Current Outputs

APPLICATIONS

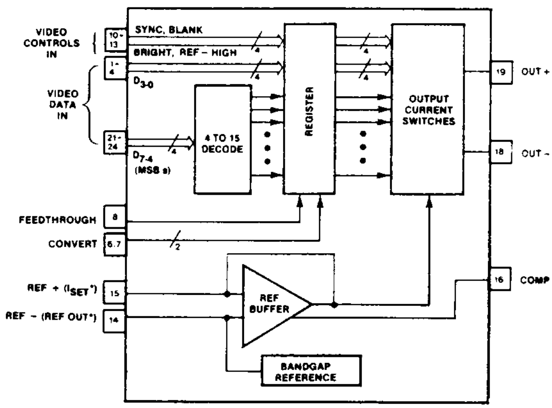
- High Resolution Color or Monochrome Displays
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

3

GENERAL DESCRIPTION

The HDAC10181 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at a 165 or 275 MWPS rate. Complete with video controls (Sync, Blank, Reference White, [Force High] Bright), the HDAC10181 directly drives doubly-terminated 50 or 75 Ohm loads to standard composite video levels. Standard set-up level is 7.5 IRE. The HDAC10181 includes an internal precision bandgap reference which can drive two HDAC10180s in an RGB graphics system. The HDAC10181 contains data and control input registers, video control logic, reference, and current switches in 24 Lead CERDIP, or ceramic sidebrazed DIP.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which the useful life will be impaired)[1]

Supply Voltages

V_{EED} (measured to V_{CCD}) .... – 7.0 to 0.5V
V_{EEA} (measured to V_{CCA}) .... – 7.0 to 0.5V
V_{CCA} (measured to V_{CCD}) .... – 0.5 to 0.5V

Input Voltages

CONV, Data, and Controls V_{EED} to 0.5V ....
(measured to V_{CCD})

REF + (measured to V_{CCA}) .... V_{EEA} to 0.5V
REF – (measured to V_{CCA}) .... V_{EEA} to 0.5V

Temperature

Operating, Ambient .... – 60 to + 140°C
Junction .... + 175°C
Lead, Soldering (10 seconds) .... + 300°C
Storage .... – 60 to + 150°C

Notes:
1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS V_{CCA} = 0.0V, V_{EEA} = V_{EED} = – 5.2V ± 0.3V, T_A = 25°C, C_C = 0pF., I_{SET} = 1.105 mA

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
E_{LI}	Integral Linearity Error	1.0mA < I_{SET} < 1.3mA	I	– 0.37 – 0.95		+ 0.37 + 0.95	% Full Scale LSB
E_{LD}	Differential Linearity Error	1.0mA < I_{SET} < 1.3mA	I	– 0.2 – ½		+ 0.2 + ½	% Full Scale LSB
E_G	Gain Error	T_A = 25°C OVER TEMP RANGE	I	– 15 – 19		+ 15 + 19	% Full Scale
TC_G	Gain Error Tempco		V		250		PPM/°C
C_{REF}	Input Capacitance, REF +, REF –		V		5		pF
V_{OCP}	Compliance Voltage, + Output		I	– 1.2		1.5	V
V_{OCN}	Compliance Voltage, – Output		I	– 1.2		1.5	V
R_{OUT}	Equivalent Output Resistance		I	20			K Ohm
C_{OUT}	Output Capacitance		V		12		pF
I_{OP}	Maximum Current, + Output		IV	45			mA
I_{ON}	Maximum Current, – Output		IV	45			mA
I_{OS}	Output Offset Current		I			½	LSB
V_{IH}	Input Voltage, Logic HIGH		I			– 1.0	V
V_{IL}	Input Voltage, Logic LOW		I			– 1.5	V
V_{ICM}	Convert Voltage, Common Mode Range		I	– 0.5		– 2.5	V
V_{IDF}	Convert Voltage, Differential		IV	0.4		1.2	V
I_{IL}	Input Current, Logic LOW, Data and Controls		I			120	µA
I_{IH}	Input Current, Logic HIGH, Data and Controls		I		10	120	µA
I_{IC}	Input Current, Convert		I		2	60	µA

ELECTRICAL SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS V_{CCA} = 0.0V, V_{EEA} = V_{EED} = −5.2V ±0.3V, T_A = 25°C, C_C = 0pF., I_{SET} = 1.105 mA

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
C_I	Input Capacitance, Data and Controls		V		3		pF
PSR	Power Supply Sensitivity		I	−120		+120	μA/V
I_{EE}	Supply Current		I		175	200	mA

DYNAMIC CHARACTERISTICS R_L = 37.5 Ohms, C_L = 5pF, TA = 25°C, I_{SET} = 1.105 mA

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
F_S	Maximum Conversion Rate	B Grade A Grade	I I	165 275			MWPS
t_{RI}	Rise Time	10% to 90% G.S.	I			1.6	ns
t_{RI}	Rise Time	10% to 90% G.S. R_L = 25 Ohms	V		1.0		ns
t_{SI}	Current Settling Time, Clocked Mode	To 0.2%	V		7		ns
t_{SI}	Current Settling Time, Clocked Mode	To 0.8%	V		5.5		ns
t_{SI}	Current Settling Time, Clocked Mode	To 0.2% R_L = 25Ω	V		4.5		ns
t_{DSC}	Clock to Output Delay, Clocked Mode		I			4	ns
t_{DST}	Data to Output Delay, Transparent Mode		I			6	ns
t_{PWL}	Convert Pulse Width, LOW	B Grade A Grade	I I	3.0 1.8			ns
	Glitch Energy	Area = ½ VT	V		10		pV-s
t_{PWH}	Convert Pulse Width, HIGH	B Grade A Grade	I I	3.0 1.8			ns
BW_{REF}	Reference Bandwidth, −3dB		V		1		MHz
t_S	Set-up Time, Data and Controls		I	1.3	1.8	2	ns
t_H	Hold Time, Data and Controls		I	0.5	0		ns
SR	Slew Rate	20% to 80% G.S.	I	400			V/μS
FT_C	Clock Feedthrough		I			−48	dB

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified conditions.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at $T_a = 25°C$, and sample tested at specified temperature.
III	QA sample tested only at specified temperatures
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

APPLICATION INFORMATION

The HDAC10181 is a high speed video Digital-to-Analog converters capable of up to 275 MWPS conversion rates. This makes the devices suitable for driving 1500 X 1800 pixel displays at 70 to 90 Hz update rates. In addition, the HDAC10181 includes an internal bandgap reference which may be used to drive other HDAC10180s if desired. (See HDAC10180 Data Sheet)

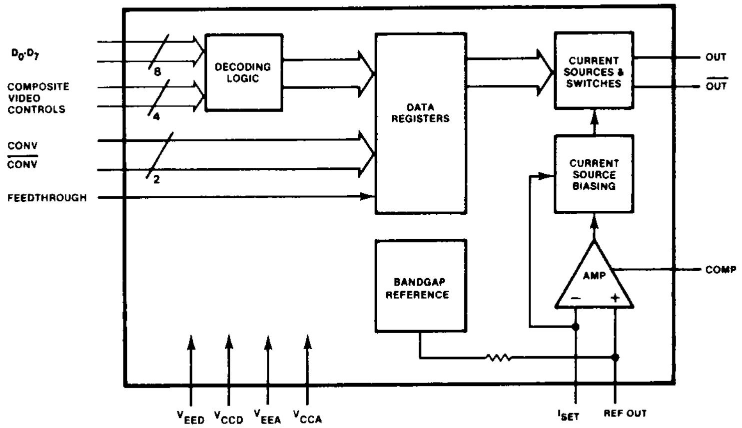
The HDAC10181 is separated into different conversion rate categories as shown in Table 2.

The HDAC10181 has 10KH and 100K ECL logic level compatible video control and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The HDAC10181 is segmented so that the four MSBs of the input data are separated into a parallel "thermometer" code. From here, fifteen current sinks, which are identical, are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches. The MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

The video control inputs drive weighted current sinks which are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation between the video control inputs and data. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered "VIDEO DACs".

FUNCTIONAL DIAGRAM



SPT

TYPICAL INTERFACE CIRCUIT

GENERAL

A typical interface circuit using the HDAC10181 in a color raster application is shown in Figure 2. The HDAC10181 requires few external components and is extremely easy to use. The very high operating speeds of the HDAC10181 requires good circuit layout, decoupling of supplies, and proper design of transmission lines. The following are several considerations that should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the HDAC10181. Note that all ECL inputs are terminated as close to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 Ohms, which is easily terminated using a 330 Ohm resistor to V_{EE} and a 220 Ohm resistor to Ground. This arrangement gives a Thevenin equivalent termination of 130 Ohms to −2 Volts without the need for a 2 Volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that the stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC10181 provides separate digital and analog ground connections to simplify ground layout.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a dual 50 or 75 Ohm load transmission system as shown. The source impedances of the HDAC10181 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CCA} which is connected to the source termination resistor R_S.

3

FIGURE 1 TIMING DIAGRAM

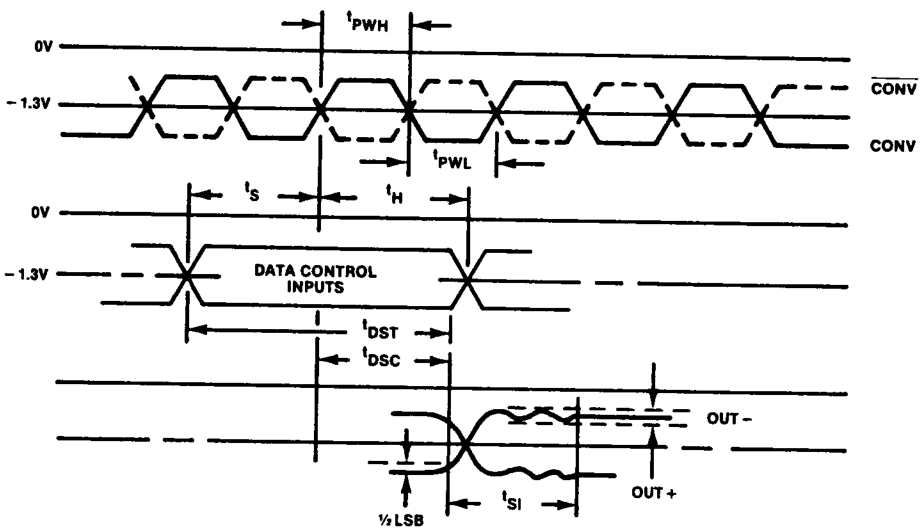
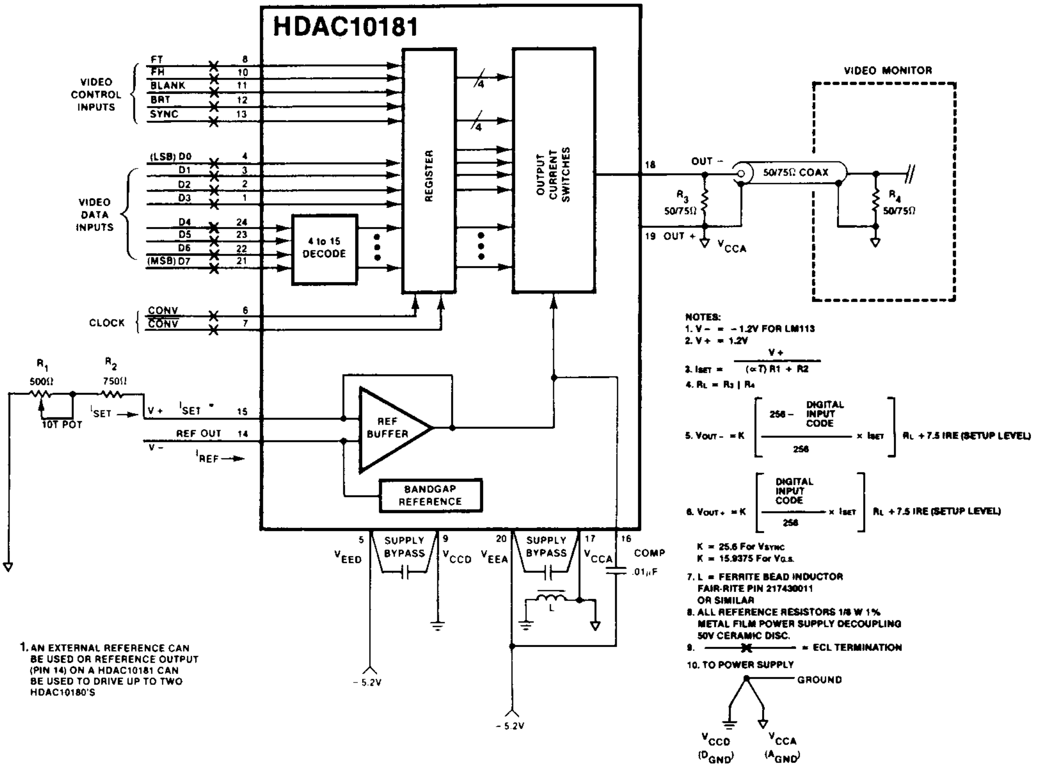


FIGURE 2 TYPICAL INTERFACE CIRCUIT



POWER CONSIDERATIONS

The HDAC10181 operates from a single standard −5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC10181's inherent supply noise rejection characteristics. As shown in Figure 2, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

The HDAC10181 operates with separate analog (V_{EEA}) and digital (V_{EED}) power supplies to establish high noise immunity. Both supplies can eventually be connected to the same power source, but they should be individually decoupled as mentioned previously. The digital supply has a separate ground return which is V_{CCD}. The analog supply return is V_{CCA}. All power and ground pins must be connected in any application. If a +5V power source is required, the ground pins V_{CCD} and V_{CCA} become the positive supply pins while V_{EED} and V_{EEA} become the ground returns. The relative polarities of the other voltages on inputs and outputs must be maintained.

REFERENCE CONSIDERATIONS

The HDAC10181 has one input (I_{SET}) and one reference output (REF OUT). Both pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer amplifier. The HDAC10181 has a bandgap reference connected internally to the inverting input of the buffer amplifier and the REF OUT.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy (see Figure 5).

Since the analog output currents are proportional to the digital input data and the reference current (I_{SET}), the full-scale output may be adjusted by varying the reference current. I_{SET} is controlled through the I_{SET} input on the HDAC10181. A method and equations to set I_{SET} is shown in Figure 2. The HDAC10181 uses its own reference voltage for setting up I_{SET} as shown in Figure 2. The value for I_{SET} can be varied with the 500 Ohm trimmer to change the full scale output. A double 50 Ohm load (25 Ohm) can be driven if I_{SET} is increased 50% more than I_{SET} for doubly terminated 75 Ohm video applications.

COMPENSATION

The HDAC10181 provides an external compensation input (COMP) for the reference buffer amplifier. In order to use this pin correctly, a capacitor (C_C) should be connected between COMP and V_{EEA} as shown in Figure 2. Keep the lead lengths as short as possible. If the reference is to be kept as a constant, the Cc should be large (.01μF). The value of Cc determines the bandwidth of the amplifier. If modulation of the reference is required, smaller values of Cc can be used to get up to a 1 MHz bandwidth.

DATA INPUTS AND VIDEO CONTROLS

The HDAC10181 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) to minimize glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as mentioned earlier. The controls and data inputs are all 10KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than 8-bits are used.

The HDAC10181 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a set-up time of t_s before, and a hold time of t_h after the rising edge of the clock (CONV) in order to be synchronously registered. The set-up and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors (see Figure 1).

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table 1 shows the video control effects on the analog output. Internal logic governs Blank, Sync and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (Figure 4).

Reference white video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL driven, differentially, by utilizing CONV and $\overline{\text{CONV}}$ (Figure 3). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the HDAC10181. Since the actual switching threshold of CONV is determined by $\overline{\text{CONV}}$, the clock can be driven single-ended by connecting a bias voltage to $\overline{\text{CONV}}$. The switching threshold of CONV is set by this bias voltage.

ANALOG OUTPUTS

The HDAC10181 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scale output can be changed by setting I_{REF} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 Ohm load to standard video levels. In the standard configuration of Figure 7, the output voltage is the product of the output current and load impedance and is between 0 and − 1.07V. The OUT − output (Figure 4) will provide a video output waveform with the SYNC pulse bottom at the − 1.07V level. The OUT + is inverted with SYNC up.

Table 1 Video Control Operation (Output values for Set-up = 10 IRE and 75 Ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out – (mA)	Out – (V)	Out – (IRE)	Description
1	X	X	X	X	28.57	– 1.071	– 40	Sync Level
0	1	X	X	X	20.83	– 0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	– 0.073	100	Normal High Level
0	0	0	0	000...	19.40	– 0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	– 0.073	100	Normal High Level
0	0	0	1	000...	17.44	– 0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

Table 2 The HDAC10181 family and speed designations.

Part Number	Update	Comments
HDAC10181A	275 MWPS	Suitable for 1200 X 1500 to 1500 X 1800 displays at 60 to 90 Hz update rate.
HDAC10181B	165 MWPS	Suitable for 1024 X 1280 to 1200 X 1500 displays at 60 to 90 Hz update rate.

FIGURE 3 CONVert, $\overline{\text{CONVert}}$ SWITCHING LEVELS

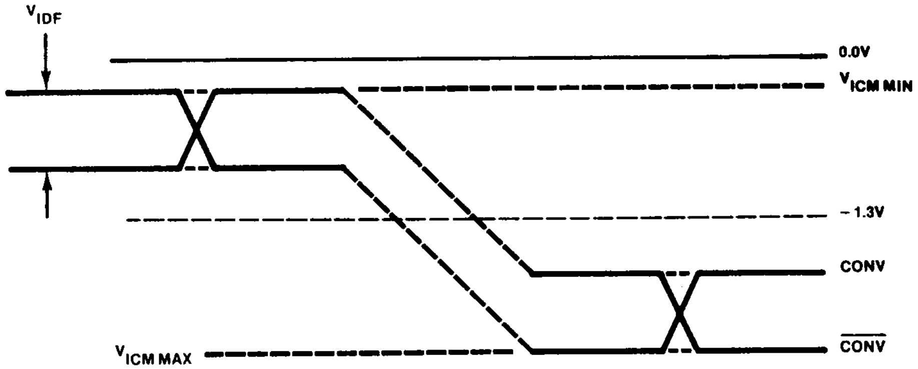


FIGURE 4 VIDEO OUTPUT WAVEFORM FOR STANDARD LOAD

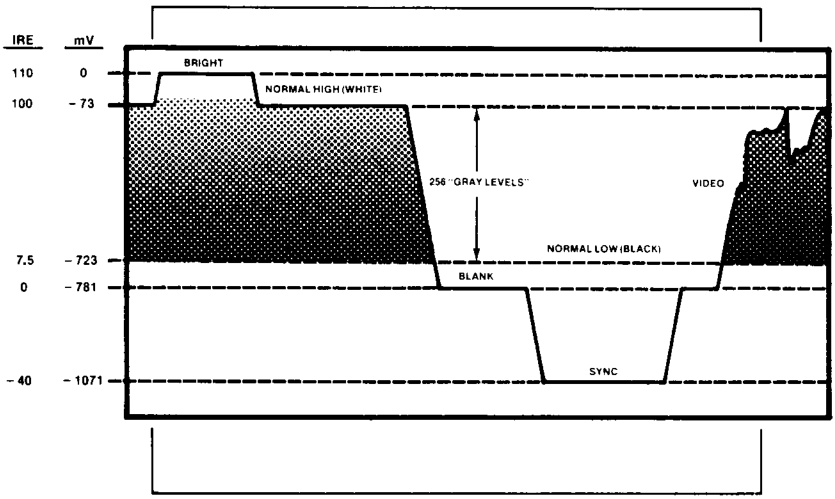


FIGURE 5 EQUIVALENT INPUT CIRCUITS—DATA, CLOCK, CONTROLS AND REFERENCE

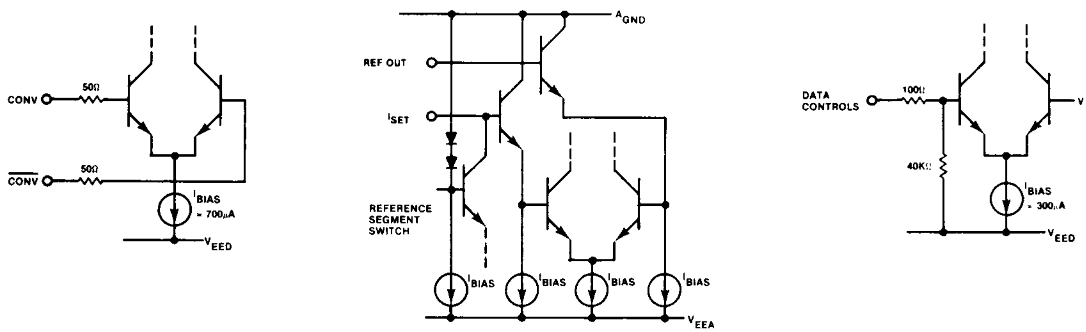


FIGURE6 DAC OUTPUT CIRCUIT

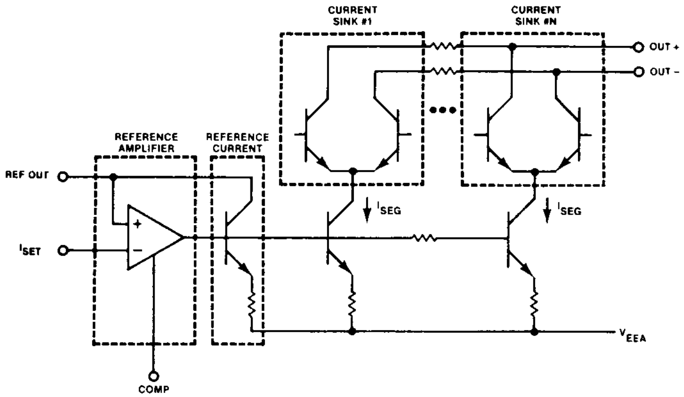


FIGURE 7A STANDARD LOAD

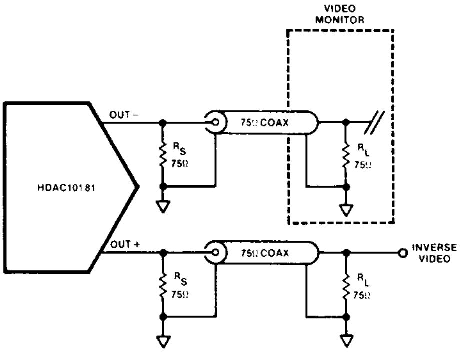
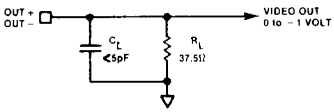


FIGURE 7B TEST LOAD



TYPICAL RGB GRAPHICS SYSTEM

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch. This may also eliminate the need for individual calibration of each DAC during production assembly.

The HDAC10181 contains an internal precision bandgap reference which completely eliminates the need for an external reference. The reference can supply up to 50μA to an external load, such as another DAC reference input.

The circuits shown in Figure 8 illustrate how a single HDAC10181 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the HDAC10181's reference output. The HDAC10180s shown are especially well-suited to be slaved to a 10181, since they are essentially 10181s without the reference. The 10180 is pin-compatible with the TDC1018, which like the 10180, does not have an internal reference. Although either the TDC1018 or HDAC10180 may be slaved from an HDAC10181, the higher performance HDAC10180 is the best choice for new designs. (See HDAC10180 Data Sheet)

No external reference is required for operation of the HDAC10181, as this function is provided internally. The internal reference is a bandgap type and is suitable for operation over extended temperature ranges. The HDAC10180 must use an external reference.

FIGURE 8
TYPICAL RBG GRAPHICS SYSTEM

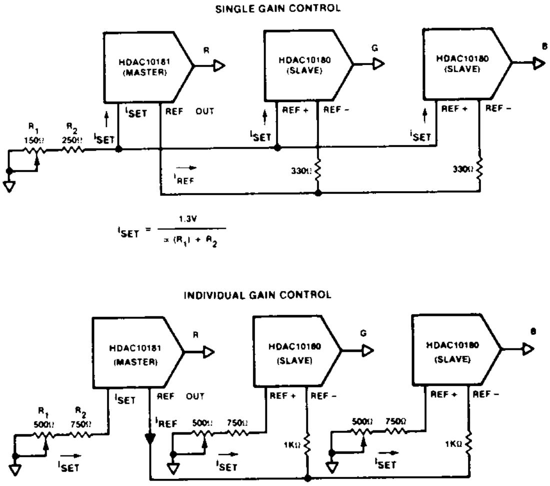
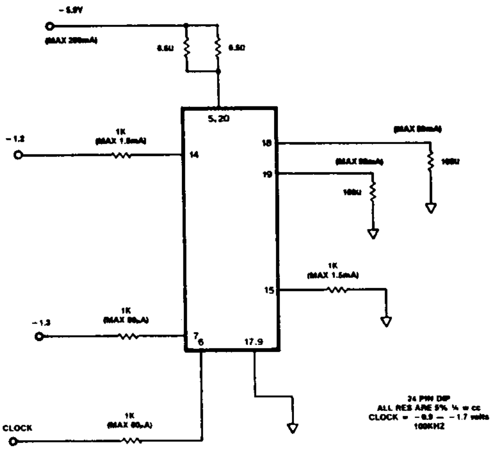
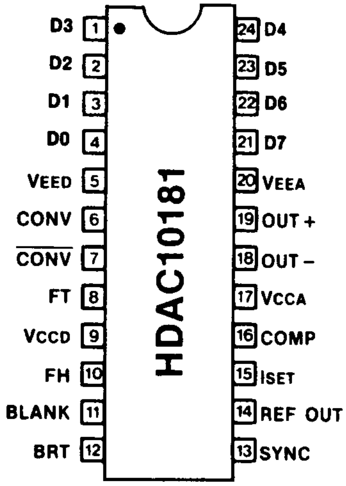


FIGURE 9 BURN-IN CIRCUIT



PIN ASSIGNMENTS



24 LEAD DIP

PIN FUNCTIONS

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
VEED	Digital Negative Supply
CONV	Convert Clock Input
$\overline{\text{CONV}}$	Convert Clock Input Complement
FT	Register Feedthrough Control
VCCD	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF OUT	Reference Output
ISET	Reference Current + Input
COMP	Compensation Input
VCCA	0Analog Positive Supply
OUT –	Output Current Negative
OUT +	Output Current Positive
VEEA	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

***For Ordering Information See Section 1.*