OKI semiconductor

MSM6994-02 SS/GS/JS

FRONT END PROCESSOR FOR MULTI-STANDARD MODEM

General Description

The MSM6994 is a New Front End Processor for modems, which allows construction of the standard 300 FDX through 9600 FDX modems when used with a general digital signal processor. This device incorporates band-limit-filtering, carrier-detection call progress tone detection, and A/D and D/A convertors at 5 MIPs. Every function is digitally processed by the core processor provided on chip, and has the mask programmability to adapt to user defined filter specifications.

The MSM6994 utilizes a unique oversampling delta-sigma technique for A/D and D/A conversion, which provides 80dB dynamic range with 13 bit accuracy. The MSM6994 has 4 major interfaces: microprocessor interface for operating mode control, DSP interface for Transmit/Receive data transfer, analog interface for Transmit out/Receive in, and DAA interface for line network control.

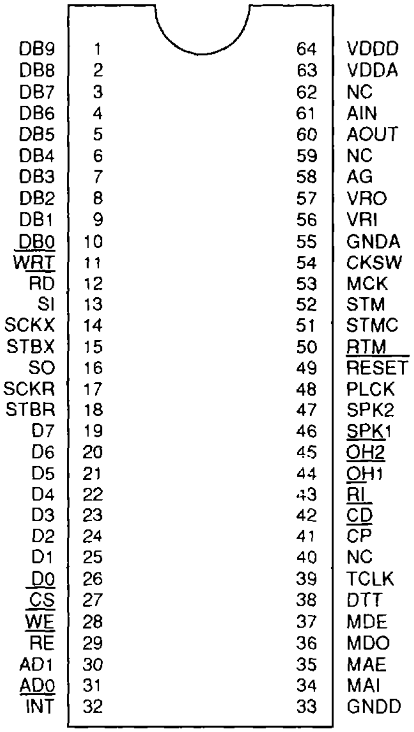
The MSM6994 operates with a single 5V power supply, and typical power dissipation is 150mW. The chip is packaged in a 64 pin Mini DIP, 64 pin Flatpack, or 68 pin PLCC package.

Features

- General Purpose Front End Processor;
  Intelligent 300 FDX 9600 FDX Modems
- Handles a maximum of 8 modes of Modem applications;
  Ex: V.21, BELL103, V.22/BELL212/V.22bis, V.23, BELL202, V.27, V.29, V.32
- On chip A/D, D/A Converters;
  Oversampling (2.592 MHz) delta-sigma A/D, D/A converters
- On-chip Core Digital Signal Processor
  Channel filtering, Tone detection, Carrier detection, AGC
  1 Kword Program Read Only Memory, 1 Kword Data Read Only Memory
  64 words Random Access Memory at 5.184 MIPs
- Powerful instruction Set;
  4 cycles for one biquad filter processing
- User defines filter specifications
- Single +5V, 150mW Typical
- 64 pin MiniDip/Flatpack, 68 pin PLCC package

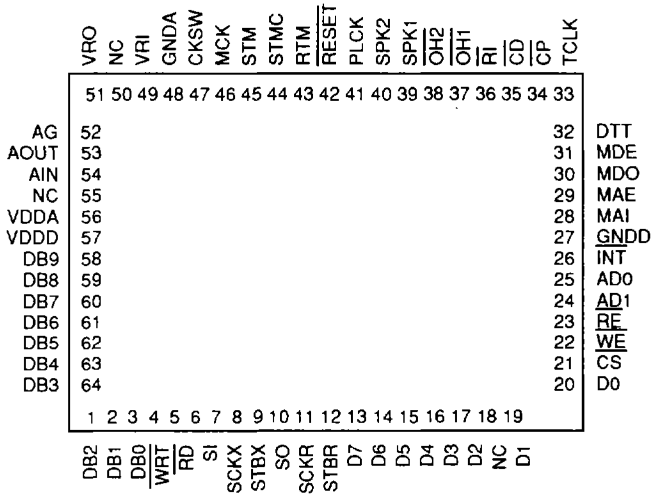
Pin Configuration (Top View)

64 pin Mini DIP (MSM6994SS)

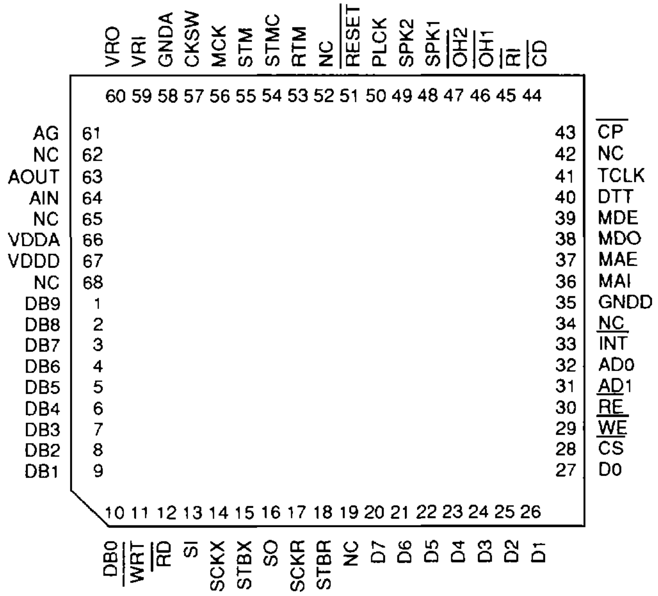


NC: Non connection pin

64 pin Flat (MSM6994GS)



68 pin PLCC (MSM6994JS)



Block Diagram

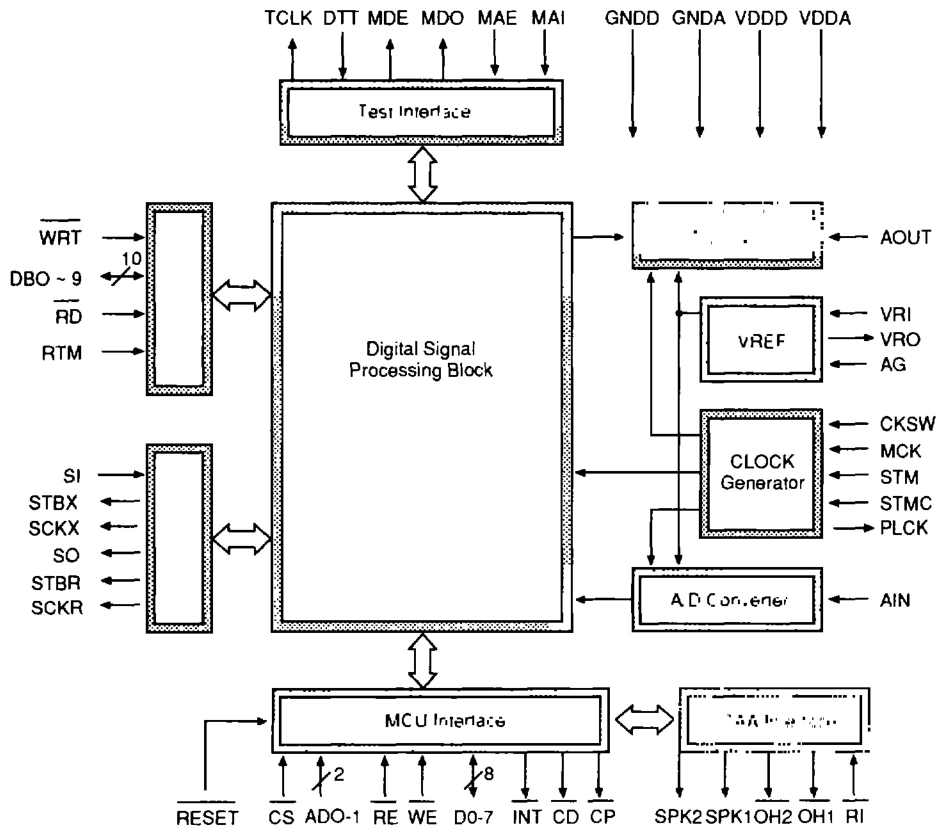


Figure 1

Signal Flow

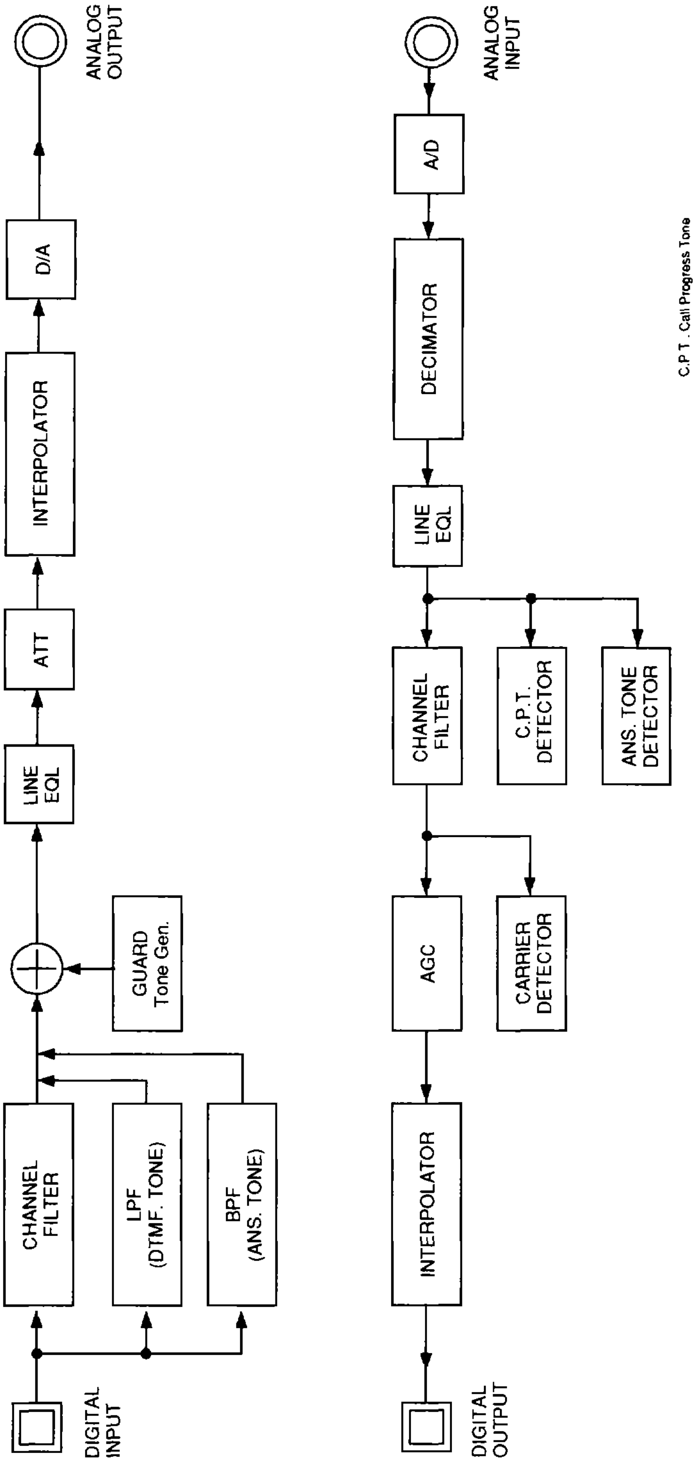
MSM6994 operation is synchronized with the sampling rate clock which should be either 9.6 kHz or 7.2 kHz.

Figure 2 shows the signal flow diagram of the MSM6994. The input digital data, which is the modulated transmit data generated by the external DSP, is given to the chip through the DSP interface. The on-chip DSP will execute channel-filtering, DTMF tone filtering, answer tone filtering, and if necessary, add the guard tone signal to the band-limited signal. Line equalization and variable attenuation will also be done by the on-chip DSP, and its output signal will be routed to the transmit interpolator which interpolates the incoming signal into the 2.592 MHz sampling rate data for D/A converter. The D/A output signal is given to the smoothing filter, and its output signal is transmitted over the phone line through DAA.

The receive analog signal is given to the A/D converter through the pre-low pass filter, and is converted into 2.592 MHz sampling rate digital data. The decimator will suppress the out-of-band noise from the A/D output digital data, and convert the 2.592 MHz sampling rate digital data into the 9.6 or 7.2 kHz rate digital data which is routed to the on-chip DSP.

The on-chip DSP executes channel filtering, Call Progress Tone detecting and Answer Tone detection.

Automatic Gain Control and Carrier detection is also handled by the on-chip DSP, and its output signal is routed to the receive interpolator which interpolates the 9.6 or 7.2 kHz rate digital data into the 2.592 MHz sampling rate digital data. In this scheme, the external DSP can trap the receive digital data at its own receive timing.



C.P.T. . Call Progress Tone

Figure 2 Signal Flow Diagram

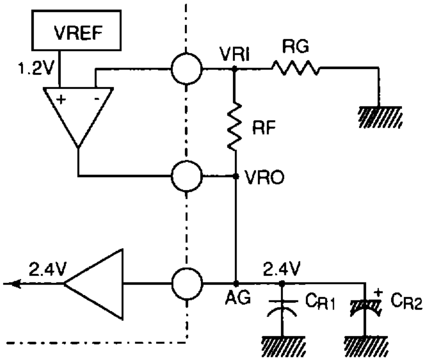
Pin Description

- Power

NAME	DIP	FLAT	PLCC	TYPE	Description
GNDA	55	48	58	I	Analog Circuit Ground, 0V
GNDD	33	27	35	I	Digital Circuit Ground, 0V
VDDA	63	56	66	I	Analog Circuit Power Supply, +5.0V ± 5%
VDDD	64	57	67	I	Digital Cirucit Power Supply, +5.0V ± 5%

Note: GNDA and GNDD will be connected each other externally.
Note: VDDA and VDDD will be connected each other externally

- Voltage Reference

NAME	DIP	FLAT	PLCC	TYPE	Description
VRI	56	49	59	I	 $R_G = R_F$ (25K) $C_{R1} = 0.1\ \mu F$ $C_{R2} = 22\ \mu F$ The voltage of the pin VRO should be adjusted to be 2.4V through VRI and VRO pins by using the external resistors shown above. Its output should be fed to pin AG which is used as the on-chip signal ground and the reference for A/D, D/A conversions. AG should be bypassed with 0.1 and 22 μF capacitors to ground.
VRO	57	51	60	$\overline{O}$	
AG	58	52	61	I	

- Parallel MCU interface

NAME	DIP	FLAT	PLCC	TYPE	Description
AD0~1	30, 31	24, 25	31, 32	I	Internal Registers Address Assignment.
D0~7	19~26	12~20	20~27	I/O	Data Bus. These pins are bidirectional tri-state bus, through which information can be transferred to and from the internal registers.
$\overline{CS}$	27	21	28	I	Chip select. Digital "0" on this pin allows a read cycle or a write cycle on D0~7 data bus.
$\overline{WE}$	28	22	29	I	Write. Digital "0" on this pin makes data available on D0~7 for writing into an internal register Data is latched on the rising edge of WE. No data is written unless both WE and CS are active low.
$\overline{RE}$	29	23	30	I	Read. Digital "0" on this pin requests a read of an internal register. Data cannot be output unless both RE and CS are active low.
$\overline{INT}$	32	26	33	O	Interrupt. This output is used to inform MCU that a detect flag has occurred. MCU must then read the status register to determine which detection triggered the interrupt. INT will stay active until the MCU reads the status register.
$\overline{RESET}$	49	42	51	I	Reset. Digital "0" on this pin makes the chip inactive. All internal registers and sequence flags of the on-chip DSP are reset.
$\overline{CD}$	42	35	44	O	Carrier Detect. Digital "0" on this pin indicates that an in-band carrier has been detected in the receive channel. This output is directly associated with SR register bit 3.
$\overline{CP}$	41	34	43	O	Call Progress Tone Detect Digital "0" on this pin indicates the presence of call progress tones in the 350 to 620Hz bandwidth. This output is directly associated with SR register bit 2.

- DSP interface

NAME	DIP	FLAT	PLCC	TYPE	Description
DB0	1~10	1~3, 58~64	1~10	I/O	Transmit/Receive Data Bus. These pins are a bi-directional tri-state bus, through which transmit/ receive data will be transferred to and from the on-chip DSP.
$\overline{\text{WRT}}$	11	4	11	I	Write. Digital "0" on this pin makes data available on DB0~9 for writing into an input buffer of the rising edge of WRT. No data is written unless WRT is active low.
$\overline{\text{RD}}$	12	5	12	I	Read. Digital "0" on this pin requests a read of an output buffer of the receive interpolator. Data cannot be output unless RD is active low.
RTM	50	43	53	I	Receive Timing. The rising edge of this signal allows the latching of the receive interpolator output data into the output buffer. Usually, RD will be directly connected to this pin except for the application when the read timing is different from the receive timing.

- Serial interface

NAME	DIP	FLAT	PLCC	TYPE	Description
SI	13	6	13	I	Serial Data Input. The 16 bits of serial data will be clocked into the serial input buffer on the falling edge of SCKX.
SCKX	14	7	14	O	Shift Clock for SI. 18 consecutive shift clocks will appear synchronized with STBX. Serial data should be clocked out on the rising edge of SCKX. The clock cycle of SCKX is 1.296 MHz.
STBX	15	8	15	O	Framing pulse for SI. After reading the serial input buffer data into the on-chip DSP, the framing pulse STBX will appear to request the next serial input data. This pulse is syncrhronized with SCKX and its period equals to one clock of SCKX.
SO	16	9	16	O	Serial Data Output. The 16 bit serial data will be clocked out from the serial output buffer on the rising edge of SCKR.
SCKR	17	10	17	O	Shift clock for SO. 18 consecutive shift clocks will appear synchronized with STBR. Serial data will be latched on the falling edge of SCKR. The clock cycle of SCKR is 1.296 MHz.
STBR	18	11	18	O	Framing pulse for SO. After writing the serial output buffer data from the on-chip DSP, the framing pulse of STBR will appear to send out the serial output data. This pulse is synchronized with SCKR and its period equals to one clock of SCKR.

- Analog interface

NAME	DIP	FLAT	PLCC	TYPE	Description
AOUT	60	53	63	O	Transmit analog signal output pin.
AIN	61	54	64	I	Receive analog signal input pin.

- Test interface

NAME	DIP	FLAT	PLCC	TYPE	Description
MAI	34	28	36	I	These pins are used for IC testing only. Input pins of MAI, DTT and MAE should be connected to a digital "0" for normal use.
MAE	35	29	37	I	
MDO	36	30	38	O	
MDE	37	31	39	O	
DTT	38	32	40	I	
TCLK	39	33	41	O	

- DAA interface

NAME	DIP	FLAT	PLCC	TYPE	Description
SPK1	46	39	48	O	These pins are mainly used as the control signals for the speaker facility. Bit 3 and Bit 2 of the DAA register correspond to SPK1 and SPK 2 on positive logic, respectively.
SPK2	47	40	49	O	
$\overline{\text{OH1}}$	44	37	46	O	These pins are mainly used as the control signals for the relay facility. Bit 1 and Bit 0 of the DAA register correspond to $\overline{\text{OH1}}$ and $\overline{\text{OH2}}$ on negative logic, respectively.
$\overline{\text{OH2}}$	45	38	47	O	
$\overline{\text{RI}}$	43	36	45	I	Ringing indicator. Digital "0" on this pin informs the status that the external ringing detector is detecting the ring signal from the phone line. Bit 0 of the status register corresponds to $\overline{\text{RI}}$ on negative logic.

- Clock interface

NAME	DIP	FLAT	PLCC	TYPE	Description
MCK	53	46	56	I	Master Clock. The clock frequency is 20.736 MHz ± 100 ppm, and the duty ratio should be within 40 to 60%.
STM	52	45	55	I	Sample Timing Clock. The MSM6994 will operate in the synchronizing mode with the rising edge of this clock. When CKSW is a '1', the on-chip D-PLL will chase the rising edge of STM for procedure synchronization. WRT can be substituted for STM. The clock frequency of STM must be either 9.6 kHz or 7.2 kHz.
STMC	51	44	54	I	Timing Clock Select. STMC = 1 (High); STM = 7.2 kHz STMC = 0 (Low); STM = 9.6 kHz
CKSW	54	47	57	I	STM Select. A "1" on this pin allows M6994 to synchronize with asynchronous STM. Digital '0' on this pin allows MSM6994 to synchronize with synchronous STM, which is generated on the same MCK.
PLCK	48	41	50	O	Digital PLL Output. When CKSW is set to digital '1', the locked DPLL output (5.184MHz) will appear on this pin. When CKSW is on digital "0", the internally generated clock (5.184MHz) will appear on this pin

Register Description

Four 8-bit internal registers are accessible for control and status monitoring. These registers can be accessed into the read or write mode by addressing the AD0-1. The control register CR0 determines the basic operation mode for the MODEM standards. The control register CR1 controls the auxiliary functions for channel processing. The status register SR is a detect register which provides the indication of monitored MODEM status conditions. The DAA register DR is directly associated with DAA interface, which controls the Direct Access Arrangement circuitry. Table 1 shows the register bit summary of the MSM6994. CR0-1 & DR are WRITE registers which are allowed only to write, but user can read the written data. SR is a READ register which is allowed only to read, and the user can not write the data.

Table 1 Register Bit Summary

		Address		Data Bit							
Register		AD1	AD0	B7	B6	B5	B4	B3	B2	B1	B0
Control Register	CR0	0	0	Operating Mode		Modem Standard			Answer/ originate	Transmit Enable	Backward Channel Enable
				MODE4	MODE3	MODE2	MODE1	MODE0			
Control Register	CR1	0	1	Guard tone Enable	Guard tone Select	Serial/ Parallel Select	Line EQL Enable	AGC Enable	ATT2	ATT1	ATT0
Status Register	SR	1	0					Carrier Detect	C.P.T. Detect	Answer Tone Detect	Ring indicator
DAA Register	DR	1	1					Speaker Control		OFF Hook Control	
								SPK1	SPK2	OH1	OH2

CR0	B7	B6	B5	B4	B3	B2	B1	B0
	OPERATING MODE		MODEM STANDARD			ANSWER/ ORIGINATE	TRANSMIT ENABLE	BACKWARD CHANNEL ENABLE
WRITE	MODE 4	MODE 3	MODE 2	MODE 1	MODE 0			

BIT No.	NAME	CONDITION			DESCRIPTION	
B0	BACKWARD CHANNEL ENABLE	0			Backward Channel disable	
		1			Backward Channel enable	
B1	TRANSMIT ENABLE	0			Transmit disable	
		1			Transmit enable	
B2	ANSWER/ ORIGINATE	0			Originate mode (transmits Low Band)	
		1			Answer mode (transmits High Band)	
B3~5	MODEM STANDARD	B5	B4	B3		
		0	0	0	CCITT V.21	STMC = 1
		0	0	1	CCITT V.22/V.22 bis/Bell 212A	STMC = 1
		0	1	0	CCITT V.23 with backward	STMC = 0
		0	1	1	CCITT V.27 ter with backward	STMC = 0
		1	0	0	CCITT V.29	STMC = 0
		1	0	1	User option	
		1	1	0	CCITT V.32 with notch	STMC = 1
		1	1	1	CCITT V.32	STMC = 1
B6~7	OPERATING MODE	B7	B6		Data Transmission Mode	
		0	0		Data Transmission path will be formed. Digital transmit data through DSP or Serial I/O interface will be processed and transmitted from the AOUT pin. Analog receive signal input to the AIN pin will be digitized by A/D, and processed to output the digital data to the external modem processor through DSP or Serial I/O interface.	
		0	1		Loop Test Mode Analog Loop Back path will be formed. Digital transmit data will bypass the transmit filter, and be routed to the receive filter. At this time, AOUT will be grounded, and the receive signal on AIN will be ignored.	
		1	0		Call Progress Mode In originate mode, call progress tone detector and answer tone detector will be valid, and TRANSMIT ENABLE (B1) will enable the DTMF filtering procedure. In Answer mode, TRANSMIT ENABLE (B1) will enable the Answer tone filtering procedure. Refer to Figure 2.	
		1	1		Test Mode This mode will be used for IC testing only. User should not select this mode.	

CR1	B7	B6	B5	B4	B3	B2	B1	B0
WRITE	GUARD TONE ENABLE	GUARD TONE SELECT	SERIAL/ PARALLEL SELECT	LINE EQL ENABLE	AGC ENABLE	ATT2	ATT1	ATT0

<table>
<tr><th>BIT No.</th><th>NAME</th><th>CONDITION</th><th>DESCRIPTION</th></tr>
<tr><td>B0</td><td>ATT0</td><td rowspan="3"></td><td rowspan="3">Transmit Signal Attenuator
<table><tr><th>B2</th><th>B1</th><th>B0</th><th>ATT (dB)</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>5</td></tr><tr><td>1</td><td>1</td><td>0</td><td>6</td></tr><tr><td>1</td><td>1</td><td>1</td><td>7</td></tr></table></td></tr>
<tr><td>B1</td><td>ATT1</td></tr>
<tr><td>B2</td><td>ATT2</td></tr>
<tr><td rowspan="2">B3</td><td rowspan="2">AGC ENABLE</td><td>0</td><td>AGC disable</td></tr>
<tr><td>1</td><td>AGC enable</td></tr>
<tr><td colspan="4">When AGC is disabled, the serial 16 bits output data of receive BPF will appear at SO.</td></tr>
<tr><td rowspan="2">B4</td><td rowspan="2">LINE EQL ENABLE</td><td>0</td><td>Line EQL disable (flat)</td></tr>
<tr><td>1</td><td>Line EQL enable (see Figure 8)</td></tr>
<tr><td rowspan="2">B5</td><td rowspan="2">SERIAL/ PARALLEL SELECT</td><td>0</td><td>Parallel Input (DSP interface 10 bits)</td></tr>
<tr><td>1</td><td>Serial Input (Serial interface 16 bits)</td></tr>
<tr><td rowspan="2">B6</td><td rowspan="2">GUARD TONE SELECT</td><td>0</td><td>1800 Hz</td></tr>
<tr><td>1</td><td>500 Hz</td></tr>
<tr><td rowspan="2">B7</td><td rowspan="2">GUARD TONE ENABLE</td><td>0</td><td>Transmit Guard Tone disable</td></tr>
<tr><td>1</td><td>Transmit Guard Tone enable</td></tr>
</table>

SR READ	B7	B6	B5	B4	B3	B2	B1	B0
					CARRIER DETECT	C.P.T. DETECT	ANSWER TONE DETECT	RINGING INDICATOR

BIT No.	NAME	CONDITION	DESCRIPTION
B0	RING INDICATOR	0	RING INDICATOR OFF
		1	RING INDICATOR ON
			* This bit will be directly set by the status of the $\overline{RI}$ pin.
B1	ANSWER TONE DETECT	0	No answer tone detected.
		1	Indicates detection of 2100 or 2225 Hz answer tone. This function will be valid in originate mode.
B2	C.P.T. DETECT	0	No call progress tone detected.
		1	Indicates presence of call progress tones in the 350 to 620 Hz bandwith
B3	CARRIER DETECT	0	No carrier detected in the receive channel.
		1	Indicates detection of the carrier signal in the receive channel.
	The status change of B0 to B3 is informed by the $\overline{INT}$ signal.		

DR WRITE	B7	B6	B5	B4	SPEAKER CONTROL		OFF HOOK CONTROL	
					SPK1	SPK2	OH1	OH2

BIT No.	NAME	CONDITION	DESCRIPTION
B0	OH2	0	OFF-HOOK Control.
		1	Telephone side relay control.
B1	OH1	0	OFF-HOOK Control.
		1	Line side relay control.
B2	SPK2		Speaker Volume Control
B3	SPK1		

B1	B2	Description
0	0	Control-0
0	1	Control-1
1	0	Control-2
1	1	Control-3

Electrical Specifications

- ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
VDD Supply Voltage	VDD	+7	V	
Analog Applied Voltage	VAIN	-0.3 ~ VDD + 0.3	V	VDD: 4.75 ~ 5.25 V
Digital Applied Voltage	VDIN	0.3 ~ VDD + 0.3		
Operating Temperature	TOP	-40 ~ + 85	°C	
Storage Temperature	TST	-55 ~ + 150	°C5	

- RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN	TYP	MAX	Unit	Note
VDD Supply Voltage	VDD	4.75	5.0	5.25	V	
Analog Input Voltage	VAIN	0.5 VAG		1.5 VAG	V	
Digital Input Rise Time	TR	0		50	ns	
Digital Input Fall Time	TF	0		50	ns	
MASTER Clock Frequency	FMCK	20.374	20.736	20.738	MHz	MCK ± 100 ppm
MASTER Clock Duty Ratio	DMCK	40	50	60	%	
Operating Temperature	TOP	0		70	°C	
Operating Humidity	HOP	0		80	%	
AG Input Voltage	VAG	2.38	2.40	2.42	V	
STM Input Clock Frequency	FSTM		7.2		kHz	STMC = 1
			9.6		kHz	STMC = 0
STM Pulse Width	PWST	200			ns	
RTM Pulse Width	PWRT	400			ns	
VREF Adjust Resistor	R_F		25		kΩ	VRI to VRO
VREF Terminate Resistor	P_G		25		kΩ	VRI to GND

RECOMMENDED OPERATING CONDITIONS (continued)

Parameter	Symbol	MIN	TYP	MAX	Unit	Note
VREF Bypass Capacitor 1	C_{R1}		0.1		μF	
VREF Bypass Capacitor 2	C_{R2}		22		μF	
VDD Bypass Capacitor 1	C_{D1}		0.2		μF	
VDD Bypass Capacitor 2	C_{D2}		22		μF	
Analog Output Load	AOL	20			kΩ	
Digital Output Load	DOL			100	PF	

- DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	MIN	TYP	MAX	Unit	Note
Supply Current	IDD		25	35	mA	
Digital Input High Voltage	VIH	2.0		VDD	V	
Digital Input Low Voltage	VIL	0		0.8	V	
Digital Input High Current	IIH	-10		10	μA	
Digital Input Low Current	IIL	-10		10	μA	
Digital Output High Voltage	VOH	2.4		VDD	V	IOH = -20μA
Digital Output Low Voltage	VOL	0		0.4	V	IOL = 0.4mA
RESET Input High Voltage	VIHR	4.0		VDD	V	
RESET Input Low Voltage	VILR	0		2.0	V	
AOUT Offset Voltage	VAOF	-50		50	mV	

- AC ELECTRICAL CHARACTERISTICS

Parameter		Symbol	MIN	TYP	MAX	Unit	Note
Analog Input Resistance		AIR		10		MΩ	AIN, AG, VRI
Analog Input Capacitance		AIC		10		PF	
Analog Output Load (Resistance)		AOLR	50			kΩ	AOUT, VRO
Analog Output Load (Resistance)		AOLC			100	PF	
Digital Input Capacitance		DIC		5		PF	
Digital Output Load (Resistance)		DOLR	1			kΩ	
Digital Output Load (Capacitance)		DOLC			100	PF	
Filter Response (Relative)							
V.21	Loss at 500Hz	L1L1	38	39		dB	Low band
	Loss at 900Hz	L1L2	1.9	2.4	2.9	dB	
	Loss at 1100Hz	L1L3		0		dB	
	Loss at 1300Hz	L1L4	6.0	6.5	7.0	dB	
	Loss at 1800Hz	L1L5	53	54		dB	
	Loss at 600Hz	L1H1	54	55		dB	High band
	Loss at 1600Hz	L1H2	0.5	1.0	1.5	dB	
	Loss at 1800Hz	L1H3		0		dB	
	Loss at 1900Hz	L1H4	1.0	1.5	2.0	dB	
	Loss at 3400Hz	L1H5	49	50		dB	
V.22 bis	Loss at 500Hz	L2L1	24	25		dB	Low band
	Loss at 800Hz	L2L2	2.3	2.8	3.3	dB	
	Loss at 1200Hz	L2L3		0		dB	
	Loss at 1600Hz	L2L4	2.1	2.6	3.1	dB	
	Loss at 2400Hz	L2L5	80	90		dB	
	Loss at 1200Hz	L2H1	80	90		dB	High band
	Loss at 2000Hz	L2H2	0.7	1.2	1.7	dB	
	Loss at 2400Hz	L2H3		0		dB	
	Loss at 2900Hz	L2H4	5.8	6.3	6.8	dB	
	Loss at 3400Hz	L2H5	23	24		dB	

AC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Symbol	MIN	TYP	MAX	Unit	Note
V.23	Loss at 1700Hz	L3T1		0		dB	Transmit
	Loss at 2700Hz	L3T2	3.5	4.0	4.5	dB	
	Loss at 4600Hz	L3T3	45	50		dB	
	Loss at 420Hz	L3R1	55	60		dB	Receive
	Loss at 800Hz	L3R2	3.4	3.9		dB	
	Loss at 1700Hz	L3R3		0	4.4	dB	
	Loss at 2700Hz	L3R4	3.5	4.0		dB	
	Loss at 4600Hz	L3R5	45	50	4.5	dB	
V.29/ V.27 ter	Loss at 100Hz	L9T1		0		dB	Transmit
	Loss at 2400Hz	L9T2	-2.0	-1.5		dB	
	Loss at 4500Hz	L9T3	18	19	-1.0	dB	
	Loss at 100Hz	L9R1	24.5	25.5		dB	Receive
	Loss at 300Hz	L9R2	1.7	2.2		dB	
	Loss at 1700Hz	L9R3		0	2.7	dB	
	Loss at 3500Hz	L9R4	-3.5	-3.0		dB	
	Loss at 4600Hz	L9R5	12	13	-2.5	dB	
V.27ter with backward channel	Loss at 100Hz	L7R1	62	67		dB	Receive
	Loss at 590Hz	L7R2	2.1	2.6		dB	
	Loss at 1700Hz	L7R3		0		dB	
	Loss at 3500Hz	L7R4	-3.5	-3.0		dB	
	Loss at 4600Hz	L7R5	12	13	-2.5	dB	
V.23 V.27ter Backward Channel	Loss at 420Hz	LBT1		0		dB	Transmit
	Loss at 500Hz	LBT2	5.1	5.6		dB	
	Loss at 1280Hz	LBT3	60	65		dB	
	Loss at 100Hz	LBR1	30	31		dB	Receive
	Loss at 300Hz	LBR2	5.7	6.2		dB	
	Loss at 420Hz	LBR3		0		dB	
	Loss at 500Hz	LBR4	5.5	6.0		dB	
	Loss at 1280Hz	LBR5	53	58		dB	

AC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Symbol	MIN	TYP	MAX	Unit	Note
Call Progress Tone BPF	Loss at 100Hz	LCP1	36.6	37.6		dB	
	Loss at 300Hz	LCP2	0.5	1.0	1.5	dB	
	Loss at 500Hz	LCP3		0		dB	
	Loss at 600Hz	LCP4	0.22	0.72	1.22	dB	
	Loss at 1400Hz	LCP5	39	40		dB	
DTMF Tone LPF	Loss at 100Hz	LDF1		0		dB	
	Loss at 1800Hz	LDF2	3.8	4.3	4.8	dB	
	Loss at 3600Hz	LDF3	70	80		dB	
Answer Tone BPF	Loss at 1200Hz	LAT1	30	31		dB	
	Loss at 2200Hz	LAT2		0		dB	
	Loss at 3500Hz	LAT3	29	30		dB	
Line Amplitude EQL	Loss at 500Hz	LEQ1	1.0	1.5	2.0	dB	
	Loss at 1800Hz	LEQ2		0		dB	
	Loss at 3000Hz	LEQ3	-1.7	-1.2	-0.7	dB	
Call Progress Tone Detector		CTDL1	-44			dBmO	V.32
Detect Level		CTDL2	-54			dBmO	except for V.32
Delay		CTDY	30		80	ms	$\frac{1.2}{\sqrt{2}}$ Vrms
Hold Time		CTHT	5		30	ms	
Carrier Detector		CDDL1	-49		-44	dBmO	V.32
Detect Level		CDDL2	-59		-54	dBmO	except for V.32
Delay Time		CDDY	5		20	ms	V.22 bis Carrier
Hold Time		CDHT	5		15	ms	
Hysteresis		CDHY	2			dB	
Answer Tone Detector		ATDL1	-44			dBmO	V.32
Detect Level		ATDL2	-54			dBmO	except for V.32
Delay		ATDY	10		30	ms	2100 Hz 2225 Hz
Hold Time		ATHT	5		20	ms	

AC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	MIN	TYP	MAX	Unit	Note
Transmit Level						
V.21 Low band	TL1L	-12	-11	-10	dBmO	See Figure 11 Level Diagram * Including Guard Tone
V.21 High band	TL1H	-12	-11	-10	dBmO	
V.22 bis Low band	TL2L	-12	-11	-10	dBmO	
V.22 High band*	TL2H	-12	-11	-10	dBmO	
V.23	TL2H	-12	-11	-10	dBmO	
V.29/V.27 ter	TL9T	-12	-11	-10	dBmO	
Harmonic Distortion (Transmit)						
V.21 Low band	TH1L		-65	-60	dB	Measured with Single-tone
V.21 High band	TH1H		-65	-60	dB	
V.22 bis Low band	TH2L		-65	-60	dB	
V.22 bis High band	TH2H		-65	-60	dB	
V.23	TH3T		-65	-60	dB	
V.29/V.27 ter	TH9T		-65	-60	dB	
Harmonic Distortion (Receive)						
V.21 Low band	RH1L		-65	-60	dB	Measured with Single-tone
V.21 High band	RH1H		-65	-60	dB	
V.22 bis Low band	RH2L		-65	-60	dB	
V.22 bis High band	RH2H		-65	-60	dB	
V.23	RH3R		-65	-60	dB	
V.29/V.27 ter	RH9R		-65	-60	dB	

AC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Symbol	MIN	TYP	MAX	Unit	Note
Guard Tone							
Frequency Deviation	1800 Hz	FD18	1799	1800	1801	Hz	
Frequency Deviation	550 Hz	FD55	549	550	551	Hz	
Transmit Level	1800 Hz	TL18	-18	-17	-16	dBmO	
Transmit Level	550 Hz	TL55	-15	-14	-13	dBmO	
Harmonic Distortion	1800 Hz	HD18			-60	dB	
Harmonic Distortion	550 Hz	HD55			-60	dB	
AGC							
Output Level		OLAG	-12	-11	-10	dBr*	
Set-up Time after CD/ON		STAG		15	20	ms	
Set-up Time after Gain Hit		STGH		800		ms	Gain Hit ± 10dB
Output Level deviation		OLDV	-1		1	dB	
Idle Channel Noise							
Transmit Idle Channel Noise		IDNT		-80	-75	dBmO	0 dBmO = $\frac{1.2}{\sqrt{2}}$ Vrms
Receive Idle Channel Noise		IDNR		-80	-75	dBmO	

* See Figure 23

AC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Symbol	MIN	TYP	MAX	Unit	Note
Filter Response (Relative)							
V.32	Loss at 100Hz	L3T1		0		dB	Transmit
	Loss at 1800Hz	L3T2		0		dB	
	Loss at 3600Hz	L3T3	11	12		dB	
	Loss at 4200Hz	L3T4	55	60		dB	
	Loss at 100Hz	L3R1	35	40		dB	Receive
	Loss at 300Hz	L3R2	30	35		dB	
	Loss at 1800Hz	L3R3		0		dB	
	Loss at 2700Hz	L3R4		0		dB	
	Loss at 3600Hz	L3R5	30	35		dB	
	Loss at 4200Hz	L3R6	55	60		dB	
Filter Response (Relative)							
V.32 notch	Loss at 600Hz	L3N1		0		dB	1800 Hz notch Originate
	Loss at 1800Hz	L3N2	55	60		dB	
	Loss at 3000Hz	L3N3		0		dB	
	Loss at 600Hz	L3N4	55	60		dB	600/3000 Hz notch Answer
	Loss at 1200Hz	L3N5	2.5	3.0	3.5	dB	
	Loss at 1800Hz	L3N6		0		dB	
	Loss at 2400Hz	L3N7	1.0	1.5	2.0	dB	
	Loss at 3000Hz	L3N8	55	60		dB	
Transmit Level							
V.32 Transmit		TL32	-12	-11	-10	dBmO	Multi-tone
Harmonic Distortion							
V.32 Transmitter		TH32			-80	dBmO	Measured(*) with Multi-tone
V.32 Receiver		RH32			-80	dBmO	

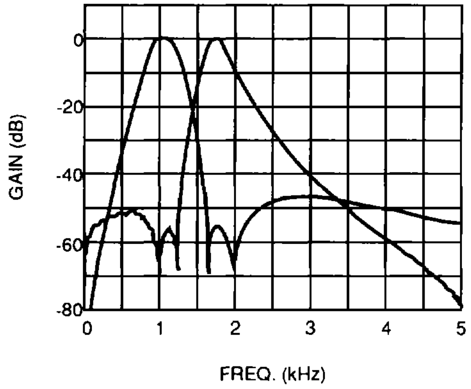


Figure-3 CCITT V.21 Receive BPF

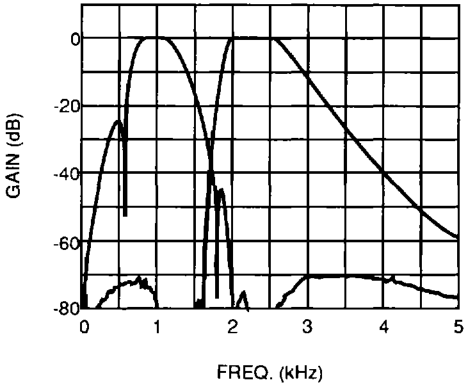


Figure-4 CCITT V.22 Receive BPF

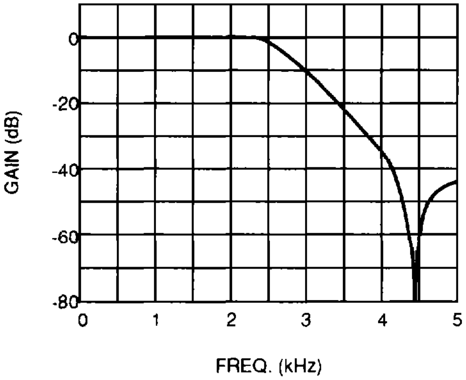


Figure-5 CCITT V.23 Transmit LPF

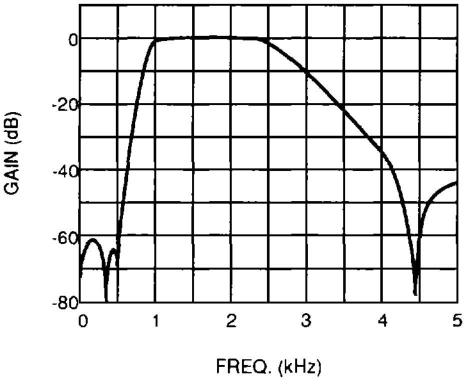


Figure-6 CCITT V.23 Receive BPF

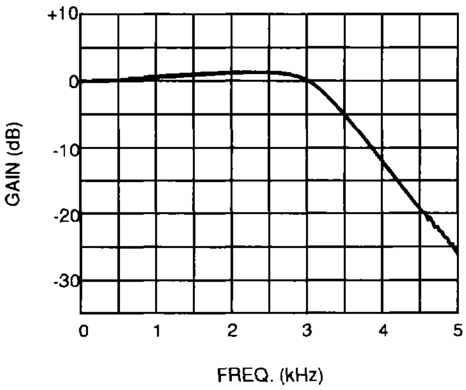


Figure-7 CCITT V.29/V.27ter Transmit LPF

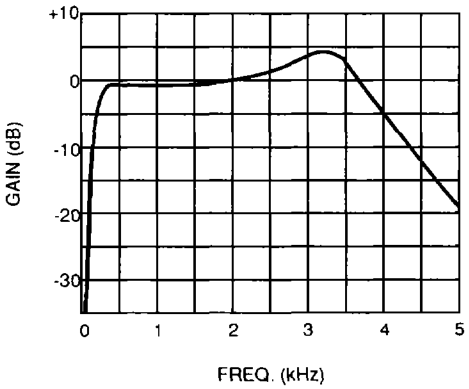


Figure-8 CCITT V.29/V.27ter Receive BPF

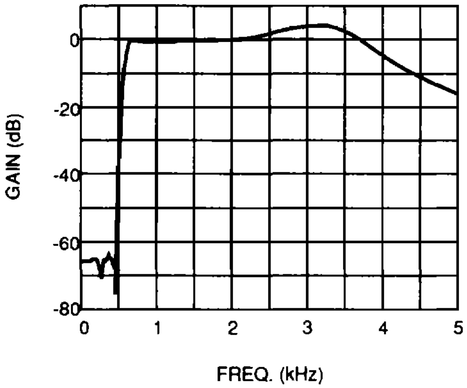


Figure-9 CCITT V.27ter Receive BPF with backward channel

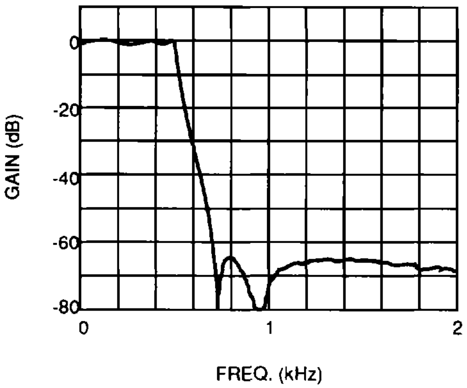


Figure-11 CCITT V.23/V.27ter Backward Transmit

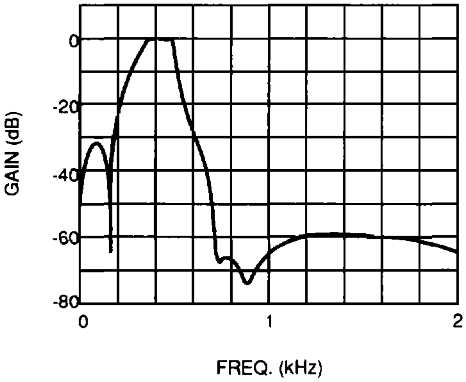


Figure-12 CCITT V.23/V.27ter Backward Receive

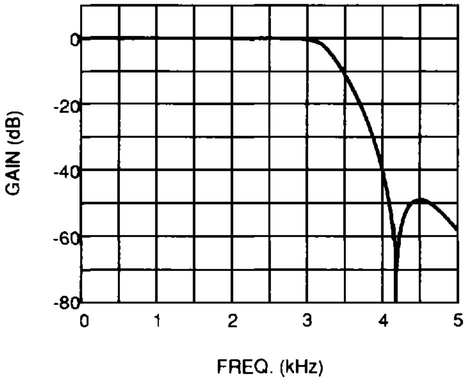


Figure-13 V.32 Transmit LPF

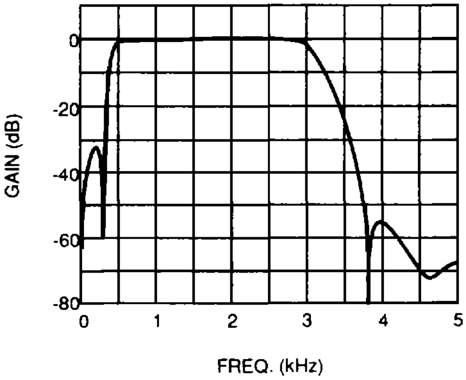


Figure-14 V.32 Receive BPF

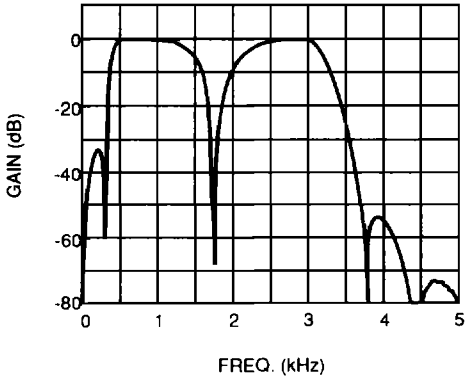


Figure-15 V.32 Receive1800HZ Notch (Originate)

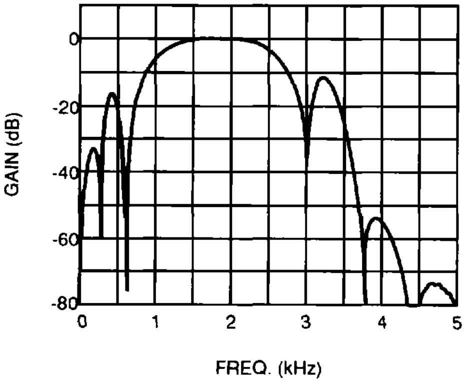


Figure-16 V.32 Receive 600/3000Hz Notch (Answer)

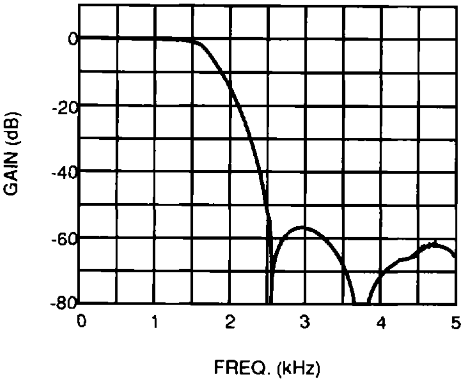


Figure-17 DTMF Tone LPF

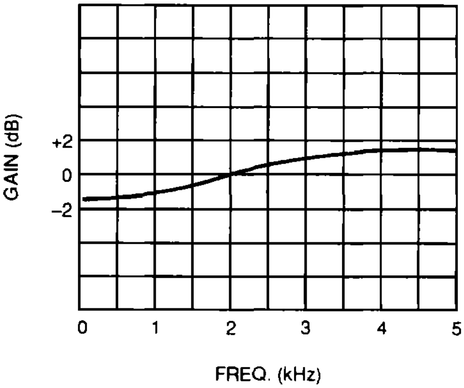


Figure-18 Amplitude EQL

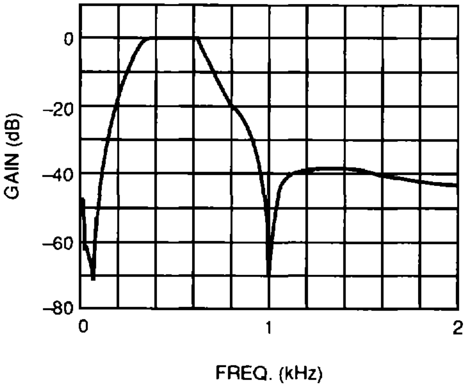


Figure-19 Call Progress Tone BPF

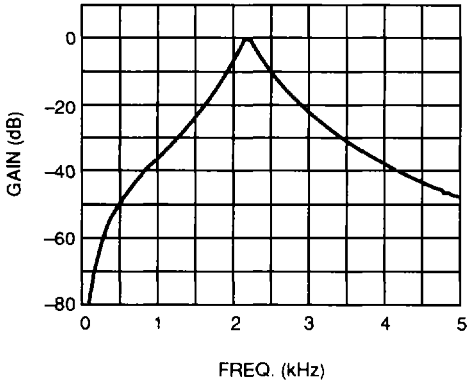


Figure-20 Answer Tone BPF

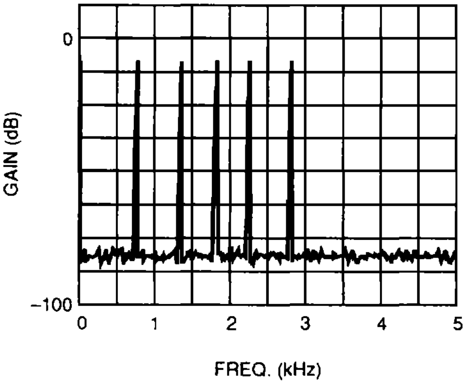


Figure-21 V.32 Transmit Harmonic Distortion

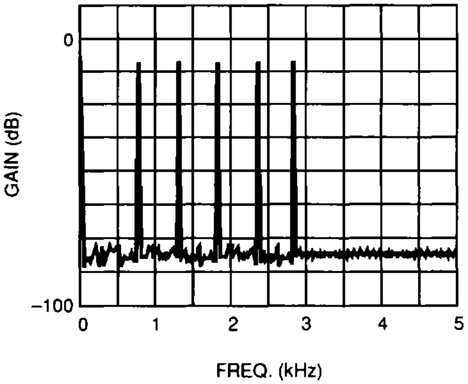
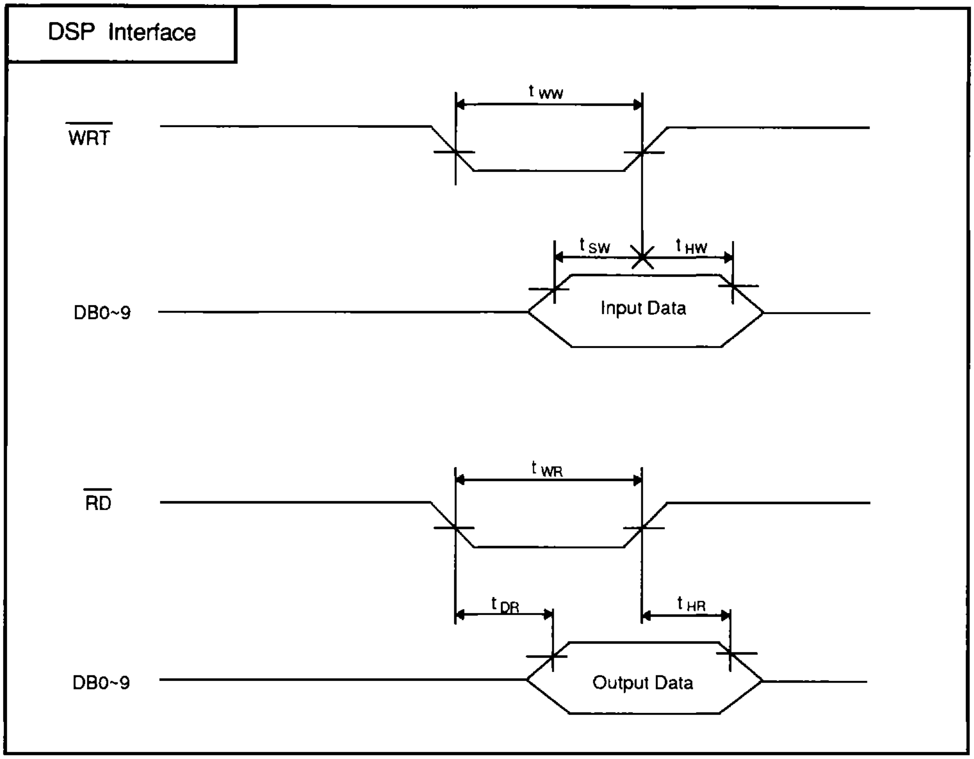


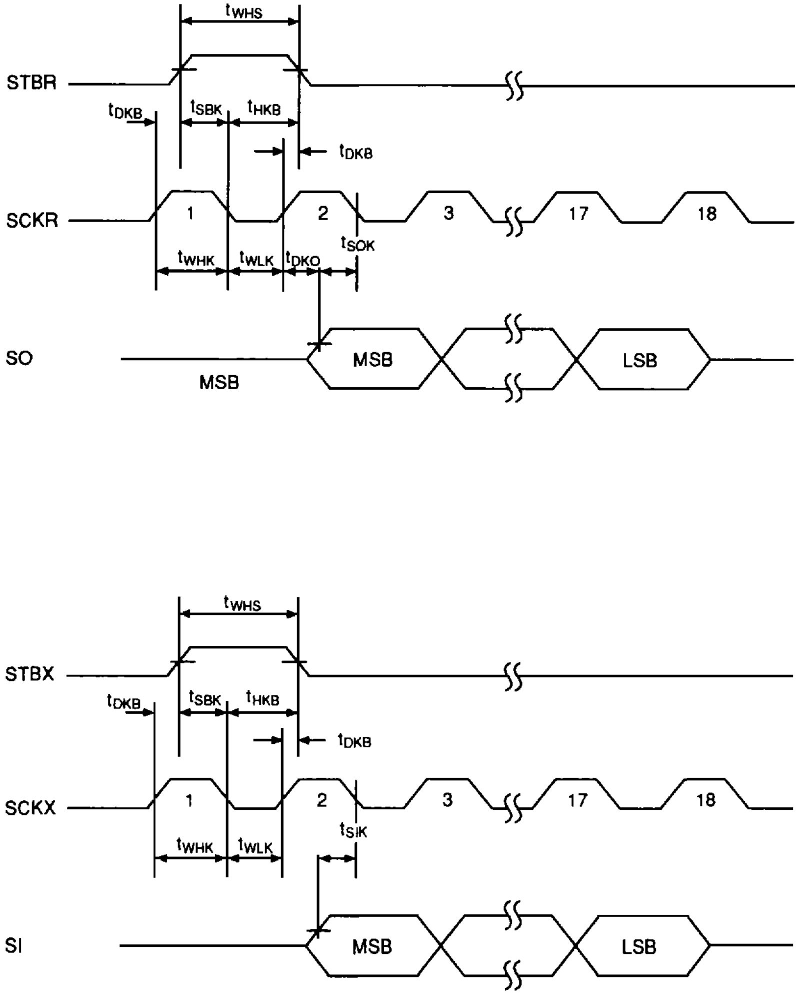
Figure-22 V.32 Receive Harmonic Distortion

- TIMING DIAGRAMS

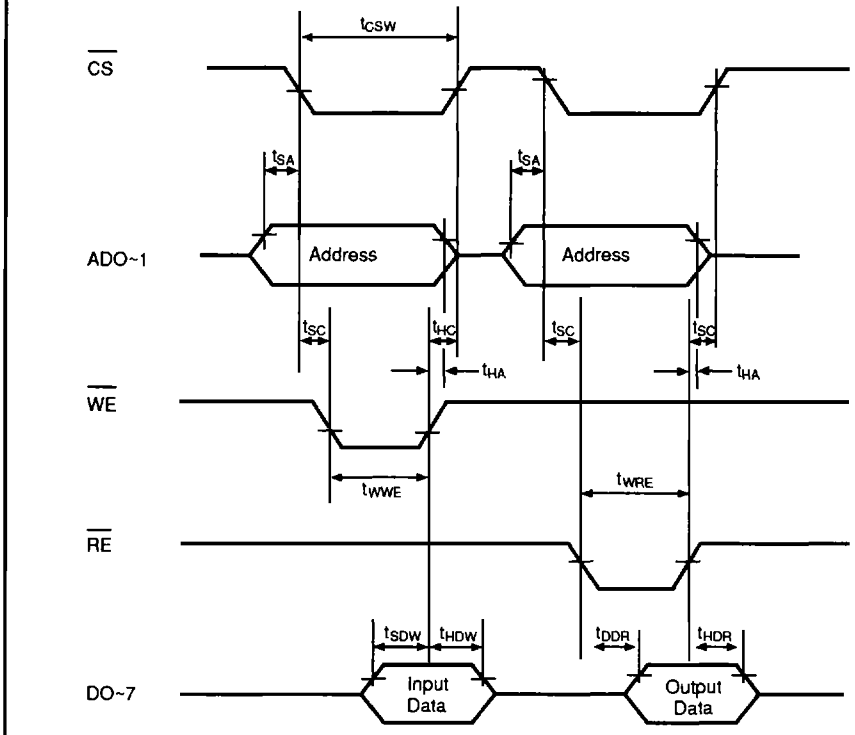


Symbol	Description	MIN	TYP	MAX	Unit
t_{WW}	$\overline{WRT}$ pulse width	100			ns
t_{SW}	DB0~9 setup before $\overline{WRT}$ ↑	20			ns
t_{HW}	DB0~9 hold after $\overline{WRT}$ ↑	0			ns
t_{WR}	RD pulse width	100			ns
t_{DR}	DB0~9 delay from $\overline{RD}$ ↓			50	ns
t_{HR}	DB0~9 hold after $\overline{RD}$ ↑	0			ns

DSP Interface



MCU Interface



Symbol	Description	MIN	TYP	MAX	Unit
t_{WHB}	STBR/STBX pulse width	771.4	771.6	771.8	ns
t_{DKB}	STBR/STBX delay after SCKR/SCKX ↑	-40		60	ns
t_{SBK}	STBR/STBX setup before SCKR/SCKX ↓	325.7		425.9	ns
t_{HKB}	STBR/STBX hold after SCKR/SCKX ↓	345.7		445.9	ns
t_{WHK}	SCKR/SCKX pulse width	385.7	385.8	385.9	ns
t_{WLK}	SCKR/SCKX pulse width	385.7	385.8	385.9	ns
t_{DKO}	SO delay from SCKR ↑			60	ns
t_{SOK}	SO setup before SCKR↓	325.7			ns
t_{SIK}	SI setup before SCKX ↓	20			ns

Symbol	Description	MIN	TYP	MAX	Unit
t_{SA}	AD0~1 setup before $\overline{CS}$↓	20			ns
t_{SC}	$\overline{CS}$ setup before $\overline{WE/RE}$↓	20			ns
t_{HC}	$\overline{CS}$ hold after $\overline{WE/RE}$↑	0			ns
t_{HA}	AD0~1 hold after $\overline{WE/RE}$↑	0			ns
t_{WWE}	$\overline{WE}$ pulse width	100			ns
t_{WRE}	$\overline{RE}$ pulse width	100			ns
t_{SDW}	D0~7 setup before $\overline{WE}$↑	20			ns
t_{HDW}	D0~7 hold after $\overline{WE}$↑	0			ns
t_{DDR}	D0~7 delay from $\overline{RE}$ ↓			50	ns
t_{HDR}	D0~7 hold after $\overline{RE}$↑	0			ns
t_{CSW}	$\overline{CS}$ pulse width	140			ns

Level Diagram

Figure 23 shows the Level Diagram of MSM6994.

With digital data, maximum digital signal power 0 dBr means that the allowance of the digital peak code is as below.

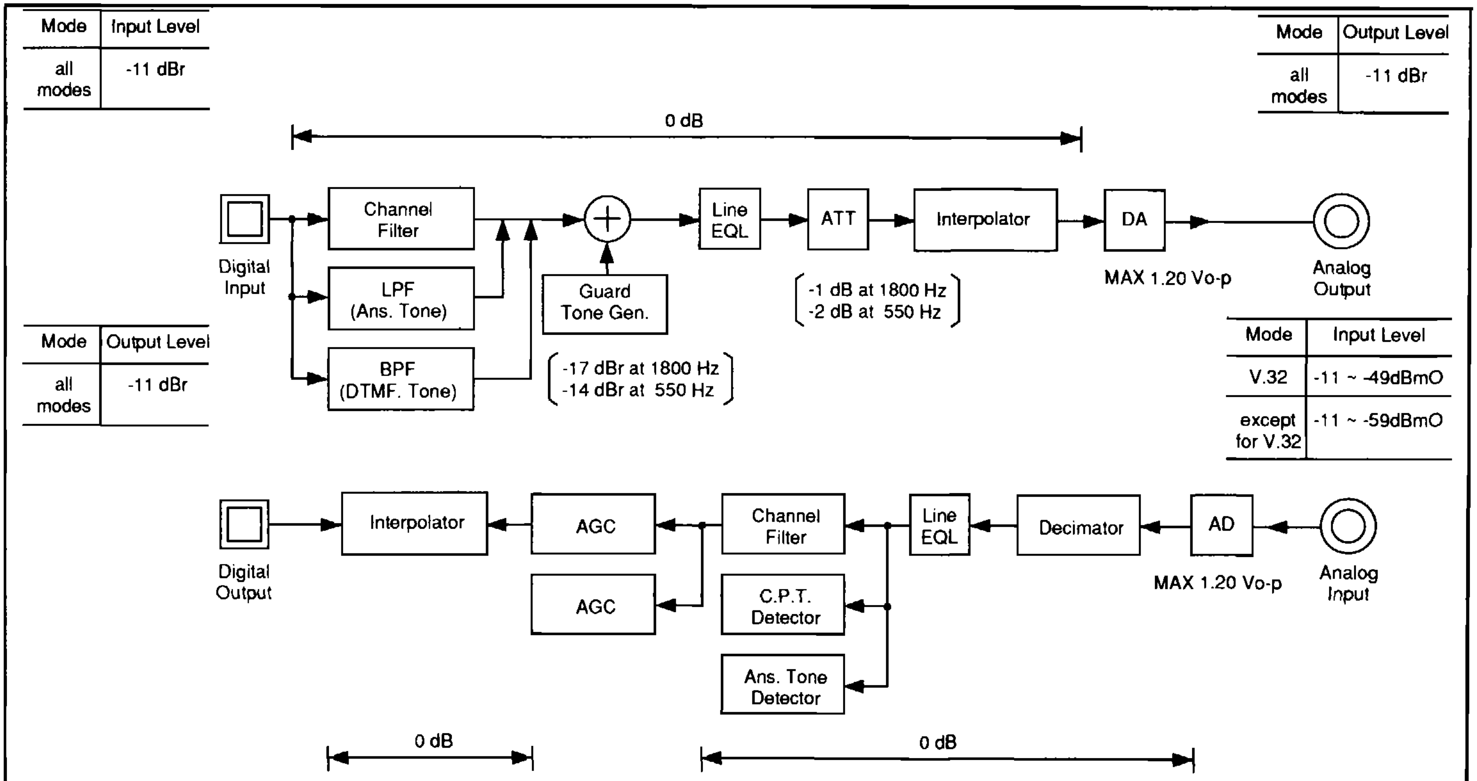
	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Max (peak)	0	1	1	1	1	1	1	1	1	1
Min (peak)	1	0	0	0	0	0	0	0	0	0

The rms digital signal power corresponds to the value of the peak code multiplied by $1/\sqrt{2}$. The lefthand-side table of Figure 23 shows the typical digital signal level for each mode.

As for analog signal level, maximum analog signal power 0 dbmO means that the allowance of the analog peak voltage is 1.20 V0-p and the rms power is $1.2/\sqrt{2}$ Vrm.

The righthand-side table of Figure 23 shows the typical analog signal level for each mode.

Please remember that 11 dB of peak margin should be considered for V.22 bis or V.29 mode, respectively.



Mode	Input Level
all modes	-11 dBr

Mode	Output Level
all modes	-11 dBr

Mode	Output Level
all modes	-11 dBr

Mode	Input Level
V.32	-11 ~ -49dBmO
except for V.32	-11 ~ -59dBmO

		Peak Code									
		DB9									CB0
0 dBr	MAX	0	1	1	1	1	1	1	1	1	1
	MIN	1	0	0	0	0	0	0	0	0	0

Note: $0\text{dBmO} = \frac{1.2}{\sqrt{2}}$ Vrms

Figure 23 Level Diagram

Application

The MSM6994 is designed to be used in conjunction with a microprocessor which utilizes the controller and a digital signal processor as a modulator/demodulator. Figure 24 shows the typical configuration for a multi-standard modem using the MSM699215 as the digital signal processor. The MSM6994 will communicate mod/demod data with the MSM699215 through parallel (DSP) and Serial I/O interfaces, and will be controlled by using the MCU interface in the same manner as the MSM699215. A dedicated MCU monitors and interprets the commands included in the data stream from the terminal, and takes control action in response to these commands, and transfers TXD and RXD at the proper time to and from the MSM699215.

Figure 25 shows the operation of an echo cancelling modem processed by the MSM6994. The replica processor will generate the near-end echoes, and transmit its replica to the MSM6994. The MSM6994 will substract this replica from incoming signal and send back its error to the replica processor through 16 bits serial I/O interface. The mod/demod data will then be transferred by using a parallel (DSP) interface between MOD/DEM processors and the MSM6994.

Figure 26 shows the typical example of the phone line interface. The MSM6994 operates with a single 5.0 V power supply, therefore the analog signal will be interfaced to the line based on AG reference by buffer amplifiers which also operate with a single 5.0 V power supply.

The MSM6994 is designed so as to be used in conjunction with not only the MSM699215 (OKI original DSP), but also many other well-known standard DSPs.

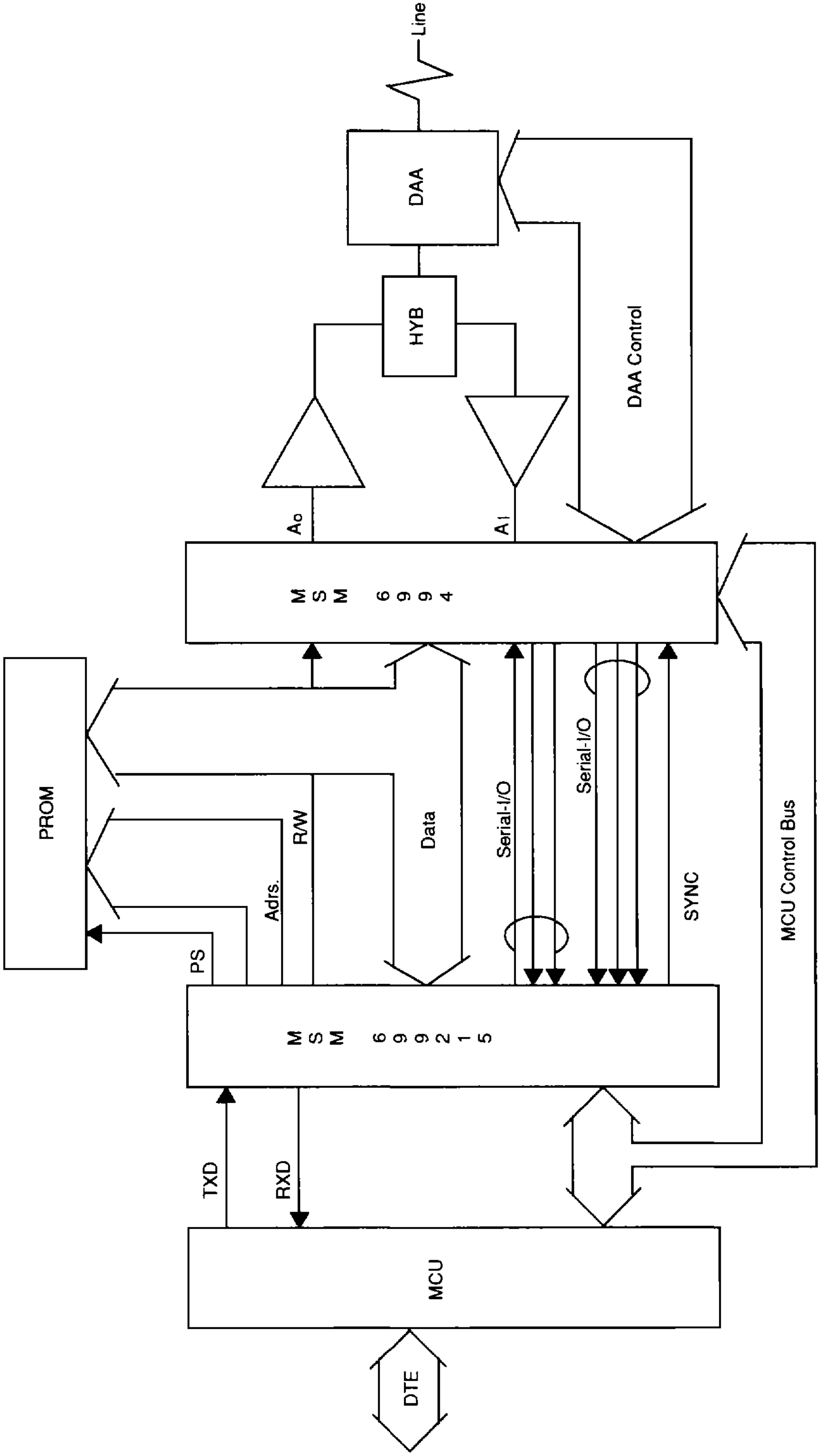


Figure 24 System configuration for Multi-Standard Modem

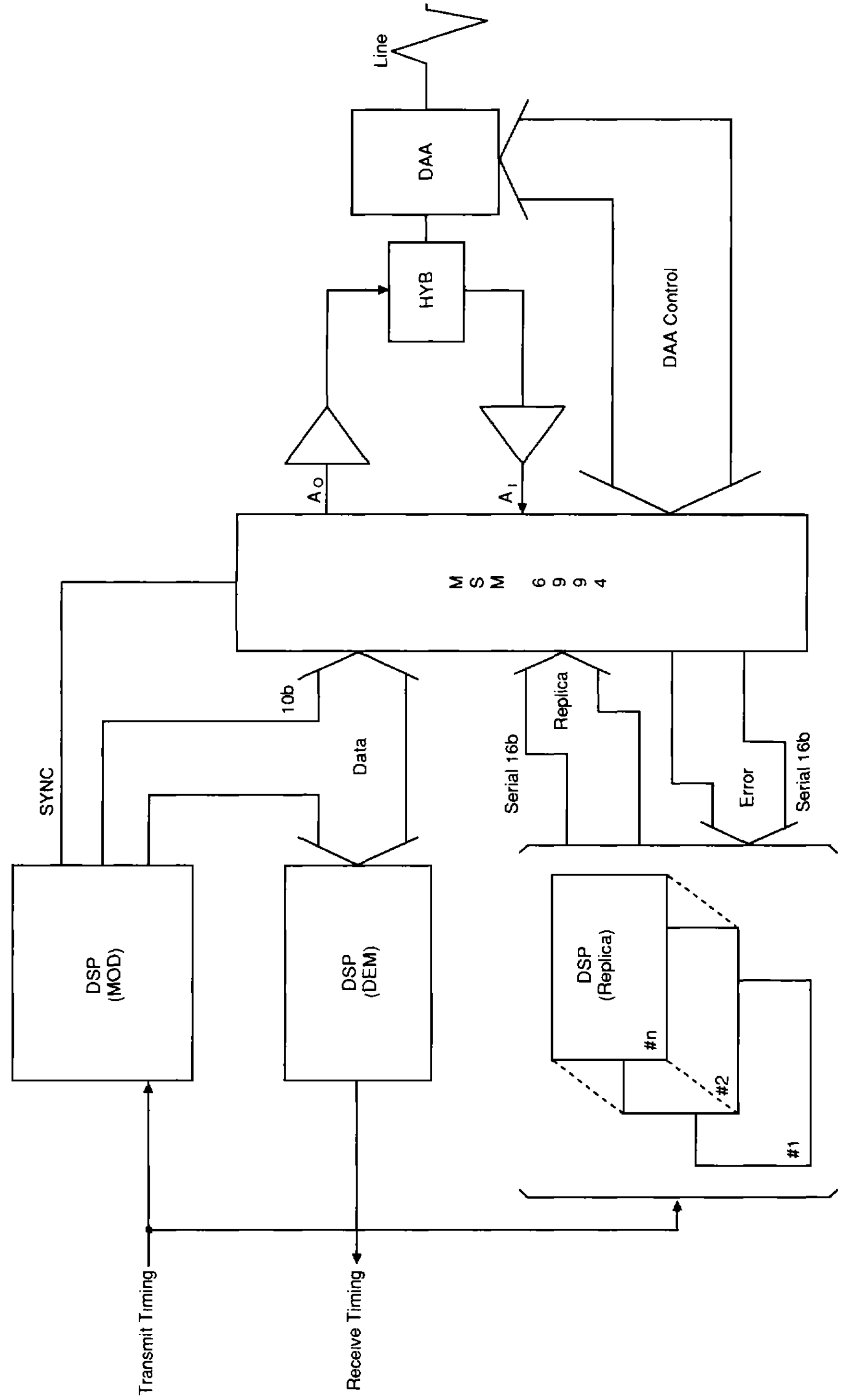
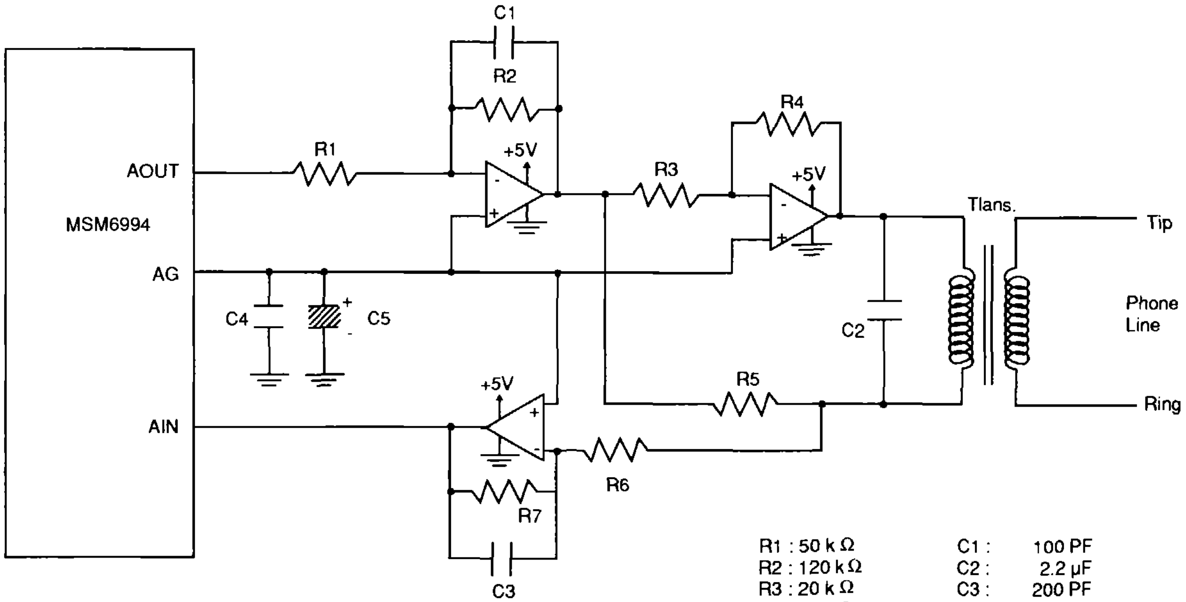


Figure 25 System Configuration for Echo Cancelling Modem



R1 : 50 k Ω
R2 : 120 k Ω
R3 : 20 k Ω
R4 : 20 k Ω
R5 : 560 Ω
R6 : 50 k Ω
R7 : 75 k Ω

C1 : 100 PF
C2 : 2.2 μF
C3 : 200 PF
C4 : 0.1 μF
C5 : 22 μF

Tlans. : 600 : 600 Ω

Figure-26 Line Interface

V.32 Application

Fig. 27 shows the system configuration of V.32 echo cancelling Modem using MSM6994. A 7.2 KHz sampling rate should be used for the modulation DSP and the replica generation DSP.

A 9.6 KHz sampling rate will be used for the demodulation DSP. MSM6994 fetches both transmit data of 16 bits and replica data of 16 bits by using the serial input interface during a period of the 7.2 KHz sampling rate, so the serial input frame pulse of STBX will appear in twice during one sampling rate.

After fetching the replica data, the MSM6994 routes the error word of 16 bits, which is derived by subtracting the replica data from incoming signal, to the replica DSP through the serial output interface. The demodulation DSP can fetch the real incoming signal through the parallel 10 bit interface, whose output will be held on a steady level by the AGC procedure in MSM6994 program.

Fig. 28 shows the timing diagram of the serial interface. The An indicates the serial input timing of the 16 bit transmit data, the Bn indicates the serial input timing of the 16 bit replica data. The Mn denotes the 16 bits error data the En means the 16 bits error data.

The stored data in the SIB is routed to the internal register at the next serial input internal which is caused by executing the SI instruction in MSM6994 program.

Therefore, the transmit data being input at An timing will be provided to the transmit LPF within 1 STM, however the replica data being input at Bn internal will be used at the next STM for its substraction. Hence, there is 1 STM of absolute delay between the replica input timing and the substraction timing.

Table 2 shows the timing specification of An, Bn and Cn.

Table 2 Timing Specification

Item	MIN	TYP	MAX	Unit	Note
An - 0	0		5	μs	
Cn - An	22		27	μs	
Bn - An	18		23	μs	STBX Interval

Please note that the shift clock of the serial interface is 1.296 MHz, therefore it takes about 13 μsec to shift the 16 bits of serial data into the serial input buffer.

Fig. 29 shows the example of V.32 construction using MSM6994 combining with TMS320 family DSP.

When two DSPs are used, one is for Modulation/Demodulation and the other for replica generation. The replica generation is synchronized with the modulation procedure.

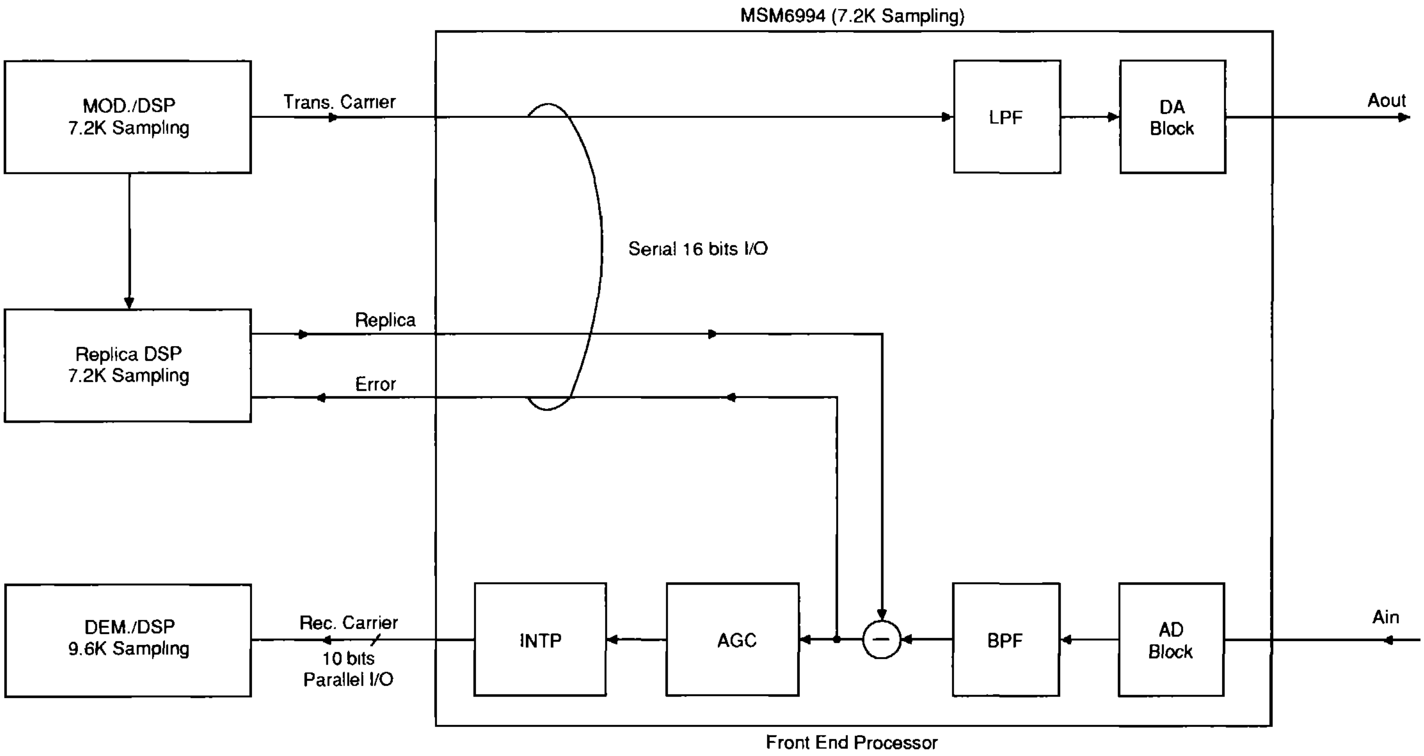
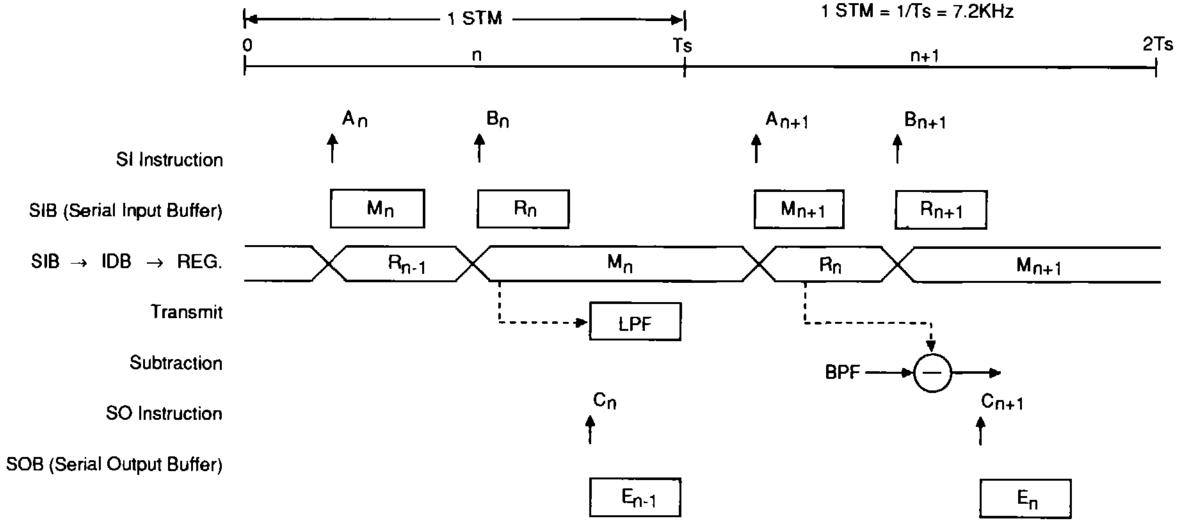


Figure 27 System Configuration



$0\,\mu s < A_n\text{-}0 < 5\,\mu s$
$22\,\mu s < C_n\text{-}A_n < 27\,\mu s$
$18\,\mu s < B_n\text{-}A_n < 23\,\mu s$

Figure 28 Timing Diagram

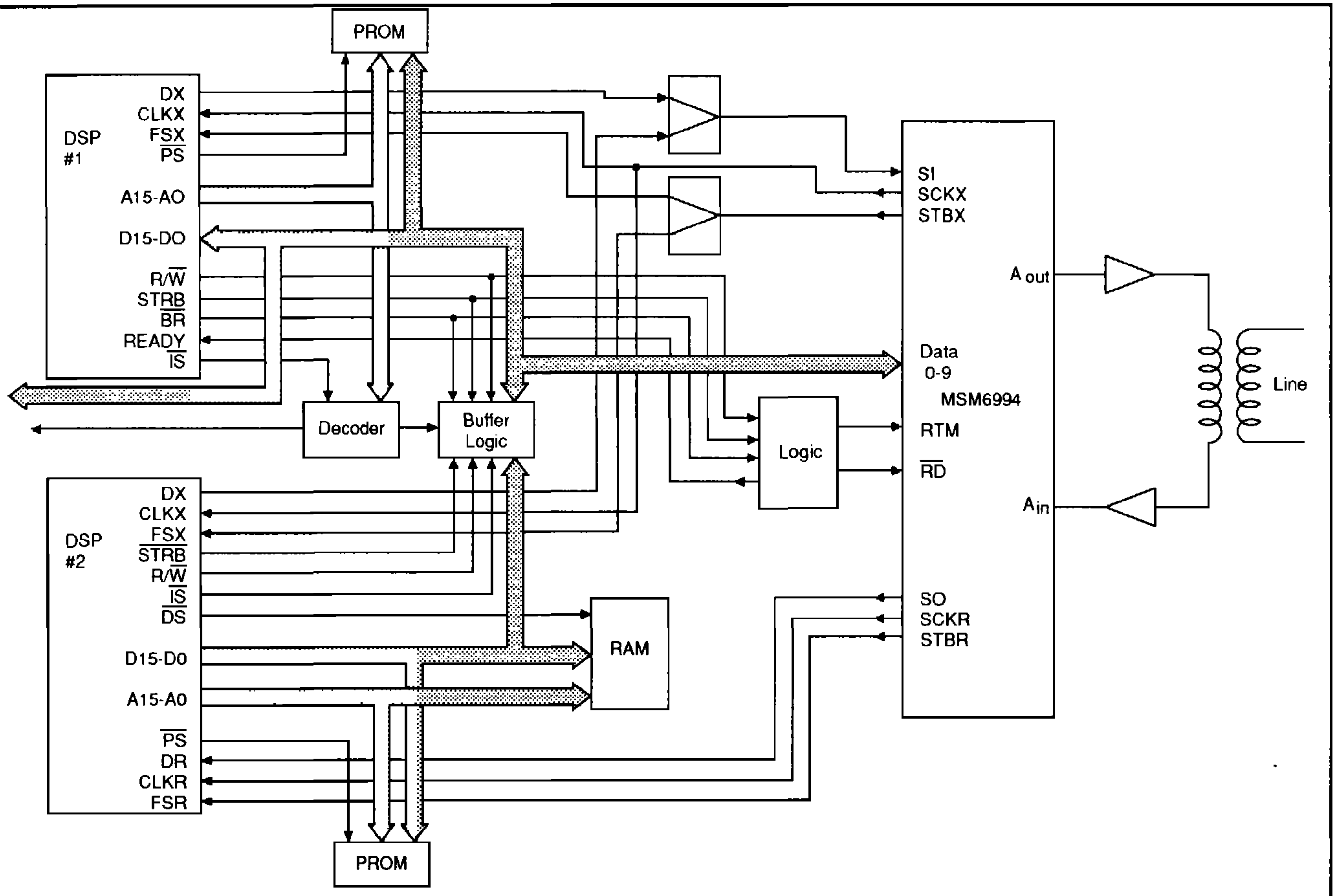


Figure 29 V.32 Application