National Semiconductor

DM54L71/DM74L71 AND-Gated Master-Slave R-S Flip-Flop with Preset, Clear and Complementary Outputs

General Description

This device contains a positive pulse triggered master-slave R-S flip-flop with complementary outputs. Multiple R and S inputs are ANDed together to produce the internal R and S functions for the flip-flop. The R and S data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive going transition of the clock, the data from the AND gates is transferred to the master. While the clock is high the AND gate inputs are disabled. On the negative transition of the clock the data is transferred from the master to the slave. The R and S inputs must be held constant while the clock is high. Data is transferred to the output on the falling edge of the clock pulse. A low level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

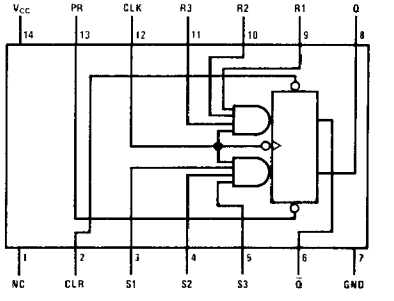
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6628-1

DM54L71 (J) DM74L71 (N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	S(1)	R(1)	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_O	$\bar{Q}_O$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Indeterminate	

Note 1: S = (S1)(S2)(S3), R = (R1)(R2)(R3)

H = High Logic Level

X = Low or High Logic Level

L = Low Logic Level

⎍ = Positive pulse. The R and S inputs must be held constant while the clock is high. Data is transferred to the output on the falling edge of the clock pulse.

Q_O = The level of Q before the indicated input conditions were established.

* = This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs returned to their inactive (high) level.

Recommended Operating Conditions

Sym	Parameter		DM54L71			DM74L71			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage	Clock			0.6			0.6	V
		Others			0.7			0.7	
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency		0		6	0		6	MHz
t_W	Pulse Width	Clock High	100			100			ns
		Clock Low	100			100			
		Preset Low	100			100			
		Clear Low	100			100			
t_{SU}	Input Setup Time (Note 1)		0↑			0↑			ns
t_H	Input Hold Time (Note 1)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbols (↑, ↓) indicate the edge of the clock pulse used for reference: ↑ for rising edge, ↓ for falling edge.

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Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 5.5V	R, S			100	mA
			Clear			200	
			Preset			200	
			Clock			200	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	R, S			10	μA
			Clear			20	
			Preset			20	
			Clock			−200	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	R, S			−0.18	mA
			Clear			−0.36	
			Preset			−0.36	
			Clock			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			0.76	1.44	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		6	11		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		35	75	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		60	150	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		35	75	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		60	150	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$	10	35	75	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$	10	60	150	ns