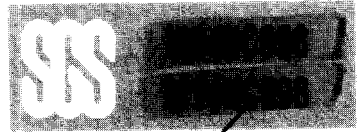


HS-C²MOS™ INTEGRATED CIRCUITS

Apr 1985



PRODUCT PREVIEW

U/D DECADE COUNTER/REGISTER (3-STATE)

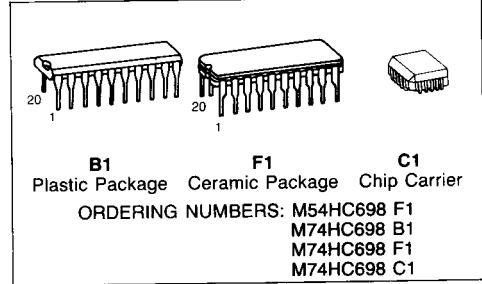
DESCRIPTION

The M54/74HC698 is a high speed CMOS U/D DECADE COUNTER/REGISTER (3-STATE) fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device incorporates synchronous up/down counter, four-bit D-type register, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The up/down counter is programmable from the data inputs and feature enable \bar{P} and enable \bar{T} and a ripple-carry output for easy expansion. The register/counter select input, R/C, selects the counter when low or the register when high for the three-state outputs, QA, QB, QC, and QD.

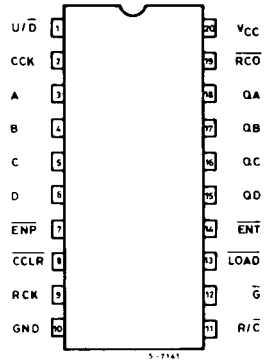
Both the counter clock CCK and register clock RCK are positive-edge triggered. The counter clear CCLR is active low and is, synchronous. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

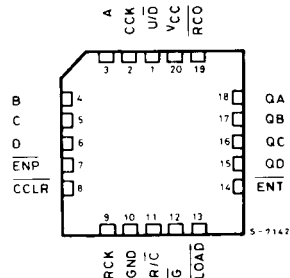
- Low Power Dissipation
 $I_{CC} = 4 \mu A$ (Max.) at $T_A = 25^\circ C$
- High Noise Immunity
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Output Drive Capability
10 LSTTL Loads
- Symmetrical Output Impedance
 $|I_{OH}| = I_{OL} = 4 \text{ mA}$ (Min.)
- Balanced Propagation Delays
 $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range
 $V_{CC} \text{ (opr)} = 2V \text{ to } 6V$
- Pin and Function compatible
with 54/74LS698



PIN CONNECTIONS (top view)



CHIP CARRIER





M54HC698
M74HC698

TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
CCLR	LOAD	ENP	ENT	CCK	U/D	RCK	R/C	G	QA	QB	QC	QD	
*	*	*	*	*	*	*	*	H	Z	Z	Z	Z	High Impedance
L	*	*	*		*	*	L	L	L	L	L	L	Clear Counter
H	L	*	*		*	*	L	L	a	b	c	d	Load Counter
H	H	H	*		*	*	L	L	No Change			No count	
H	H	*	H		*	*	L	L	No Change			No count	
H	H	L	L		H	*	L	L	Count up			Count up	
H	H	L	L		L	*	L	L	Count Down			Count Down	
*	*	*	*		*	*	L	L	No Change			No count	
*	*	*	*	*	*		H	L	a'	b'	c'	d'	Load Register
*	*	*	*	*	*		H	L	No change			No Load	

* : Don't care

Z : High Impedance

a-d : The level of steady state inputs at inputs A through D respectively.

a'-d' : The level of steady state outputs at internal counter outputs QA' through QD' respectively.

RCO FUNCTION: $RCO = (UP \cdot QA \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QB} \cdot \overline{QC} \cdot \overline{QD} \cdot ENT)$

INPUT AND OUTPUT EQUIVALENT CIRCUIT

