10 Device Specifications

10.1 Absolute Maximum Ratings

Ambient temperature under bias (T_A) ..... 0 °C to + 70 °C
Storage temperature (T_{ST}) ..... – 65 °C to + 150 °C

Voltage on V_{CC} pins with respect to ground (V_{SS}) ..... – 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}) ..... – 0.5 V to V_{CC} + 0.5 V

Input current on any pin during overload condition ..... – 10 mA to + 10 mA
Absolute sum of all input currents during overload condition ..... | 100 mA |

Power dissipation ..... TBD

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.*

10.2 DC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V; T_A = 0 to + 70 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$, RESET)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage (RESET)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (except $\overline{EA}$, RESET, XTAL1)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL1	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	
Input high voltage to $\overline{EA}$, RESET	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage					
Ports 1, 2, 3 (except P1.2, P1.4)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Port 0, ALE, $\overline{PSEN}$	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
P1.2 / P1.4 pull-down transistor resistance	R_{DSon}	–	120	Ω	V_{OL} = 0.45 V
Output high voltage					
Ports 1, 2, 3	V_{OH}	2.4	–	V	I_{OH} = – 80 µA
		0.9 V_{CC}	–	V	I_{OH} = – 10 µA
Port 0 in ext. bus mode, ALE, $\overline{PSEN}$	V_{OH1}	2.4	–	V	I_{OH} = – 800 µA
		0.9 V_{CC}	–	V	I_{OH} = – 80 µA
P1.2 / P1.4 pull-up transistor resistance	R_{DSon}	–	120	Ω	V_{OH} = 0.9 V_{CC}
Logic 0 input current (Ports 1, 2, 3)	I_{IL}	– 10	– 50	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (Ports 1, 2, 3)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Maximum output low current per pin (Ports 0, 1, 2, 3)	I_{OLM}	–	5	mA	$V_{OL} \leq$ 1 V
Input leakage current Port 0 (if $\overline{EA}$=0), $\overline{EA}$, P1.2, P1.3, P1.5 as SSC inputs	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance [7]	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Power supply current:					
SAB-C511/C511A/C513/C513A					
Active mode, 8 MHz [6]	I_{CC}	–	TBD	mA	V_{CC} = 5 V, [4]
Idle mode, 8 MHz [6]	I_{CC}	–	TBD	mA	V_{CC} = 5 V, [5]
Power Down Mode	I_{PD}	–	50	µA	V_{CC} = 2 ... 5.5 V, [3]
SAB-C513A-H					
Active mode, 8 MHz [6]	I_{CC}	–	TBD	mA	V_{CC} = 5 V, [4]
Idle mode, 8 MHz [6]	I_{CC}	–	TBD	mA	V_{CC} = 5 V, [5]
Power Down Mode	I_{PD}	–	50	µA	V_{CC} = 2 ... 5.5 V, [3]

Notes:

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall bellow the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (Power Down Mode) is measured under following conditions:
$\overline{EA}$ = Port0 = V_{CC}; RESET = V_{SS}; XTAL2 = N.C.; XTAL1 = V_{SS}; all other pins are disconnected.

4) I_{CC} (active mode) is measured with:
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
$\overline{EA}$ = Port0 = RESET = V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS}; Port0 = V_{CC}; all other pins are disconnected;

6) $I_{CC\,Max}$ at other frequencies is given by:

SAB-C511/C511A/C513/C513A :	Active mode:	TBD
	Idle mode:	TBD
SAB-C513A-H :	Active mode:	TBD
	Idle mode:	TBD

where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

7) This parameter is periodically sampled and not 100% tested.

10.3 AC Characteristics (applies to all SAB-C511/513 Family Microcontrollers)

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V T_A = 0 °C to + 70 °C

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

10.3.1 Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		8 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 8 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	210	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	85	–	$t_{CLCL} - 40$	–	ns
Address hold after ALE	t_{LLAX}	102	–	$t_{CLCL} - 23$	–	ns
ALE low to valid instr in	t_{LLIV}	–	400	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	100	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	340	–	$3t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	–	275	–	$3t_{CLCL} - 100$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	–	105	–	$t_{CLCL} - 20$	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	100	–	$t_{CLCL} - 25$	–	ns
Address to valid instr in	t_{AVIV}	–	510	–	$5t_{CLCL} - 115$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the SAB-C511/513 microcontrollers to devices with float times up to 100 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

10.3.2 External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		8 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 8 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	650	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	650	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	215	–	$2t_{CLCL} - 35$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	460	–	$5t_{CLCL} - 165$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	180	–	$2t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	–	850	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	960	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	325	425	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	370	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	85	165	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	75	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	725	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	75	–	$t_{CLCL} - 40$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

10.3.3 SSC Interface Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock Cycle Time : Master Mode	t_{SCLK}	1	–	µs
Slave Mode	t_{SCLK}	900	–	ns
Clock high time	t_{SCH}	400	–	ns
Clock low time	t_{SCL}	400	–	ns
Data output delay	t_{D}	–	100	ns
Data output hold	t_{HO}	0	–	ns
Data input setup	t_{S}	100	–	ns
Data input hold	t_{HI}	100	–	ns
TC bit set delay	t_{DTC}	–	16 t_{CLCL}	ns

10.3.4 External Clock Characteristics

Parameter	Symbol	Limit Values Variable Clock Freq. = 3.5 MHz to 8 MHz		Unit
		min.	max.	
Oscillator period	t_{CLCL}	125	290	ns
High time	t_{CHCX}	30	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	30	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	30	ns
Fall time	t_{CHCL}	–	30	ns

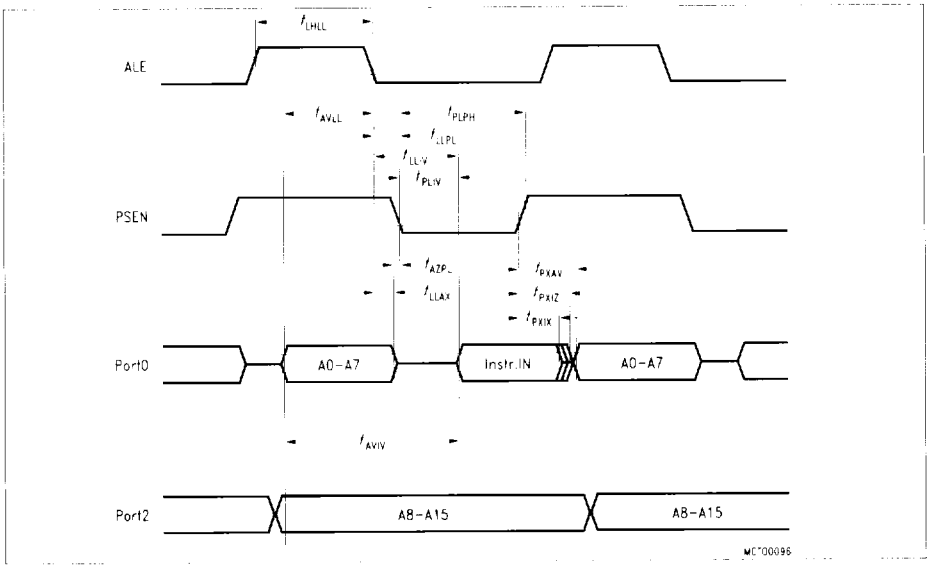


Figure 10-1
Program Memory Read Cycle

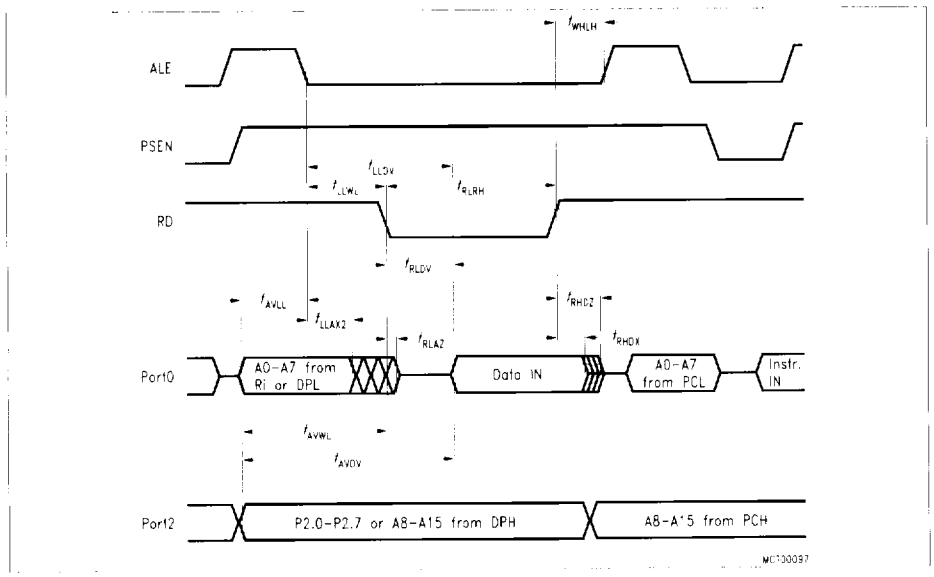


Figure 10-2
Data Memory Read Cycle

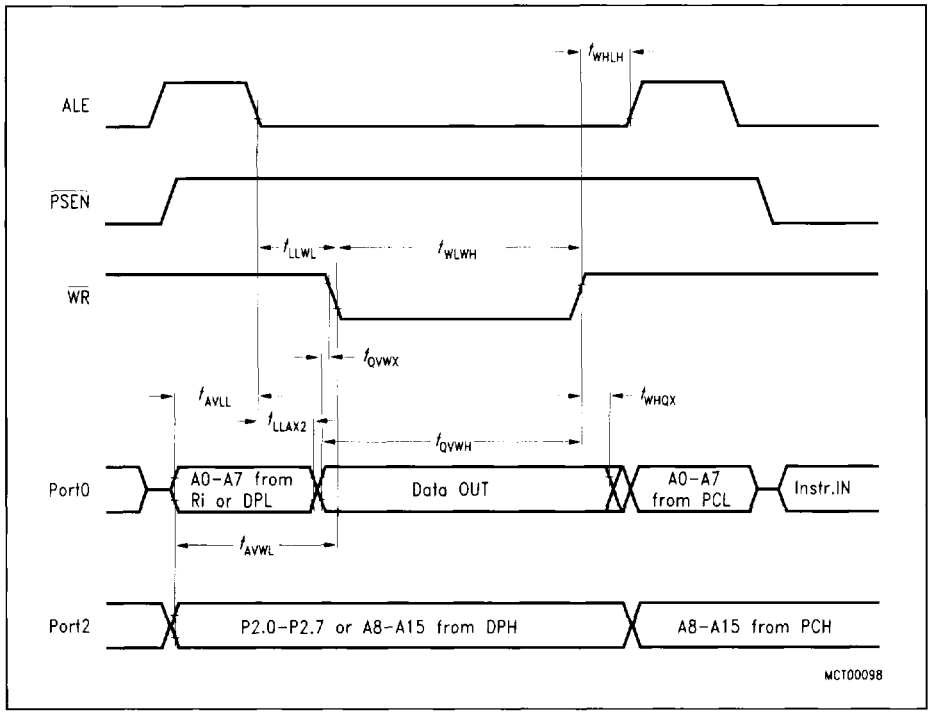
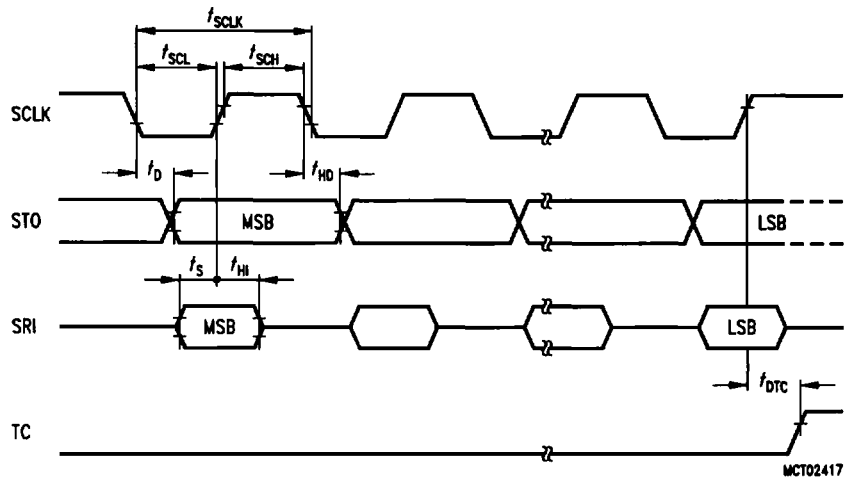


Figure 10-3
Data Memory Write Cycle



Notes: Shown is the data/clock relationship for CPOL = CPHA = 1. The timing diagram is valid for the other cases accordingly.

In the case of slave mode and CPHA = 0, the output delay for the MSB applies to the falling edge of $\overline{SLS}$ (if transmitter is enabled).

In the case of master mode and CPHA = 0, the MSB becomes valid after the data has been written into the shift register, i.e. at least one half SCLK clock cycle before the first clock transition.

Figure 10-4
SSC Timing

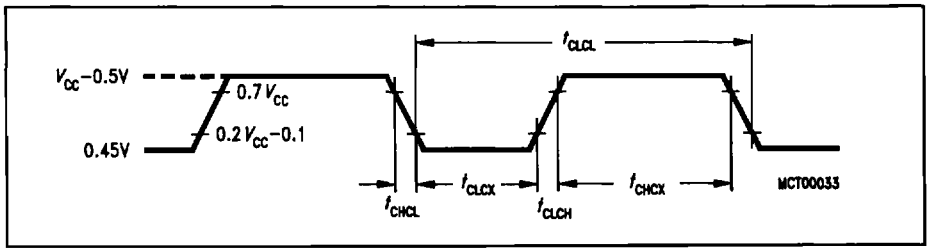
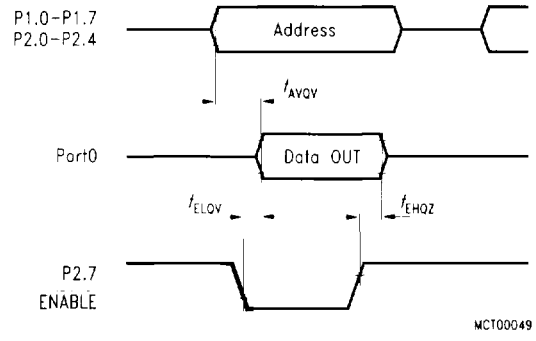


Figure 10-5
External Clock Drive Drive at XTAL2

10.3.5 ROM Verification Characteristics (only SAB-C511/C511A/C513/C513A)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	$48t_{CLCL}$	ns
ENABLE to valid data	t_{ELQV}	–	$48t_{CLCL}$	ns
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz



Address: P1.0-P1.7=A0-A7
P2.0-P2.4=A8-A12
Data: P0.0-P0.7=D0-D7

Inputs: P2.5-P2.6, PSEN=V_{SS}
ALE, $\overline{EA}$= V_{IH}
RESET = V_{IH1}

Device Type	ROM Size	Active Address Lines at Port 2	Inactive Address Lines at Port 2
SAB-C511	2.5 KB	P2.0 - P2.3 = A8 - A11	P2.4 - P2.6 = V_{SS}
SAB-C511A	4 KB	P2.0 - P2.3 = A8 - A11	P2.4 - P2.6 = V_{SS}
SAB-C513	8 KB	P2.0 - P2.4 = A8 - A12	P2.5 - P2.6 = V_{SS}
SAB-C513A	12 KB	P2.0 - P2.5 = A8 - A13	P2.6 = V_{SS}

Figure 10-6
ROM Verification Timing

10.4 AC Characteristics of SAB-C513A-H Programming Interface

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V T_A = 0 °C to + 70 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{PLL}	60	–	ns
Address setup to ALE	t_{PAL}	20	–	ns
Address hold after ALE	t_{PLA}	20	–	ns
Address to valid data out	t_{PAD}	–	230	ns
$\overline{PRD}$/$\overline{PWR}$ pulse width	t_{PCC}	250	–	ns
$\overline{PRD}$ to valid data out	t_{PRDV}	–	200	ns
Data hold after $\overline{PWR}$	t_{PWDH}	0	–	ns
Data float after $\overline{PRD}$	t_{PDZ}	–	40	ns
Chip select setup to ALE active	t_{PCS}	0	–	ns
Chip select hold after $\overline{PRD}$/$\overline{PWR}$ inactive	t_{PCH}	0	–	ns
ALE to $\overline{PWR}$ or $\overline{PRD}$	t_{PLC}	90	–	ns
$\overline{PWR}$ or $\overline{PRD}$ high to ALE high	t_{PCL}	20	–	ns
Data setup before $\overline{PWR}$ rising edge	t_{PWDS}	50	–	ns
Data hold after $\overline{PWR}$ rising edge	t_{PWDH}	0	–	ns
Data float after $\overline{PCS}$	t_{PDF}	–	40	ns

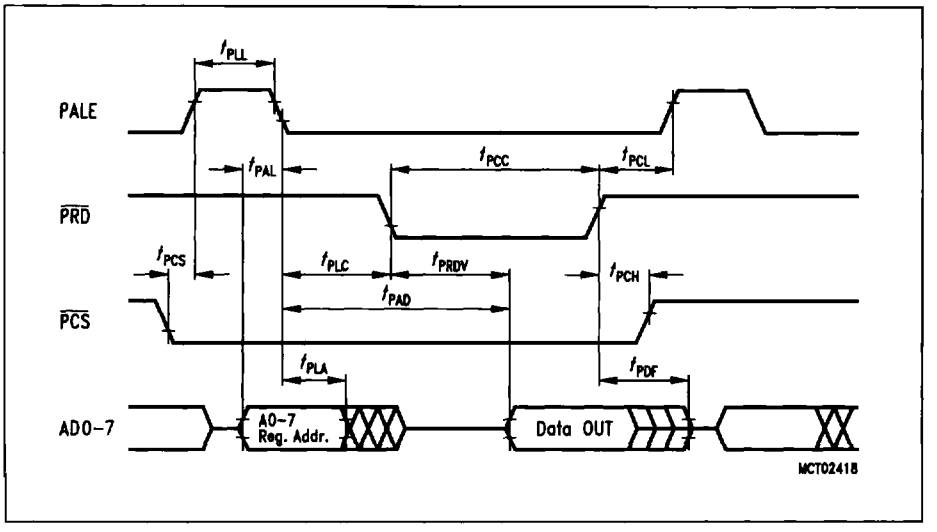


Figure 10-7
SAB-C513A-H Programming Interface Read Cycle

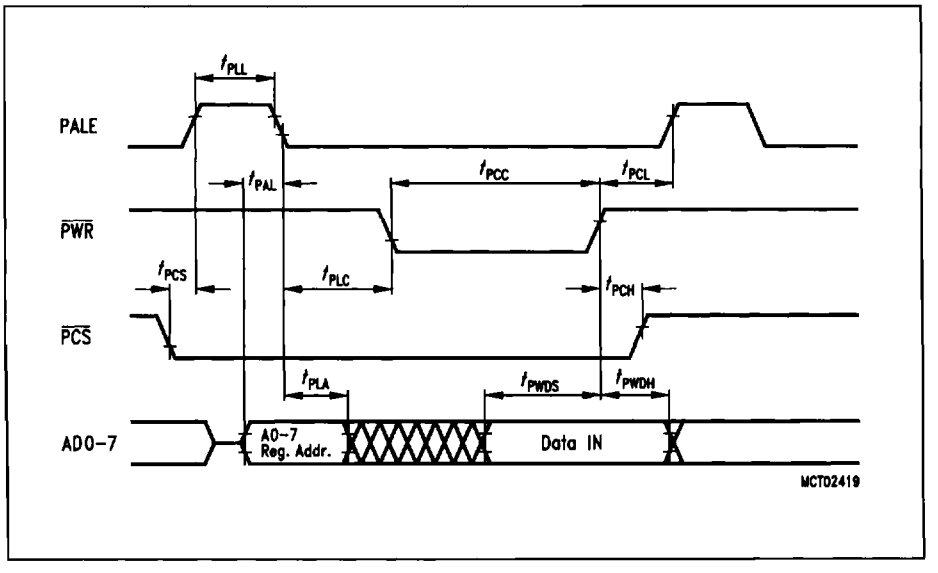


Figure 10-8
SAB-C513A-H Programming Interface Write Cycle

10.4.1 Reset Characteristics (SAB-C513A-H only)

Parameter	Symbol	Limit Values				Unit
		8 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 8 MHz		
		min.	max.	min.	max.	
RESET pulse width	t_{RLRH}	10	–	10	–	ms

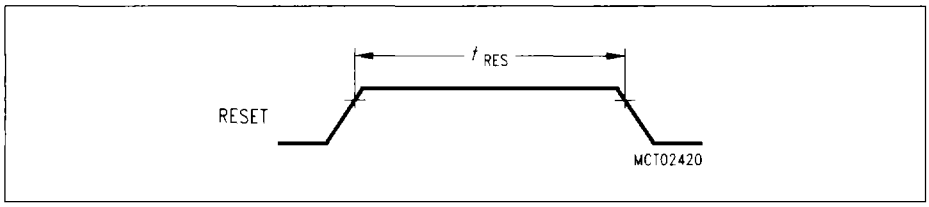
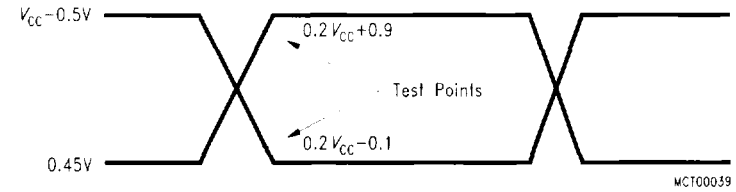
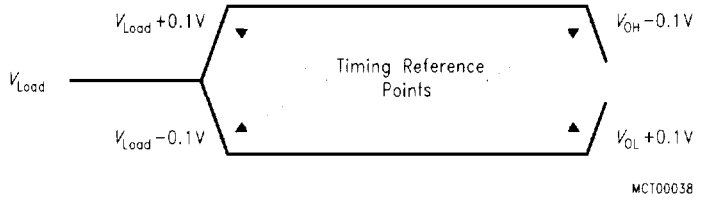


Figure 10-9
Reset Pulse



AC Inputs during testing are driven at V_{CC} - 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure 10-10
AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded I'_{OH}/I'_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm$ 20 mA

Figure 10-11
AC Testing: Float Waveforms

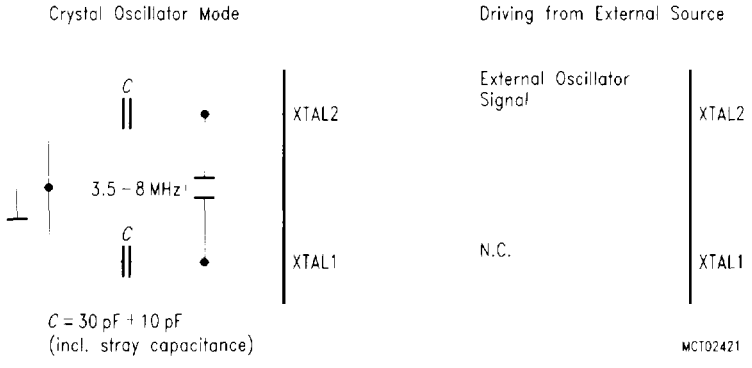
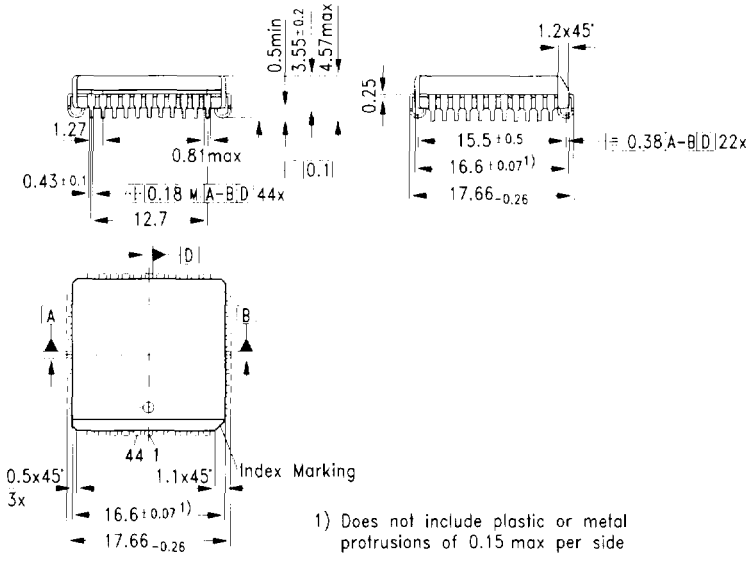


Figure 10-12
Recommended Oscillator Circuits for Crystal Oscillator

10.5 Package Outlines

Plastic Package, P-LCC-44 – SMD
(Plastic Leaded Chip-Carrier)



Dimensions in mm