AK2336A

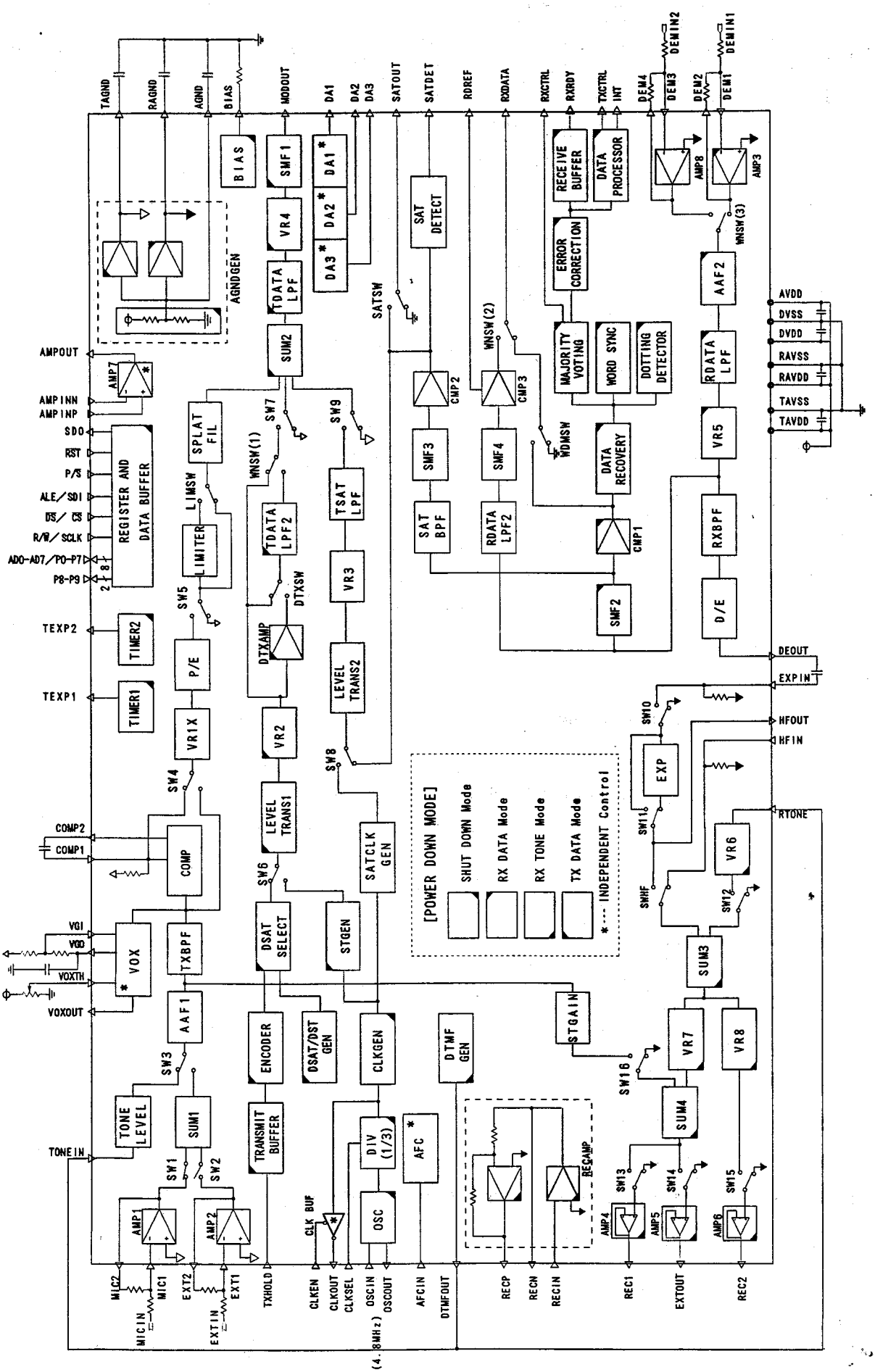
CMOS Base Band Processor for AMPS / TACS / NAMPS / NTACS

The AK2336A is a low power CMOS device incorporating all base band functions for AMPS, TACS, NAMPS and NTACS. All the functions needed for base band signal processing in a cellular telephone, not only audio related functions but also data related functions, are integrated into a single chip. The AK2336A can handle all base band functions only in conjunction with a micro-controller(μC). The AK2336A even handles FOCC data by itself during idle mode. The AK2336A also generates interrupt if first 3 consecutive FOCC data are the same and the RF block may be shutdown duaring the remaining period. Therefore, the AK2336A is suitable for hand-held portable cellular phones, in which power consumption is a key concern.

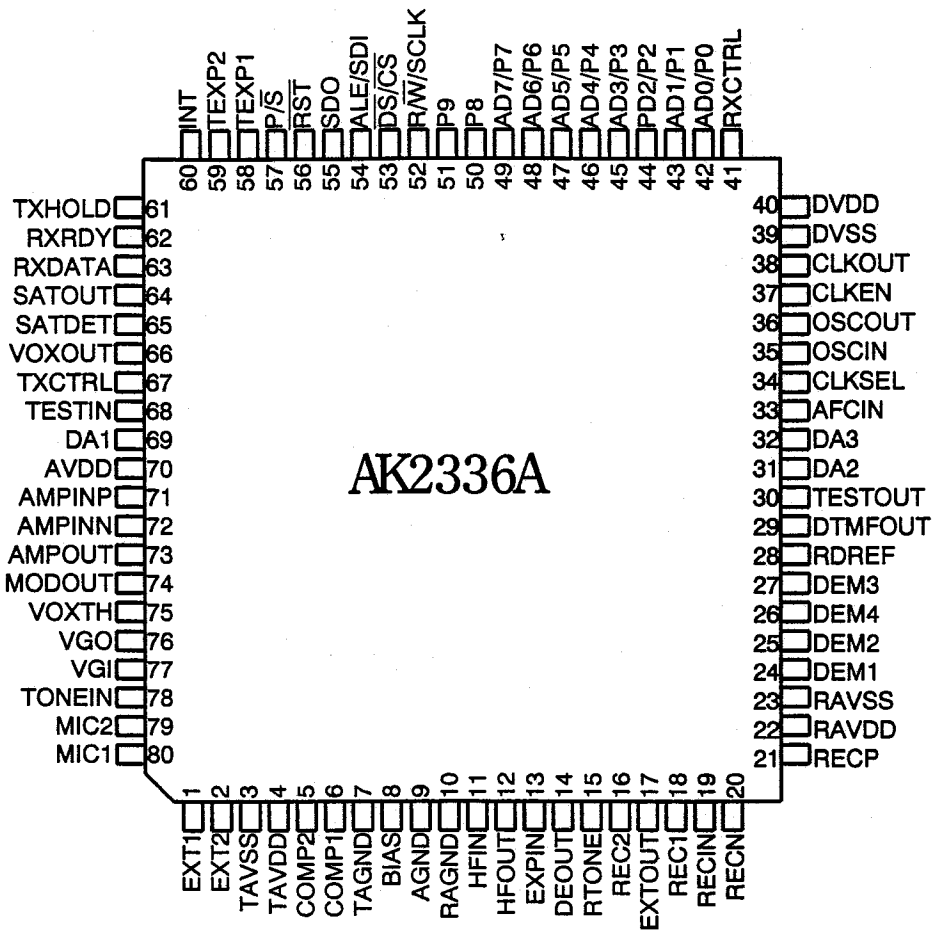
Features

- ☐ Single chip base band LSI for AMPS, NAMPS, TACS and NTACS.
- ☐ Linearity Adjustable CMOS COMPANDOR.
- ☐ Voice signal processing circuits.
- ☐ Error handling, up to 2 bit error correction.
- ☐ Busy/Idle bit extraction.
- ☐ Majority voting.
- ☐ Discontinuous Reception Support.
- ☐ Wide band data processing.
- ☐ SAT decoding and transponding circuits.
- ☐ DSAT/DST generating and transponding circuits.
- ☐ DTMF and ST generator.
- ☐ Digital gain control at various points.
- ☐ Serial/Parallel bus control.
- ☐ 10 bit programmable I/O ports.
- ☐ Ceramic receiver driver.
- ☐ VOX circuit.
- ☐ Uncommitted 8 bit linear DAC × 3.
- ☐ Uncommitted OP-AMP × 1.
- ☐ Uncommitted Timer × 2.
- ☐ Six modes of operation for meticulous power management.
- ☐ 4.8 MHz oscillator circuit / 14.4/4.8 MHz clock input.
- ☐ AFC Counter.
- ☐ Low power CMOS, 1.4mA(TYP;VDD=3V) at Rx Data Mode.
- ☐ Sidetone path circuits.
- ☐ Single 2.7V to 5.5V power supply.
- ☐ 80 pin LQFP package

BLOCK DIAGRAM



■ Pin Configuration



Block Diagram Description

Block	Functions
Transmitter Section	
AMP1	An OP-AMP to adjust the transmit voice(MIC) signal level. Set the proper gain (≦ 30dB) with external resistors.
AMP2	An OP-AMP to adjust the external input signal level. Set the proper gain (≦ 30dB) with external resistors.
SUM1	Summing junction of MIC input signal and EXT input signal.
SW1, 2	SUM1 input signal select switches.
TONE LEVEL	Trnsmit DTMF signal level adjust for TACS/NTACS.
SW3	Transmit voice signal select switch.
AAF1	Anti-aliasing filter.
STGAIN	Gain control(-29dB) circuit to adjust the sidetone level.
SW16	Sidetone signal mute switch.
TXBPF	Band-pass filter (300～3300 Hz) for transmit voice signal.
VOX	Transmit voice signal detection circuit. May be disabled from control register.
COMP	Compressor circuit. Compress the amplitude of transmit voice signal with square root characteristic. Linearity can be adjusted from the control register
SW4	Compressor bypass switch.
VR1x (x = 1, 2)	Digital gain control circuit to set the deviation level. Adjustable from +2.1dB to -2.4dB by 0.3dB step from the control register. VR11 is for MICIN and EXTIN, VR12 is for TONEIN. That selection is linked with SW3.
P／E	Pre-emphasis circuit. Emphasize the higher frequency spectrum of the transmit voice signal in order to improve the signal-to-noise ratio of transmit modulated signal.
SW5	Transmit voice signal mute switch.
LIMITER	Limiting circuit for transmit voice signal amplitude in order to confine the maximum deviation of transmit modulated signal.
LIMSW	Limiter bypass switch.
SPLAT FIL	Low pass filter to reject the higher frequency (> 3kHz) spectrum from the transmit voice signal.
SUM2	Summing junction of transmit voice signal, transmit data and transmit SAT signal.
TDATA LPF	Low pass filter to reject the higher frequency (AMPS: >20kHz, TACS: >16kHz) spectrum from the transmit data signal.
VR4	Digital gain control circuit to set the maximum frequency deviation. Adjustable from 6.2dB to -6.4dB by 0.2dB step from the control register.
SMF1	Smoothing filter for transmit signal.
TRANSMIT BUFFER	38 bits transmit data buffer. Write "[DCC (2 bits)] + [transmit data (36 bit)]"
ENCODER	Add parity to the transmit data, then frame them properly to add Dotting Pattern(Wide), Sync Word(Wide/Narrow) and DCC(Wide), and encode them to Manchester code except Narrow Sync Word.

DSAT/DST GEN	Seven valid transmit DSAT/DST data generator. One DSAT data pattern and DSAT or DST are selected from the conrol register. These generated data are 24-bit NRZ data.
DSAT SELECT	Select either DSAT/DST or data/sync words for the transmit Narrow data. DSAT/DST data is selected while data and sync words are not transmitted at Narrow Analog Mode.
SW6	Select either Transmit data signal or Signaling Tone.
LEVEL TRANS1	Transmit data level translator.
VR2	Digital gain control circuit to set the transmit data signal level. Adjustable from + 3.0dB to -3.2dB by 0.2dB step from the control register.
DTXAMP	Gain Amp(12dB) for DTX low-state.
DTXSW	DTX low-state select switch.
WNSW1	Wide/Narrow mode for transmit data select switch.
TDATA LPF2	Low pass filter(fc=144Hz) to reject the higher frequency spectrum from the transmit data signal.
SW7	Transmit data signal mute switch.
STGEN	Signaling Tone generator.
SATCLKGEN	Transmit SAT signal and SATBPF clock generator.
SW8	Select either receive SAT signal or generated SAT signal(for test) for transmit SAT signal.
LEVEL TRANS2	Transmit SAT signal level translator.
VR3	Digital gain control circuit to set the transmit SAT signal level. Adjustable from + 1.4dB to -1.6dB by 0.2dB step from the control register.
TSATLPF	Low pass filter to reject the higher frequency spectrum of transmit SAT signal.
SW9	Transmit SAT signal mute switch.
Receiver Section	
AMP3	An OP-AMP to adjust the receive signal level. Set the proper gain (≦ 30dB) with external resistors.
AMP8	An OP-AMP to adjust the receive narrow data signal. Set the proper gain (≦ 30dB) with external resistors.
WNSW3	Wide(AMP3)/Narrow(AMP8) mode for receiver input AMP select switch. It is controlled from the control register add. 01 and 28.
AAF2	Anti-aliasing filter for receive signal.
RDATA LPF	Low pass filter to reject the higher frequency spectrum of receive signal.
VR5	Digital gain control circuit to set the receive signal level. Adjustable from + 3.0dB to -3.2dB by 0.2dB step from the control register.
RXBPF	Band-pass filter (300Hz～3300Hz) for receive voice signal.
D/E	De-emphasis circuit. Equalize the pre-emphasized voice signal to the original.
SW10	Receive voice signal mute switch.
EXP	Expander circuit. Expand the compressed voice signal to the original. Linearity can be adjusted from the control register.

SW11	Expander bypass switch.
SWHF	Hands-free system select switch.
VR6	Digital gain control circuit to set the RTONE signal level. Adjustable from + 0dB to -18dB by 6dB step from the control register.
SW12	RTONE signal mute switch.
SUM3	Summing junction of receive voice signal and RTONE signal.
VR7	Digital gain control circuit to set the level of REC1 output and EXTOUT output Adjustable from + 0dB to -21dB by 3dB step from the control register.
SUM4	Summing junction of receive voice signal and sidetone signal.
SW13	REC1 output mute switch.
AMP4	REC1 output buffer. Can drive 10kΩ or larger load.
SW14	EXTOUT output mute switch.
AMP5	EXTOUT output buffer. Can drive 10kΩ or larger load.
VR8	Digital gain control circuit to set the level of REC2 output Adjustable from + 0dB to -21dB by 3dB step from the control register.
SW15	REC2 output mute switch.
AMP6	REC2 output buffer. Can drive 10kΩ or larger load.
RECAMP	Ceramic receiver driver.
SMF2	Smoothing filter for receive data signal.
CMP1	Quantize the receive wide band data signal.
WDMSW	Quantized the receive wide band data output mute switch.
DATA RECOVERY	Receive wide band data recovery circuit. Recover clock from the received data and decode Manchester code to NRZ data.
WORD SYNC	Frame synchronization circuit.
DOTTING DETECTOR	Detect the Dotting Pattern of FVC and mute receive section during data burst after frame synchronization.
WNSW2	Wide/Narrow mode for receive data output select switch.
MAJORITY VOTING	3/5 majority voting circuit. Also, support Discontinuous Reception.
ERROR CORRECTION	Error correction circuit. Correct up to 2 bits error.
DATA PROCESSOR	Data Processor. Monitor the FOCC messages and generate interrupt at proper condition. Also, monitor the RECC status (BUSY/IDLE) .
RECEIVE BUFFER	30 bits receive data buffer. Buffer Error Status (2 bits) and 1 word (28 bits) .
RDATA LPF2	Low pass filter(fc=150Hz) to reject the higher frequency spectrum of receive signal.
SMF4	Smoothing filter for Narrow band receive data signal.
CMP3	Quantize the receive narrow band receive data signal.
SATBPF	High-Q band-pass filter to select receive SAT signal.

SMF3	Smoothing filter for receive SAT signal.
CMP2	Quantize the received SAT signal.
SATSW	Quantized the receive SAT signal output mute switch.
SAT DETECT	SAT signal detector. Detect the selected SAT signal.
The others	
OSC	Oscillator circuit. Generate 4.8 MHz main clock with quartz crystal, external resistor and cap. Or input 14.4/4.8 MHz clock to OSCIN pin.
DIV (1/3)	Clock divider. (1/3) Generate 4.8 MHz main clock from external 14.4MHz clock.
CLK BUF	4.8MHz clock output buffer.
CLKGEN	Internal clock generator.
DTMFGEN	Tone (include DTMF) signal generator.
TIMER1	Uncommitted 8 bits Timer 1.
TIMER2	Uncommitted 8 bits Timer 2.
DA1	Uncommitted 8 bits linear DAC 1.
DA2	Uncommitted 8 bits linear DAC 2.
DA3	Uncommitted 8 bits linear DAC 3.
AMP7	Uncommitted OP-AMP.
AFC	Auto Frequency Control Circuit.
REGISTER & DATA BUFFER	8 bit data bus interface circuit and 2 bit programmable I/O ports at parallel mode. At serial interface mode, AD0/P0～AD7/P7 pins are available for 8 bit programmabl I/O ports. P8 and P9 pins are available for 2 bit programmable I/O ports at any time.
BIAS	OP-AMP bias current generator.
AGNDGEN	Analog ground (1/2 VDD) generator.

Pin / Functions

NOTE: The value inside ( ) at the column I/O indicates the the value after RESET.

Pin No.	Pin Name	I/O	Function
Power			
40	DVDD	-	Power supply for digital section.
39	DVSS	-	GND for digital section.
22	RAVDD	-	Power supply for receiver analog section.
23	RAVSS	-	GND for receiver analog section.
4	TAVDD	-	Power supply for transmitter analog section.
3	TAVSS	-	GND for transmitter analog section.
70	AVDD	-	Power supply for substrate.
9	AGND	-	Analog ground (1/2 AVDD), connect capacitor.
10	RAGND	O	Analog ground (1/2 AVDD) for receiver section.
7	TAGND	O	Analog ground (1/2 AVDD) for transmitter section.
8	BIAS	I	Bias current setting pin. Connect to VSS through a specified resistor below; R_{BIAS} = 20×VDD [kΩ]
Transmit			
80	MIC1	I	MIC input (Inverting input of AMP1). Input impedance > 1MΩ. Set the MIC AMP (AMP1) gain with external resistors.
79	MIC2	O	MIC AMP output (output of AMP1). This output can drive50kΩ or larger, and 15pF or smaller.
78	TONEIN	I	Transmit DTMF Tone input. Input impedance > 1MΩ.
1	EXT1	I	EXT input (Inverting input of AMP2). Input impedance > 1MΩ. Set the EXT AMP (AMP2) gain with external resistors.
2	EXT2	O	EXT AMP output (output of AMP2). This output can drive50kΩ or larger, and 15pF or smaller.
61	TXHOLD	I	Transmit data hold input.
75	VOXTH	I	VOX threshold input.
66	VOXOUT	O(L)	VOX output. ("H":detect)
77	VGI	I	VOX gain stage input. Connect external resisters and a capacitor to set the sensitivity and the recovery time.
76	VGO	O	VOX gain stage output. Connect external resisters and a capacitor to set the sensitivity and the recovery time.
6	COMP1	I	Compressor capacitor connect pin. Connect a 0.047μF capacitor between COMP1 and COMP2.
5	COMP2	O	Compressor output.
74	MODOUT	O	Transmit output. This output can drive 10kΩ or larger, and 50pF or smaller.

Receive			
24	DEM1	I	Receive signal input (inverting input of AMP3). Input impedance > 1MΩ. Set the receive input gain with external resistors.
25	DEM2	O	Output of AMP3. This output can drive 50kΩ or larger, and 15pF or smaller.
27	DEM3	I	Receive signal input (inverting input of AMP8). Input impedance > 1MΩ. Set the receive input gain with external resistors.
26	DEM4	O	Output of AMP8. This output can drive 50kΩ or larger, and 15pF or smaller.
65	SATDET	O (L)	Receive SAT detect output. ("H":detect)
64	SATOUT	O (L)	Receive SAT signal output.
28	RDREF	O	CMP3 off-set cancelation reference. Connect capacitor for off-set cancellation.
63	RXDATA	O (L)	Receive Wide/Narrow data output.
41	RXCTRL	O (H)	RF Receiver control. (refer to p71)
67	TXCTRL	O (H)	RF Transmitter control.
60	INT	O (L)	Interrupt output.
62	RXRDY	O (L)	Receive data ready.
14	DEOUT	O	De-emphasis output. Connect a 0.047μF capacitor between DEOUT and EXPIN.
13	EXPIN	I	Expander input. Connect a 0.047μF capacitor between DEOUT and EXPIN.
12	HFOUT	O	Receive voice signal output for Hands-free system. This output can drive 50kΩ or larger and 150pF or smaller
11	HFIN	I	Receive voice signal input for Hands-free system. This pin is connected RAGND with internal resister. Input impedance > 100kΩ
29	DTMFOUT	O	DTMF tone output. This output can drive 10kΩ or larger and 50pF or smaller.
15	RTONE	I	DTMF Tone input for the receiver. Input impedance > 1MΩ
17	EXTOUT	O	External receive signal output. This output can drive 10kΩ or larger and 50pF or smaller.
18	REC1	O	Receive signal output 1. This output can drive 10kΩ or larger and 50pF or smaller.
16	REC2	O	Receive signal output 2. This output can drive 10kΩ or larger and 50pF or smaller.
19	RECIN	I	Ceramic receiver driver input.
21	RECP	O	Ceramic receiver driver positive output.
20	RECN	O	Ceramic receiver driver negative output.
DAC/AMP			
69	DA1	O	DAC 1 output. This output can drive 50kΩ or larger, and 50pF or smaller.
31	DA2	O	DAC 2 output. This output can drive 50kΩ or larger, and 50pF or smaller.
32	DA3	O	DAC 3 output. This output can drive 50kΩ or larger, and 50pF or smaller.

73	AMPOUT	O	AMP7 output. This output can drive 10kΩ or larger, and 50pF or smaller.
71	AMPINP	I	AMP7 non-inverting input.
72	AMPINN	I	AMP7 inverting input.
Control			
57	P/S	I	Parallel/Serial interface select.
53	DS／CS	I	Data strobe input ／ Chip select input.
54	ALE／SDI	I	Address latch enable input ／ Serial data input.
52	R/W／SCLK	I	Read/Write Select input ／ Serial clock input.
55	SDO	O(Z)	Serial data output.
42-49	AD0～AD7／ P0～P7	I/O	Parallel interface mode: 8 bit Adress/Date bus. Serial interface mode : 8 programmable I/O ports.
50-51	P8～P9	I/O	2 programmable I/O ports.
56	RST	I	Reset input. "L" active. Minimum pulse width is 100ns.
58	TEXP1	O(L)	Timer 1 expire output.
59	TEXP2	O(L)	Timer 2 expire output.
Clock			
35	OSCIN	I	4.8 MHz Oscillator input／14.4/4.8MHz clock input.
36	OSCOUT	O	4.8 MHz Oscillator output.
34	CLKSEL	I	Clock selection pin. (14.4 MHz("L") / 4.8 MHz("H"))
38	CLKOUT	O	4.8 MHz clock output. ("L": disable)
37	CLKEN	I	Clock output enable ("L": enable, "H": disable)
33	AFCIN	I	IF signal input pin for AFC.
Test			
68	TESTIN	I	Test input pin. (Connect to AVSS at normal operation)
30	TESTOUT	O	Test output pin. (Connect nothing at normal operation)

Z: High-Z

Absolute Maximum Ratings

TAVSS, RAVSS, DVSS=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supply	VA+	-0.3	6.5	V
Input Current (except power supply pin)	I_{IN}	-	±10	mA
Analog Input Voltage	V_{INA}	-0.3	(VA+)+0.3	V
Digital Input Voltage	V_{IND}	-0.3	(VA+)+0.3	V
Storage Temperature	Tstg	-55	130	℃

Note 1: All voltage values are with respect to VSS pin.
WARNING: Operations at or beyond these limits may results in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

TAVSS, RAVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Ambient Operating Temperature		Ta	-30		85	℃
Power Supply		VDD	2.7		5.5	V
Analog Ground		AGND		1/2VDD		V
[VDD=3V]						
Power Consumption	mode 0	Idd0		0.7		mA
(Note 2)	mode 1	Idd1		1.4		
	mode 2	Idd2		2.9		
	mode 3	Idd3		2.3		
	mode 4	Idd4		3.8		
	mode 5	Idd5		7.0		
[VDD=5V]						
Power Consumption	mode 0	Idd0		1.0	1.3	mA
(Note 2)	mode 1	Idd1		2.0	2.8	
	mode 2	Idd2		3.5	5.0	
	mode 3	Idd3		2.9	4.0	
	mode 4	Idd4		4.4	6.1	
	mode 5	Idd5		7.9	11.2	

Note 1: All voltage values are with respect to VSS pin.
Note 2: Oscillator: 14.4MHz input, DACs, AMP7, VOX, AFC: OFF

Digital Characteristics

■ DC Specifications

Parameter	Pin	Symbol	min	typ	max	Units
High Level Input Voltage	(1)	V_{IH}	70%VDD			V
Low Level Input Voltage	(1)	V_{IL}			30%VDD	V
High Level Input Current V_{IH}=VDD	(1)	I_{IH}			10	μA
Low Level Input Current V_{IL}=0V	(1)	I_{IL}	-10			μA
High Level Output Voltage I_{OH}=-400μA	(2)	V_{OH}	90%VDD			V
Low Level Output Voltage I_{OL}=400μA	(2)	V_{OL}			0.4	V

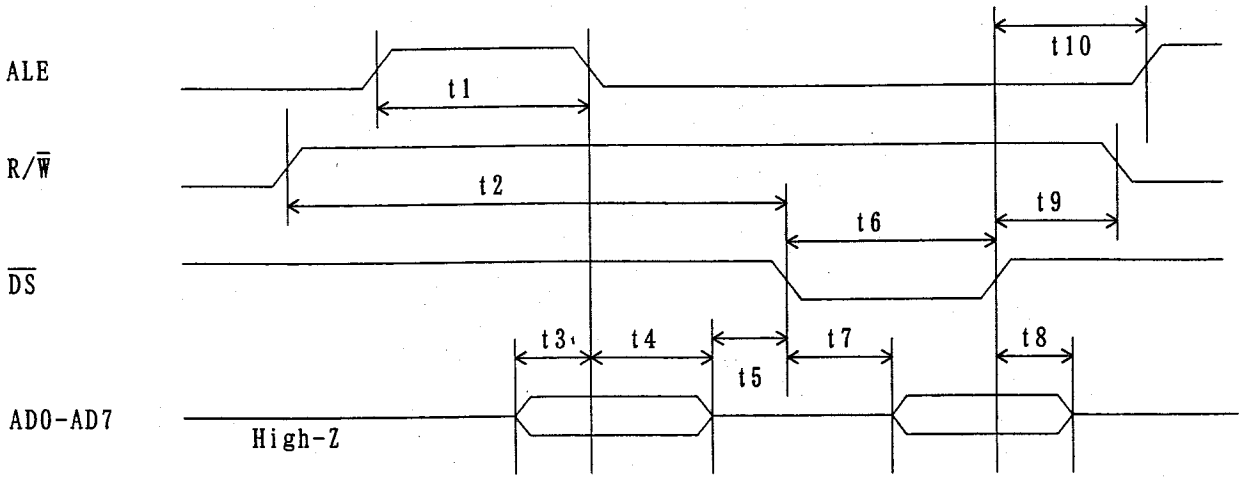
(1) All digital inputs ($\overline{RST}$, P/$\overline{S}$, SDI/ALE, $\overline{CS}$/$\overline{DS}$, SCLK/R/$\overline{W}$, CLKEN, CLKSEL, TXHOLD, P0~P7/AD0~AD7, P8, P9)

(2) All digital outputs (SDO, TEXP1, TEXP2, VOXOUT, CLKOUT, RXRDY, INT, TXCTRL, SATDET, P0~P7/AD0~AD7, P8, P9, RXDATA, RXCTRL, SATOUT)

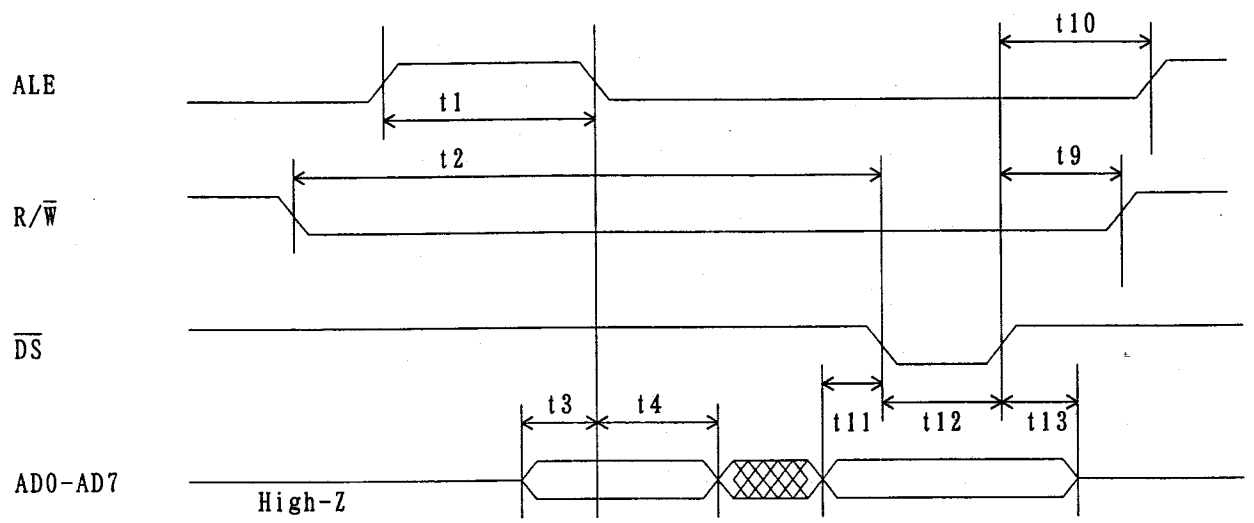
■ AC Specifications

Parameter	Pin	Symbol	min	typ	max	Units
Master Clock Frequency	OSCIN					
(CLKSEL=1)		F_{CK1}		4.8		MHz
(CLKSEL=0)		F_{CK2}		14.4		
4.8MHz Clock Duty Cycle	OSCIN	F_{CKDTY}	40		60	%
Input Level (H)		F_{CKVH}	20			V
Input Level (L)		F_{CKVL}			0.3	V
14.4MHz Clock Input Level	OSCIN	F_{OSCIN}	0.3		1.5	V_{P-P}
AFCIN Input Frequency	AFCIN	F_{AFCIN}		450		kHz
AFCIN Input Level	AFCIN	V_{AFCIN}	0.3		1.5	V_{P-P}
Parallel Interface Timing						
ALE Pulse Width "H"	ALE	t1	1000			ns
R/$\overline{W}$ Setup Time		t2	100			ns
Address Setup Time		t3	100			ns
Address Hold Time		t4	100			ns
$\overline{DS}$ Setup Time		t5	0			ns
$\overline{DS}$ Pulse Width "L"		t6				
Status and Event Register			1000			ns
Data Register			2000			ns
DS "↓" to Data Valid (Note 1)		t7			100	ns
Data Hold Time		t8	0			ns
R/$\overline{W}$ Hold Time		t9	100			ns
DS "↑" to ALE "↑"		t10	1000			ns
Data Setup Time		t11	100			ns
$\overline{DS}$ Pulse Width "L"		t12	1000			ns
Data Hold Time		t13	100			ns
$\overline{DS}$ CYCLE Time <WRITE>			2000			ns
(Status & Event) <READ>			2000			ns
(Data) <READ>			3000			ns
Serial Interface Timing						
$\overline{CS}$ "↓" to SCLK "↓"	$\overline{CS}$, SCLK	t1	100			ns
SCLK Pulse width "L"	SCLK	t2	350			ns
SCLK Pulse width "H"	SCLK	t3	350			ns
SDI data set-up time	SDI	t4	100			ns
SDI Data hold time	SDI	t5	100			ns
SCLK "↑" to $\overline{CS}$ hold time	$\overline{CS}$, SCLK	t6	600			ns
$\overline{CS}$ Pulse width "H"	$\overline{CS}$	t7	400			ns
SCLK Pulse width of R/$\overline{W}$ bit "H"	SCLK	t8				
(Status & Event)			400			ns
(Data)			2000			ns
SCLK "↓" to SDO Data Valid (Note)	SDO	t9			100	ns
$\overline{CS}$ "↑" to SDO Hi-Z		t10			100	ns

Note: Load Cap < 20pF



Parallel Interface Timing - Read



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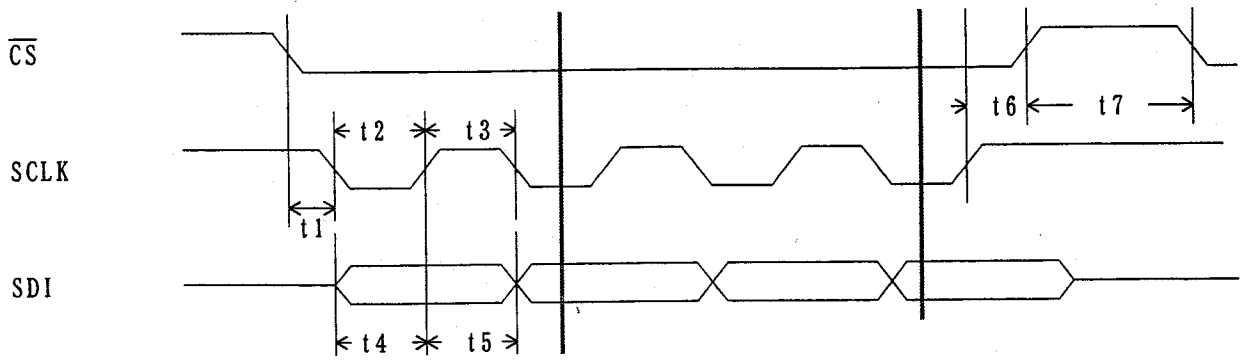

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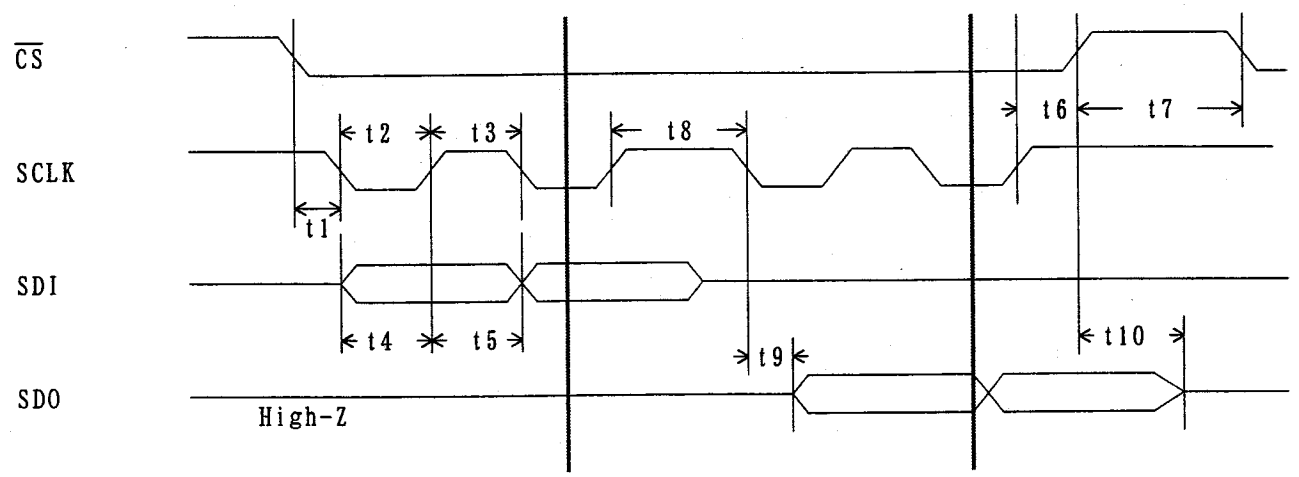


Serial Interface Timing - READ

Analog Characteristics

AVDD=3.0V
AVSS=0V
Ta=-30～+85℃

■ Transmitter

Item	Pin	Conditions	MIN	TYP	MAX	Units	Remarks
Gain	MIC2 ↓ MODOUT	MIC2=-22.0dBV @ 1kHz VR11=0dB, VR4=-5dB COMPRESSOR ON	-2.0	0.0	+2.0	dB	AMPS/ TACS
			-7.7	-5.7	-3.7	dB	NAMPS
			-5.7	-3.7	-1.7	dB	NTACS
	EXT2 ↓ MODOUT	EXT2=-22.0dBV @ 1kHz VR11=0dB, VR4=-5dB COMPRESSOR ON	-2.0	0.0	+2.0	dB	AMPS/ TACS
			-7.7	-5.7	-3.7	dB	NAMPS
			-5.7	-3.7	-1.7	dB	NTACS
	TONEIN ↓ MODOUT	TONEIN=-13.2dBV @ 1kHz VR12=0dB, VR4=-5dB COMPRESSOR OFF	-7.0	-5.0	-3.0	dB	AMPS
			-11.3	-9.3	-7.3	dB	TACS
			-14.5	-12.5	-10.5	dB	NAMPS
			-11.7	-9.7	-7.7	dB	NTACS
SINAD (S/N+D)	MIC2 ↓ MODOUT	MIC2=-8.0dBV @ 1kHz VR1=0dB VR4=-5dB COMPRESSOR ON C-message weighted	35			dB	
Noise Level	MODOUT	VR1=0dB, VR4=-5dB COMPRESSOR ON C-message weighted			-42	dBV	Note 1)
Volume Step Deviation		VR1	-0.3		+0.3	dB	
		VR2, VR3, VR4	-0.2		+0.2		
Limitter Level	MODOUT		0.584	0.619	0.656	Vp-p	
SAT Output Level	MODOUT	VR3=-12dB VR4=-5dB	-26.7	-25.2	-23.7	dBV	
Data Output Level	MODOUT	VR2=0dB VR4=-5dB	-14.7	-13.2	-11.7	dBV	AMPS/ TACS
			-35.8	-34.3	-32.8	dBV	NAMPS
			-33.8	-32.3	-30.8	dBV	NTACS
DTMF Output Level	DTMFOUT	Single Tone	-14.2	-13.2	-12.2	dBV	
DTMF Twist DTH - DTL	DTMFOUT	AMPS		0		dB	
		TACS		2			
DTMF Frequency Deviation	DTMFOUT		-1.5		+1.5	%	
DTMF Tone SINAD	MODOUT	Single tone output	20			dB	
VOX Sensitivity VOX Attack Time VOX Recovery Time		(refer to P69)					
SW1 OFF Attenuation Level	MIC2 ↓ MODOUT	MIC2=3.0Vpp @1kHz EXTIN=TAGND SW1, SW2, SW7, SW9=OFF VR1=0dB, VR4=-5dB COMPRESSOR ON C-message weighted			-49	dBV	AMPS/ TACS

Item	Pin	Conditions	MIN	TYP	MAX	Units	Remarks
SW2 OFF Attenuation Level	EXT2 ↓ MODOUT	EXT2=3.0Vpp @1kHz MICIN=TAGND SW1, SW2, SW7, SW9=OFF VR1=0dB, VR4=-5dB COMPRESSOR ON C-message weighted			-49	dBV	AMPS/ TACS

Note 1) Connect voice band input (TONEIN, MICIN, EXTIN) to TAGND through external resistor.

■ Receiver

Item	Pin	Conditions	MIN	TYP	MAX	Units	Remarks
Gain	DEM2 ↓ EXTOUT	DEM2=-20dBV @ 1kHz VR5=0dB, VR7=0dB EXPANDOR ON	-10.0	-8.0	-6.0	dB	AMPS/ TACS
			+1.4	+3.4	+5.4	dB	NAMPS
			-2.6	-0.6	+1.4	dB	NTACS
	DEM4 ↓ EXTOUT	DEM2=-20dBV @ 1kHz VR5=0dB, VR7=0dB EXPANDOR ON	+1.4	+3.4	+5.4	dB	NAMPS
			-2.6	-0.6	+1.4	dB	NTACS
	DEM2 ↓ REC2	DEM2=-20dBV @ 1kHz VR5=0dB, VR8=0dB EXPANDOR ON	-10.0	-8.0	-6.0	dB	AMPS/ TACS
			+1.4	+3.4	+5.4	dB	NAMPS
			-2.6	-0.6	+1.4	dB	NTACS
	RTONE ↓ REC1	RTONE=-20dBV @ 1kHz VR6=0dB VR7=0dB	-1.0	0	+1.0	dB	
SINAD (S/N+D)	DEM2 ↓ REC1	DEM2=-11.2dBV @ 1kHz VR5=0dB VR7=0dB EXPANDOR ON C-message weighted	35			dB	
Noise Level	REC1	VR5=0dB VR7=0dB EXPANDOR ON C-message weighted		-80	-70	dBV	Note 1)
Volume Step Deviation		VR5	-0.2		-0.2	dB	
		VR6, VR7, VR8	-0.5		+0.5		
SAT Detect Level	DEM2	f=6kHz VR5=0dB	-35.2			dBV	Note 2)

Note 1) Connect DEM1 to RAGND through external resistor.

Note 2) measured with SAT frequency of 6kHz

■ Cross Talk

Item	Pin	Conditions	MIN	TYP	MAX	Units	Remarks
Crosstalk	DEM2 ↓ MODOUT	DEM2 = -11.2dBV COMPRESSOR ON EXPANDOR ON VR1, VR5, VR7 = 0dB VR4 = -5dB			-60	dB	NOTE 1)
	MIC2 ↓ REC1	MIC2 = -8.0dBV COMPRESSOR ON EXPANDOR ON VR1, VR5, VR7 = 0dB VR4 = -5dB			-60	dB	NOTE 1)

Note 1) Connect the other analog input to RAGND/TAGND with an external resister respectively.

■ Filter Specification

Filter Name	Pin	Frequency Response	Condition		
			Input level	Reference Frequency	
RX OVERALL	DEM2 ↓ REC1	Fig-1	-20dBV	1 kHz	VR5: 0dB VR7: 0dB EXPANDOR: OFF
TX OVERALL	MIC2 ↓ MODOUT	Fig-2	-22dBV	1 kHz	VR1: 0dB VR4:-5dB COMPRESSOR:OFF
Splatter Filter		Fig-3			
TDATA LPF		Fig-4			
RDATA LPF2		Fig-5			
TDATA LPF2		Fig-6			

■ Compandor Specification(Not adjusted linearity from control register)

AVDD=3.0V f=1kHz

Item	Pin	Conditions	MIN	TYP	MAX	Units	Remarks
Compressor							
Unity Gain Level	COMP2	MIC2 = -12.0dBV	-13.0	-12.0	-11.0	dBV	
Output Level	COMP2	MIC2 = -2.0dBV	4.0	5.0	6.0	dB	Note 1)
		MIC2 = -52.0dBV	-22.0	-20.0	-18.0	dB	Note 1)
Attack Time	COMP2	MIC2 = -24.0dBV → -12.0dBV 1.5 times of final value	2	3	5	ms	
Recovery Time	COMP2	MIC2 = -12.0dBV → -24.0dBV 0.75 times of final value	7	13.5	20	ms	
Expander							
Unity Gain Level	HFOUT	EXPIN = -12.0dBV	-13.0	-12.0	-11.0	dBV	
Output Level	HFOUT	EXPIN = -7.0dBV	9.0	10.0	11.0	dB	Note 2)
		EXPIN = -32.0dBV	-43.0	-40.0	-37.0	dB	Note 2)
Attack Time	HFOUT	EXPIN = -18.0dBV → -12.0dBV 0.75 times of final value	7	13.5	20	ms	
Recovery Time	HFOUT	EXPIN = -12.0dBV → -18.0dBV 1.5 times of final value	7	13.5	20	ms	

Note 1) Relative value to unity gain level, without register adjustment (Fig-7)
Note 2) Relative value to unity gain level, without register adjustment (Fig-8)

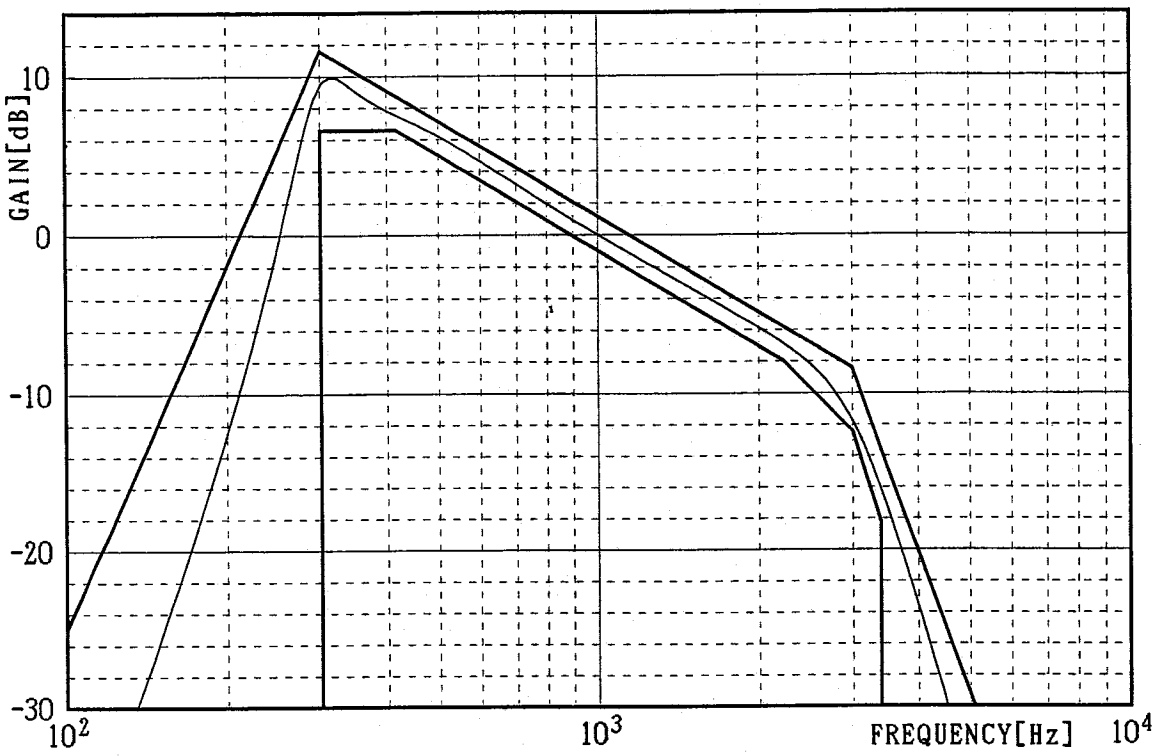


Fig - 1 Total Frequency Response of Receiver Section

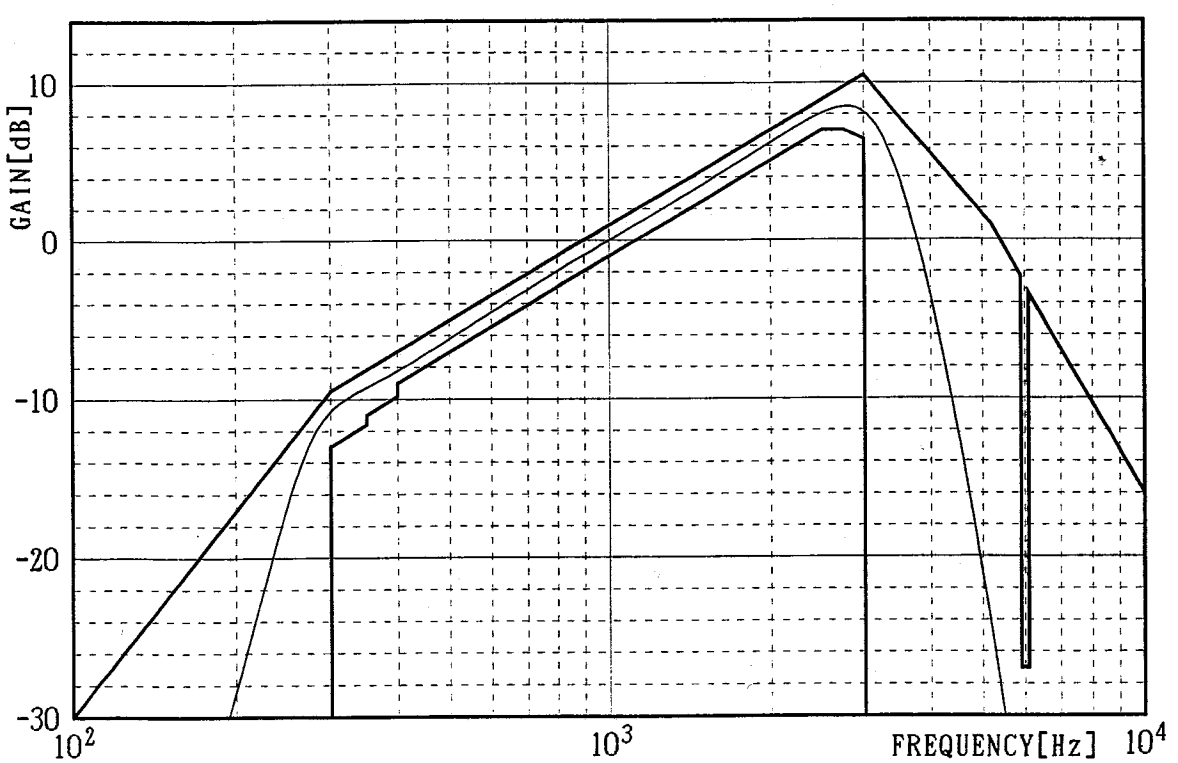


Fig - 2 Total Frequency Response of Transmitter Section

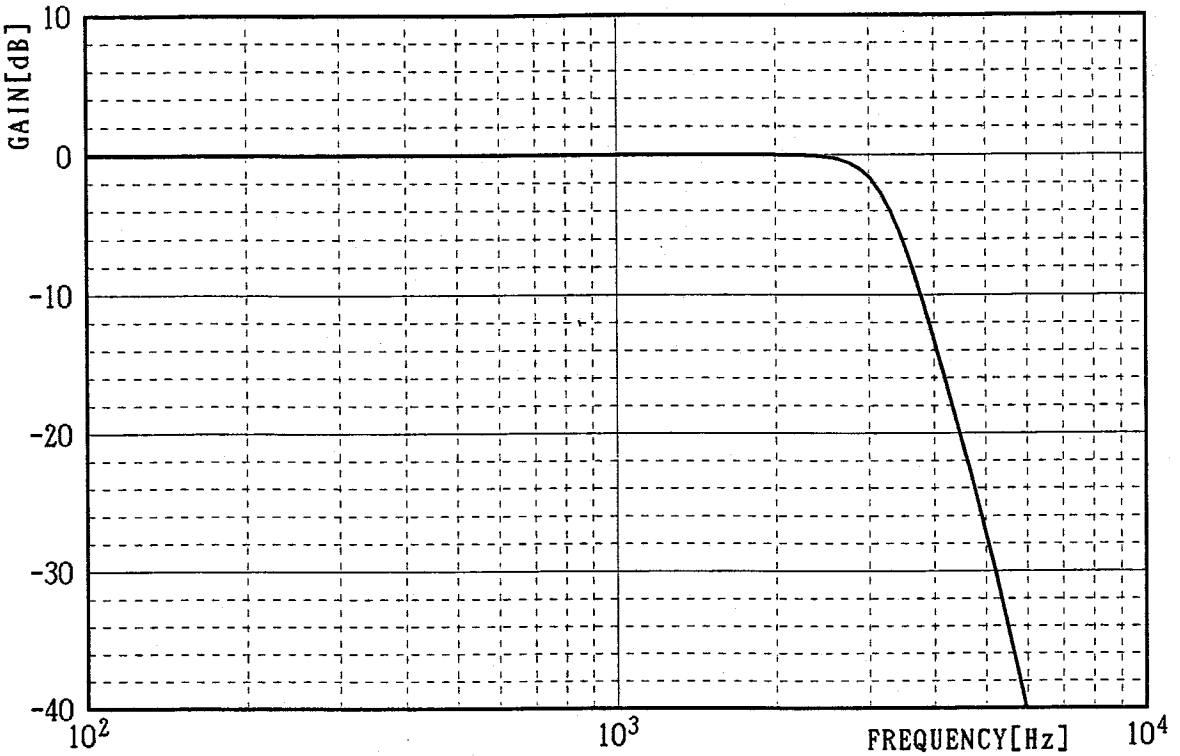


Fig - 3 Frequency Response of Splatter Filter

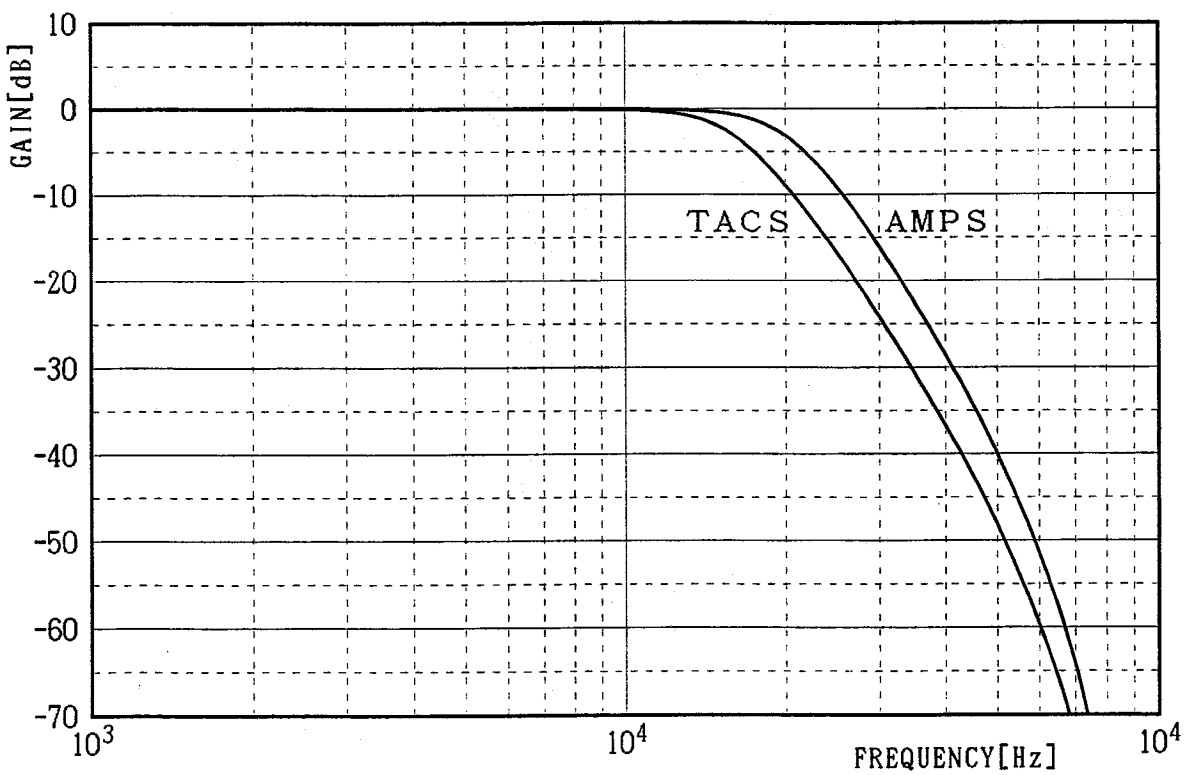


Fig - 4 Frequency Response of Transmitter Data Filter

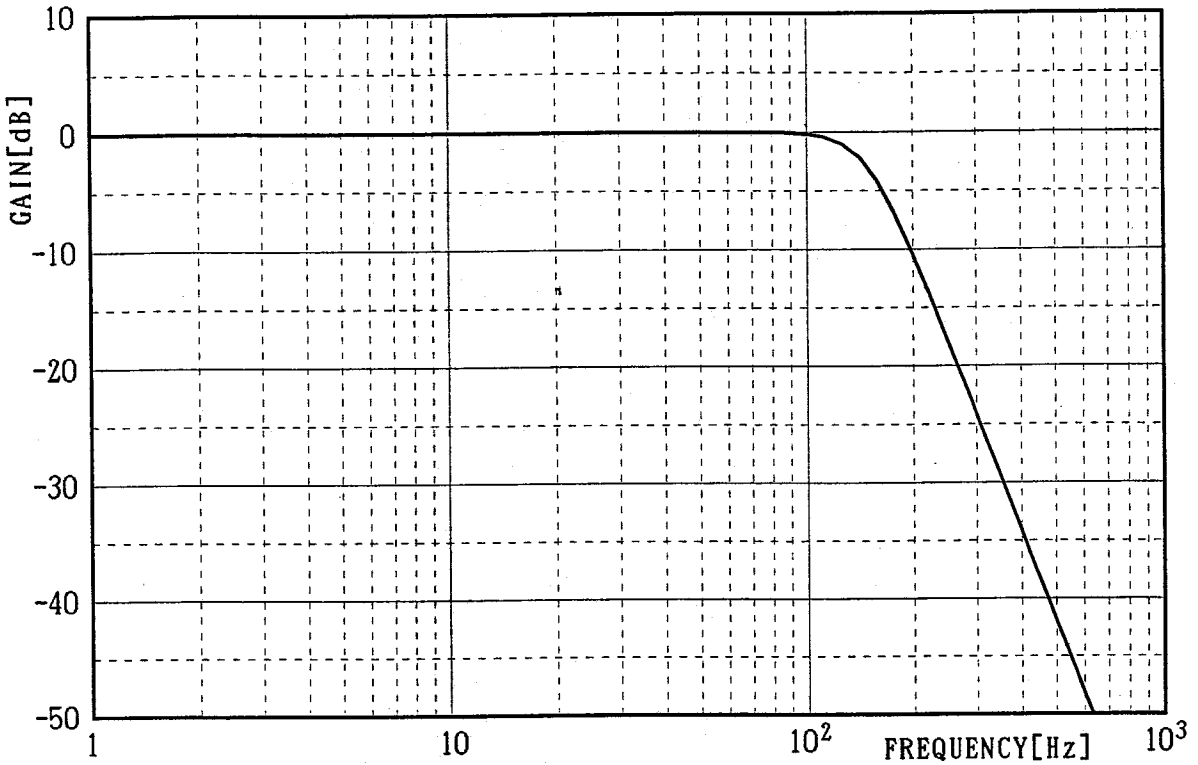


Fig - 5 Frequency Response of Receiver Data Filter2

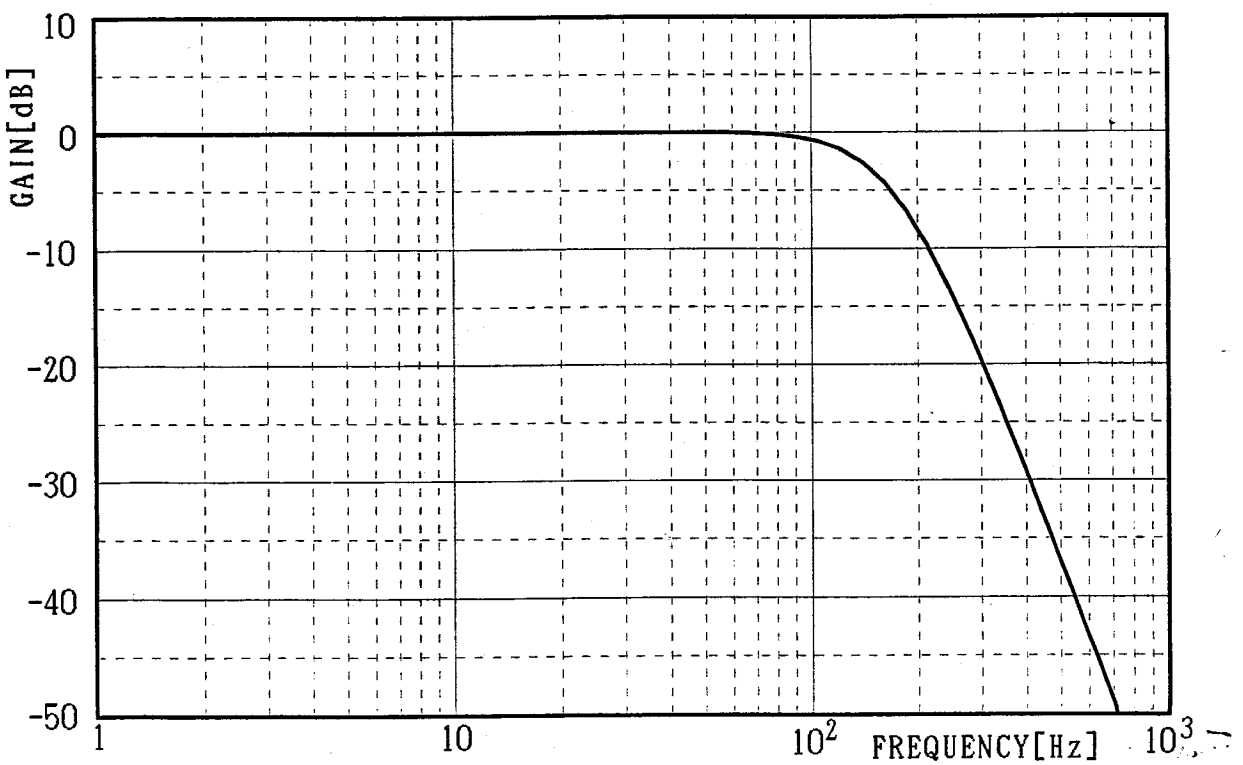


Fig - 6 Frequency Response of Transmitter Data Filter2

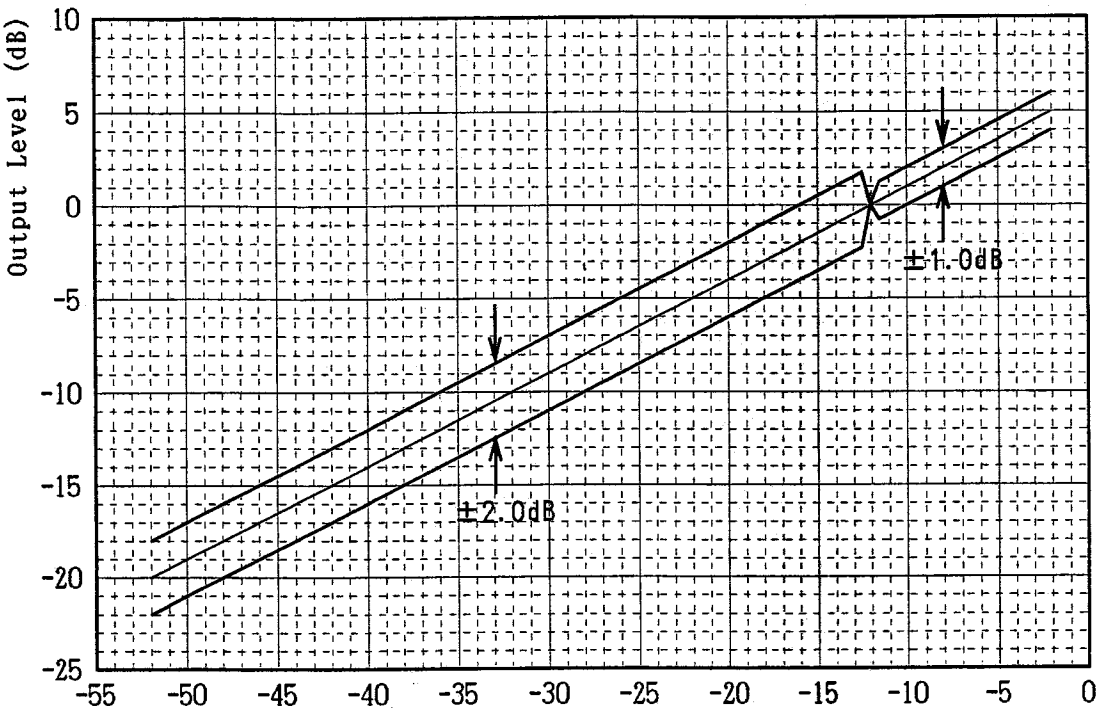


Fig-7 COMPRESSOR LINEARITY

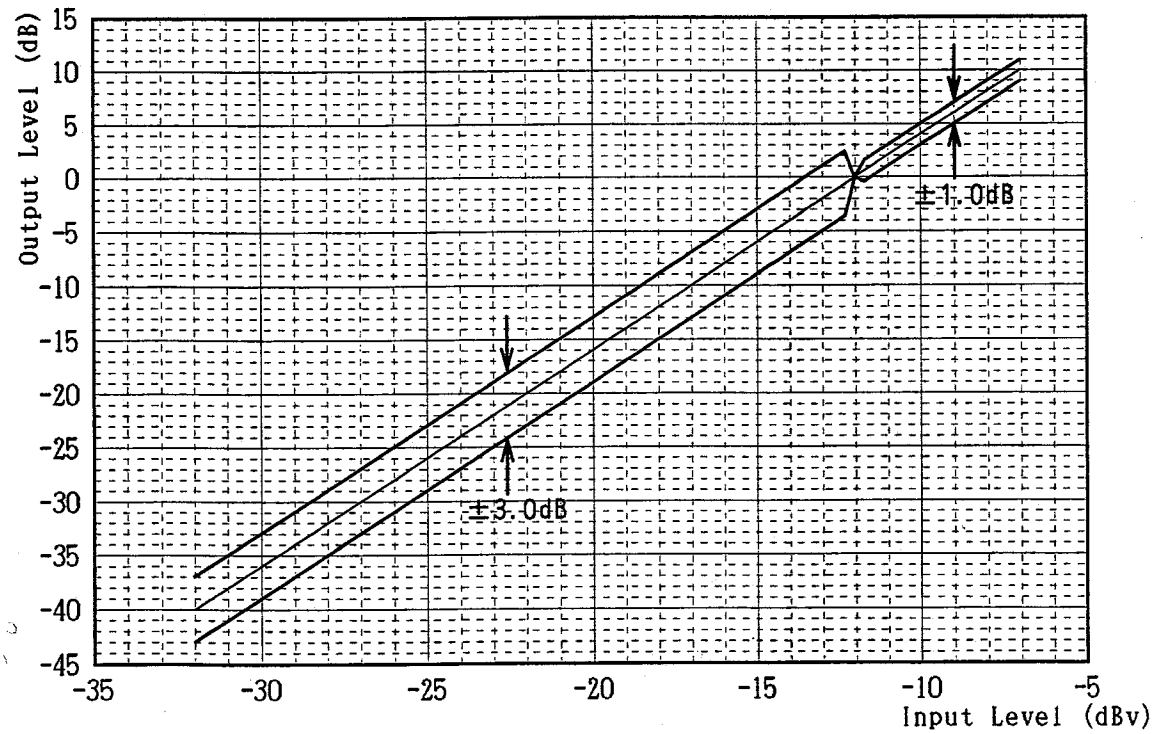
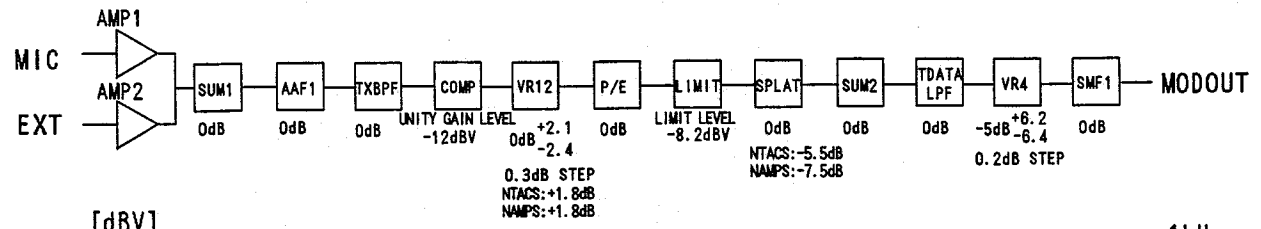
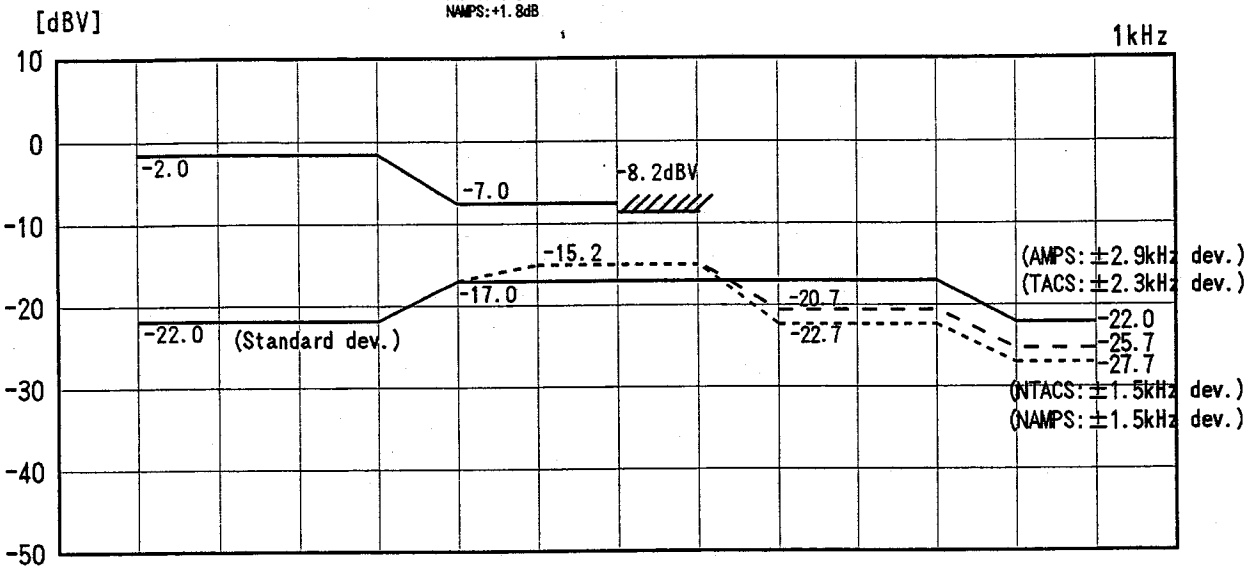


Fig-8 EXPANDER LINEARITY

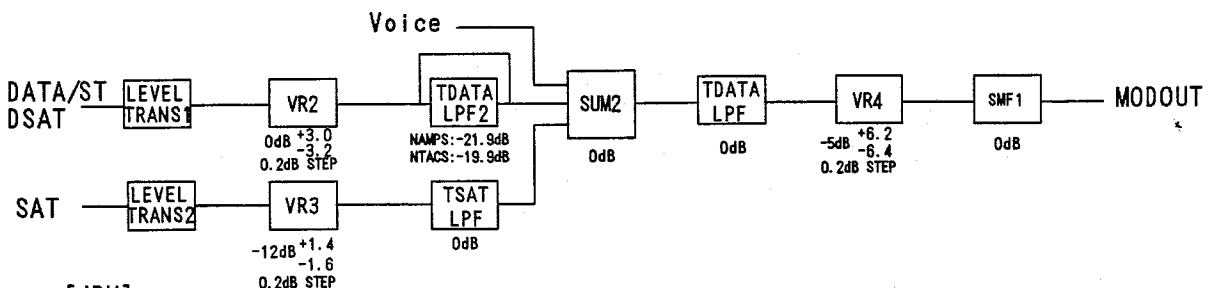
Level Diagrams

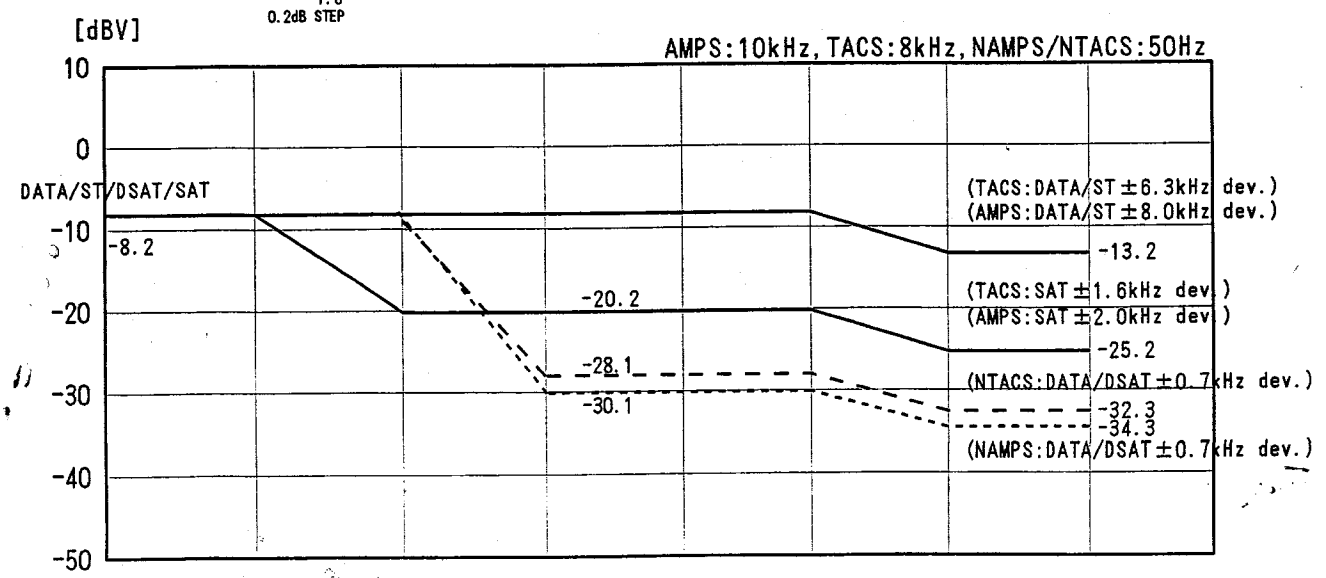
VDD=3.0V, 0dBV=1Vrms

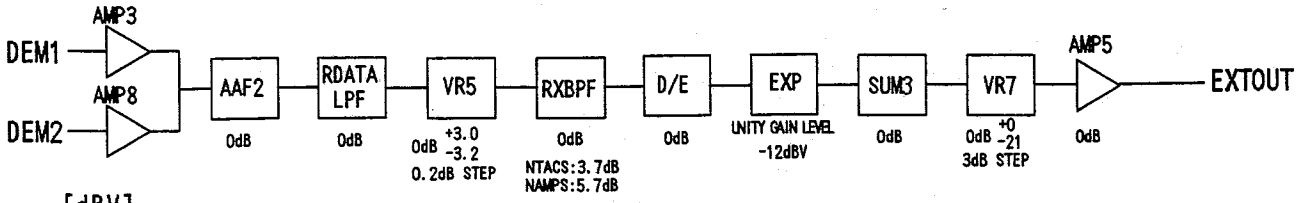


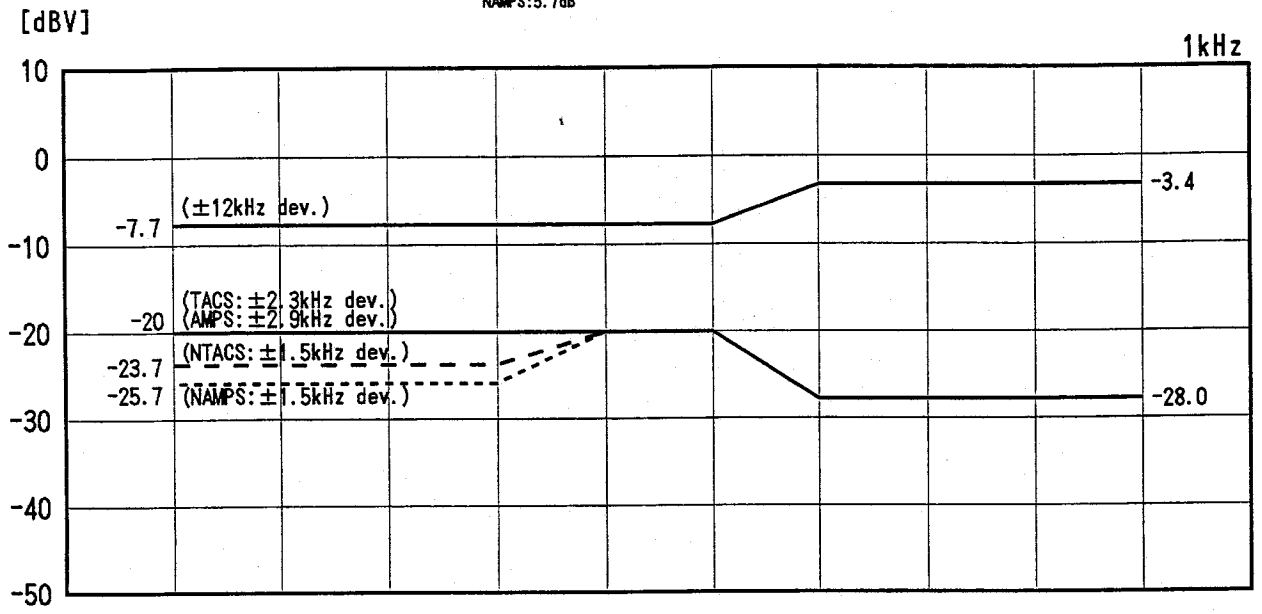


Transmit Voice Signal Level Diagram

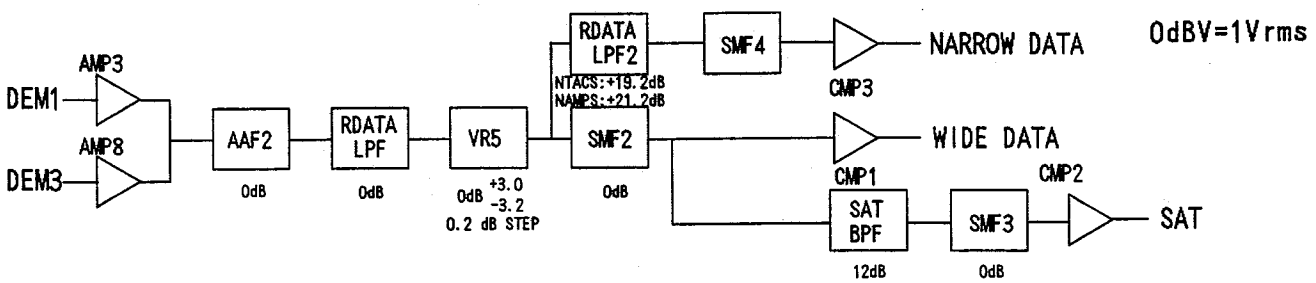


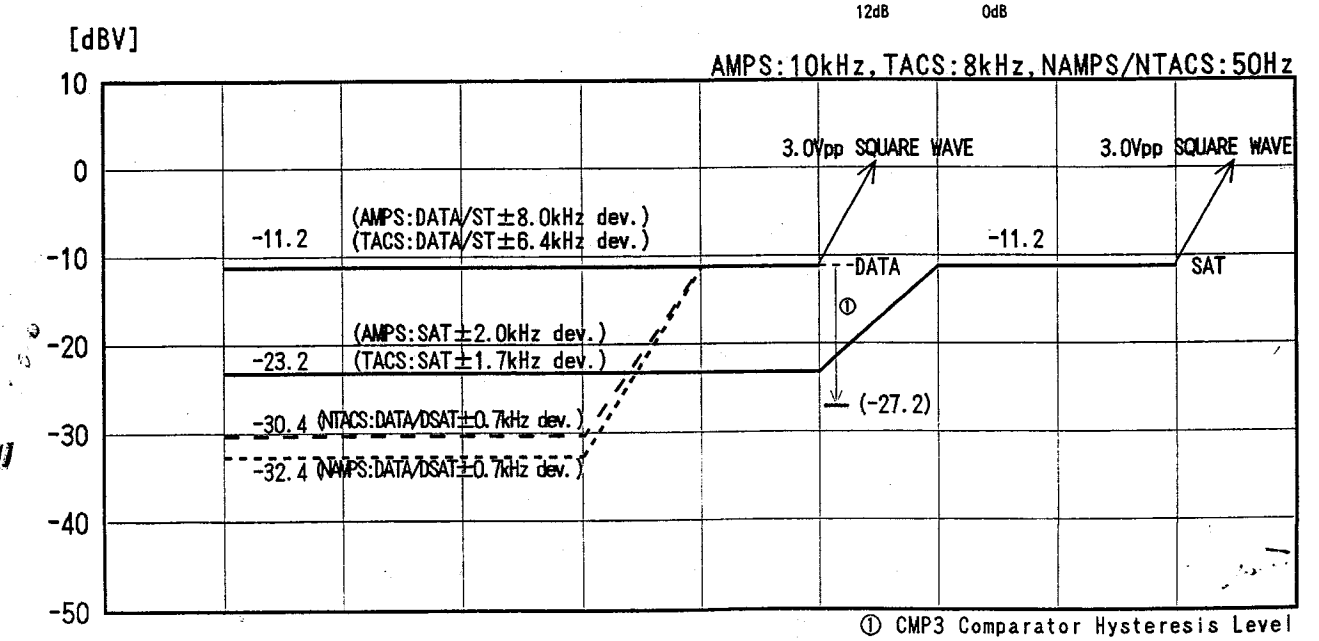




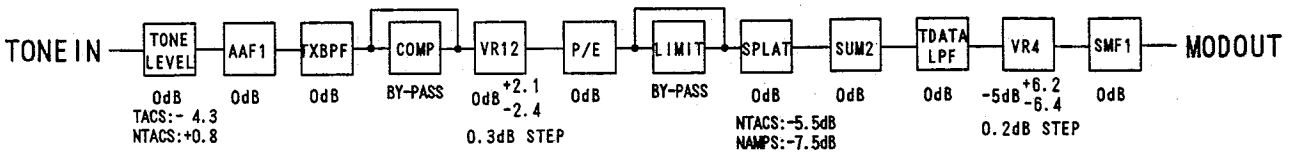


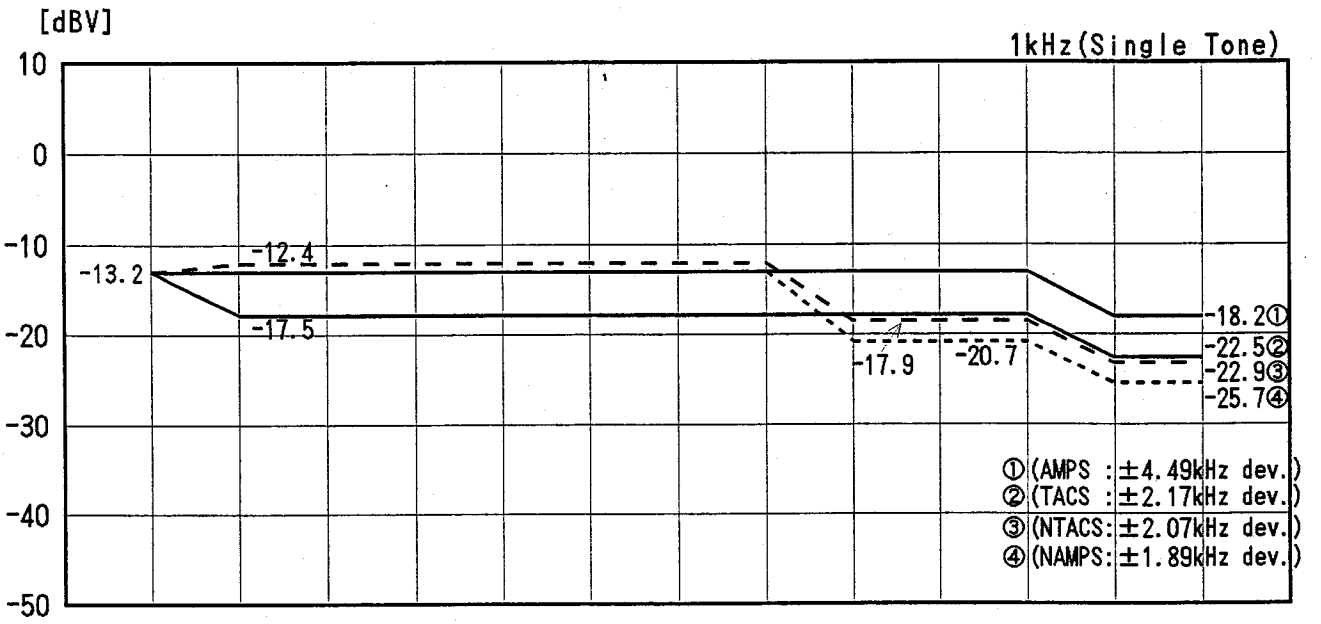
Receive Voice Signal Level Diagram





① CMP3 Comparator Hysteresis Level





Transmit DTMF Signal Level Diagram

Register

■ REGISTER MAP

《WRITE》

Address	Register Name
00	POWER DOWN MODE CONTROL
01	SYSTEM CONTROL
02	RECEIVE DATA CONTROL
03	TRANSMIT DATA CONTROL
04	VOICE PATH CONTROL
05	VR1x GAIN SET
06	VR2 GAIN SET
07	VR4 GAIN SET
08	VR5 GAIN SET
09	VR6 GAIN SET
0A	VR7 GAIN SET
0B	VR8 GAIN SET and HANDS-FREE
10	DTMF HIGH FREQ
11	DTMF LOW FREQ
12	SWITCH, DTMF and SIDETONE
13	SAT CONTROL and VR3 GAIN SET
14	DA1 OUTPUT VOLTAGE
15	DA2 OUTPUT VOLTAGE
16	DA3 OUTPUT VOLTAGE
17	COMPANDOR LINEARITY ADJUST
18	PROGRAMMABLE I/O DIRECTION
19	PROGRAMMABLE I/O WRITE DATA
20	PROGRAMMABLE I/O DIRECTION
21	PROGRAMMABLE I/O WRITE DATA
22	TIMER1 PRESET VALUE
23	TIMER2 PRESET VALUE
24	TIMER1 CONTROL
25	TIMER2 CONTROL
26	DRX INTERVAL

Address	Register Name
27	AFC CONTROL
28	SYSTEM CONTROL2
30	DATA PROCESSOR CONTROL
31	DATA RECOVERY CONTROL
40	INTERRUPT MASK REGISTER 1
41	INTERRUPT MASK REGISTER 2
50	TEST MODE (RESERVED)
51	TEST MODE (RESERVED)
60	TXCTRL SET
61	TXCTRL RESET
62	TX ABORT
63	RX MUTE RESET
64	CLEAR TX BUFFER
65	RESTART WORD SYNC
66	RXCTRL SET
67	RXCTRL RESET
68	TX BUFFER HOLD
69	TX START
6A	RESET
70	MIN1 (23 ~ 16)
71	MIN1 (15 ~ 8)
72	MIN1 (7 ~ 0)
73	MIN2 (33 ~ 26)
74	MIN2 (25 ~ 24)
75	DCC
76	TX DATA (35 ~ 28)
77	TX DATA (27 ~ 20)
78	TX DATA (19 ~ 12)
79	TX DATA (11 ~ 4)
7A	TX DATA (3 ~ 0)

《READ》

Address	Register Name
80	DATA PROCESSOR STATUS
81	STATUS WORD 1
82	STATUS WORD 2
83	EVENT REGISTER 1
84	EVENT REGISTER 2
85	PROGRAMMABLE I/O DATA
86	TIMER1 STATUS
87	TIMER2 STATUS
88	AFC COUNTER DATA (HIGH)
89	AFC COUNTER DATA (LOW)
8A	PROGRAMMABLE I/O DATA (P8, P9)
90	SPM1 (27 ~ 20)
91	SPM1 (19 ~ 12)
92	SPM1 (11 ~ 4)
93	SPM1 (3 ~ 0)
94	SPM2 (27 ~ 20)
95	SPM2 (19 ~ 12)
96	SPM2 (11 ~ 4)
97	SPM2 (3 ~ 0)
98	OHM1 (27 ~ 20)
99	OHM1 (19 ~ 12)
9A	OHM1 (11 ~ 4)
9B	OHM1 (3 ~ 0)
9C	OHM2 (27 ~ 20)
9D	OHM2 (19 ~ 12)
9E	OHM2 (11 ~ 4)
9F	OHM2 (3 ~ 0)
A0	OHM3 (27 ~ 20)
A1	OHM3 (19 ~ 12)
A2	OHM3 (11 ~ 4)
A3	OHM3 (3 ~ 0)

Address	Register Name
A4	OHM4 (27 ~ 20)
A5	OHM4 (19 ~ 12)
A6	OHM4 (11 ~ 4)
A7	OHM4 (3 ~ 0)
A8	OHM5 (27 ~ 20)
A9	OHM5 (19 ~ 12)
AA	OHM5 (11 ~ 4)
AB	OHM5 (3 ~ 0)
AC	OHM6 (27 ~ 20)
AD	OHM6 (19 ~ 12)
AE	OHM6 (11 ~ 4)
AF	OHM6 (3 ~ 0)
B0	OHM7 (27 ~ 20)
B1	OHM7 (19 ~ 12)
B2	OHM7 (11 ~ 4)
B3	OHM7 (3 ~ 0)
B4	OHM8 (27 ~ 20)
B5	OHM8 (19 ~ 12)
B6	OHM8 (11 ~ 4)
B7	OHM8 (3 ~ 0)
B8	OHM9 (27 ~ 20)
B9	OHM9 (19 ~ 12)
BA	OHM9 (11 ~ 4)
BB	OHM9 (3 ~ 0)
BC	OHM10 (27 ~ 20)
BD	OHM10 (19 ~ 12)
BE	OHM10 (11 ~ 4)
BF	OHM10 (3 ~ 0)

《READ》

Address	Register Name
C 0	OHM11 (27 ~ 20)
C 1	OHM11 (19 ~ 12)
C 2	OHM11 (11 ~ 4)
C 3	OHM11 (3 ~ 0)
C 4	OHM12 (27 ~ 20)
C 5	OHM12 (19 ~ 12)
C 6	OHM12 (11 ~ 4)
C 7	OHM12 (3 ~ 0)
C 8	OHM13 (27 ~ 20)
C 9	OHM13 (19 ~ 12)
C A	OHM13 (11 ~ 4)
C B	OHM13 (3 ~ 0)
C C	OHM14 (27 ~ 20)
C D	OHM14 (19 ~ 12)
C E	OHM14 (11 ~ 4)
C F	OHM14 (3 ~ 0)
D 0	CFM (27 ~ 20)
D 1	CFM (19 ~ 12)
D 2	CFM (11 ~ 4)
D 3	CFM (3 ~ 0)
D 4	1st MSCM WORD (27 ~ 20)
D 5	1st MSCM WORD (19 ~ 12)
D 6	1st MSCM WORD (11 ~ 4)
D 7	1st MSCM WORD (3 ~ 0)
D 8	2nd MSCM WORD (27 ~ 20)
D 9	2nd MSCM WORD (19 ~ 12)
D A	2nd MSCM WORD (11 ~ 4)
D B	2nd MSCM WORD (3 ~ 0)

Address	Register Name
D C	3rd MSCM WORD (27 ~ 20)
D D	3rd MSCM WORD (19 ~ 12)
D E	3rd MSCM WORD (11 ~ 4)
D F	3rd MSCM WORD (3 ~ 0)
E 0	RX DATA (27 ~ 20)
E 1	RX DATA (19 ~ 12)
E 2	RX DATA (11 ~ 4)
E 3	RX DATA (3 ~ 0)

ADD (Address) CONTROL WORDS (Register Name)

NOTE: Value inside ( ) indicates the initial value

CONTROL REGISTER (WRITE)

00 POWER DOWN MODE CONTROL

bit0 (0)
1 (0)
2 (0)
3 (0) } Power Down Mode

4 (0) AMP7 Control
5 (0) DA1 Control
6 (0) DA2 Control
7 (0) DA3 Control

bit0	0	
	1	RX DATA BLOCK ON
1	0	
	1	RX TONE BLOCK ON
2	0	
	1	TX DATA BLOCK ON
3	0	
	1	VOICE BLOCK & ON
4	0	AMP7 Power Down
	1	AMP7 Normal Operation
5	0	DA1 Power Down
	1	DA1 Normal Operation
6	0	DA2 Power Down
	1	DA2 Normal Operation
7	0	DA3 Power Down
	1	DA3 Normal Operation

} (NOTE)

NOTE : POWER DOWN MODE COMBINATION

bit3	bit2	bit1	bit0	POWER DOWN MODE
0	0	0	0	Mode 0 (SHUT DOWN Mode)
0	0	0	1	Mode 1 (RX DATA Mode)
0	0	1	1	Mode 2 (RX DATA & RX TONE Mode)
0	1	0	1	Mode 3 (RX DATA & TX DATA Mode)
0	1	1	1	Mode 4 (RX DATA & RX TONE & TX DATA Mode)
1	1	1	1	Mode 5 (Full Operation)

*Only the above combination is allowed.

01 SYSTEM CONTROL

bit0 (0) AMPS/TACS SELECT
1 (0) TXINV
2 (0) RXINV
3 (0) RX AUTO MUTE ENABLE
4 (0) DRX ENABLE
5 (0) VOX ENABLE
6 (0) INT POLARITY
7 (0) WIDE/NARROW SELECT

bit0	0	AMPS
	1	TACS
1	0	TX DATA Non-inversion
	1	TX DATA Inversion
2	0	RX DATA Non-inversion
	1	RX DATA Inversion
3	0	RX Auto Mute Disable
	1	RX Auto Mute Enable
4	0	Discontinuos Reception Disable
	1	Discontinuos Reception Enable
5	0	VOX OFF
	1	VOX ON
6	0	INT pin goes "H" at Interrupt
	1	INT pin goes "L" at Interrupt
7	0	Wide Analog Mode
	1	Narrow Analog Mode

AMPS/TACS and Wide/Narrow gain select

		VR11	TONE LEVEL	SPLAT	TDATALPF2	RXBPF	RDATALPF2
AMPS	Wide	0dB	0dB	0dB	—	0dB	—
	Narrow	+1.8dB	0dB	-7.5dB	-21.1dB	+5.7dB	+21.2dB
TACS	Wide	0dB	-4.3dB	0dB	—	0dB	—
	Narrow	+1.8dB	+0.8dB	-5.5dB	-19.1dB	+3.7dB	+19.2dB

Wide/Narrow switch (WNSW1～3) select

	WNSW1	WNSW2	WNSW3 (*)
Wide	VR2	VSS	AMP3
Narrow	TDATA LPF2	CMP3	AMP8/AMP3

*When Narrow Analog Mode is selected, WNSW3 is controlled from the control register address 28.

02 RECEIVE DATA CONTROL

bit0 (0) } ECC MODE SELECT (2 bit)
1 (0) }
2 (0) DISCONTINUOUS RECEPTION MODE SELECT
3 (0) DATA PROCESSOR ENABLE
4 (0) CONTROL CHANNEL / VOICE CHANNEL SELECT
5 (0) STREAM A/B SELECT (FOCC)
6 (0) R/L MODE SELECT

bit1, 0	0x	No Error Correction
	10	1 Bit Error Correction
	11	2 Bit Error Correction
2	0	3 Consecutive Data Correspondence (3/3)
	1	2 Consecutive Data Correspondence (2/2)
3	0	Data Processor Disable
	1	Data Processor Enable
4	0	Control Channel
	1	Voice Channel
5	0	Stream A
	1	Stream B
6	0	Processed B/I Bit (Note)
	1	Non-processed B/I Bit

Note:

Processed	BUSY/IDLE detect by continuous 2 bit data
Non-Processed	BUSY/IDLE detect by 1 bit data directly

03 TRANSMIT DATA CONTROL

bit0 (0) ARBITRATION ENABLE
1 (0) DTXSW (DTXAMP ON/OFF)
2 (0) SW6
3 (0) SW7
4 (0) DSAT/DST SELECT
5 (0), 6 (0), 7 (0) 24 BIT TRANSMIT DSAT SEQUENCE SELECT

bit0	0	Arbitration Disable
	1	Arbitration Enable
1	0	DTXAMP OFF
	1	DTXAMP ON
2	0	TX DATA
	1	ST
3	0	TX DATA MUTE
	1	TX DATA ON
4	0	DSAT DATA
	1	DST DATA

DSAT/DST/Bit Mask

bit7	bit6	bit5	DSAT	DST	Bit Mask
0	0	0	(#0) 2556CB	(#0) DAA934	FF003E
0	0	1	(#1) 255B2B	(#1) DAA4D4	0BBF82
0	1	0	(#2) 256A9B	(#2) DA9564	BD780F
0	1	1	(#3) 25AD4D	(#3) DA52B2	3FF118
1	0	0	(#4) 26AB2B	(#4) D954D4	0AE6F6
1	0	1	(#5) 26B2AD	(#5) D94D52	8001FF
1	1	0	(#6) 2969AB	(#6) D69654	1C0FCD

04 VOICE PATH CONTROL

bit0 (0) COMP (SW4, SW11)
1 (0) SW5
2 (0) SW1
3 (0) SW2
4 (0) SW10
5 (0) SW13
6 (0) SW14
7 (0) SW15

bit0	0	Compandor Bypass
	1	Compandor ON
1	0	TX VOICE MUTE
	1	TX VOICE ON
2	0	MIC OFF
	1	MIC ON
3	0	EXT OFF
	1	EXT ON
4	0	RX VOICE MUTE
	1	RX VOICE ON
5	0	REC1 OFF
	1	REC1 ON
6	0	EXTOUT OFF
	1	EXTOUT ON
7	0	REC2 OFF
	1	REC2 ON

05 VR1x (4bit) GAIN SET : -2.4～+2.1dB (0.3dB step) (x = 1, 2)

bit7	6	5	4	3	2	1	0
(1)	(0)	(0)	(0)	(1)	(0)	(0)	(0)
VR113	VR112	VR111	VR110	VR123	VR122	VR121	VR110
VR11 (MIC/EXT)				VR12 (TONE)			

VR1X3	VR1X2	VR1X1	VR1X0	GAIN
0	0	0	0	-2.4 dB
0	0	0	1	-2.1 dB
0	0	1	0	-1.8 dB
0	0	1	1	-1.5 dB
0	1	0	0	-1.2 dB
0	1	0	1	-0.9 dB
0	1	1	0	-0.6 dB
0	1	1	1	-0.3 dB
1	0	0	0	0.0 dB
1	0	0	1	+0.3 dB
1	0	1	0	+0.6 dB
1	0	1	1	+0.9 dB
1	1	0	0	+1.2 dB
1	1	0	1	+1.5 dB
1	1	1	0	+1.8 dB
1	1	1	1	+2.1 dB

＊VR11: X = 1, VR12: X = 2

06 VR2 (5bit) GAIN SET : -3.2～+3.0dB (0.2dB step)

bit 7	6	5	4	3	2	1	0
(1)	(0)	(0)	(0)	(0)	-	-	-
VR24	VR23	VR22	VR21	VR20			

VR2

VR24	VR23	VR22	VR21	VR20	GAIN
0	0	0	0	0	-3.2 dB
0	0	0	0	1	-3.0 dB
0	0	0	1	0	-2.8 dB
0	0	0	1	1	-2.6 dB
0	0	1	0	0	-2.4 dB
0	0	1	0	1	-2.2 dB
0	0	1	1	0	-2.0 dB
0	0	1	1	1	-1.8 dB
0	1	0	0	0	-1.6 dB
0	1	0	0	1	-1.4 dB
0	1	0	1	0	-1.2 dB
0	1	0	1	1	-1.0 dB
0	1	1	0	0	-0.8 dB
0	1	1	0	1	-0.6 dB
0	1	1	1	0	-0.4 dB
0	1	1	1	1	-0.2 dB

VR2

VR24	VR23	VR22	VR21	VR20	GAIN
1	0	0	0	0	0.0 dB
1	0	0	0	1	+0.2 dB
1	0	0	1	0	+0.4 dB
1	0	0	1	1	+0.6 dB
1	0	1	0	0	+0.8 dB
1	0	1	0	1	+1.0 dB
1	0	1	1	0	+1.2 dB
1	0	1	1	1	+1.4 dB
1	1	0	0	0	+1.6 dB
1	1	0	0	1	+1.8 dB
1	1	0	1	0	+2.0 dB
1	1	0	1	1	+2.2 dB
1	1	1	0	0	+2.4 dB
1	1	1	0	1	+2.6 dB
1	1	1	1	0	+2.8 dB
1	1	1	1	1	+3.0 dB

07 VR4 (6bit) GAIN SET : -11.4～+1.2dB (0.2dB step)

bit 7	6	5	4	3	2	1	0
		(1)	(0)	(0)	(0)	(0)	(0)
-	-	VR45	VR44	VR43	VR42	VR41	VR40

VR4

VR45	VR44	VR43	VR42	VR41	VR40	GAIN
0	0	0	0	0	0	-11.4 dB
0	0	0	0	0	1	-11.2 dB
0	0	0	0	1	0	-11.0 dB
0	0	0	0	1	1	-10.8 dB
0	0	0	1	0	0	-10.6 dB
0	0	0	1	0	1	-10.4 dB
0	0	0	1	1	0	-10.2 dB
0	0	0	1	1	1	-10.0 dB
0	0	1	0	0	0	- 9.8 dB
0	0	1	0	0	1	- 9.6 dB
0	0	1	0	1	0	- 9.4 dB
0	0	1	0	1	1	- 9.2 dB
0	0	1	1	0	0	- 9.0 dB
0	0	1	1	0	1	- 8.8 dB
0	0	1	1	1	0	- 8.6 dB
0	0	1	1	1	1	- 8.4 dB
0	1	0	0	0	0	- 8.2 dB
0	1	0	0	0	1	- 8.0 dB
0	1	0	0	1	0	- 7.8 dB
0	1	0	0	1	1	- 7.6 dB
0	1	0	1	0	0	- 7.4 dB
0	1	0	1	0	1	- 7.2 dB
0	1	0	1	1	0	- 7.0 dB
0	1	0	1	1	1	- 6.8 dB
0	1	1	0	0	0	- 6.6 dB
0	1	1	0	0	1	- 6.4 dB
0	1	1	0	1	0	- 6.2 dB
0	1	1	0	1	1	- 6.0 dB
0	1	1	1	0	0	- 5.8 dB
0	1	1	1	0	1	- 5.6 dB
0	1	1	1	1	0	- 5.4 dB
0	1	1	1	1	1	- 5.2 dB

VR4

VR45	VR44	VR43	VR42	VR41	VR40	GAIN
1	0	0	0	0	0	- 5.0 dB
1	0	0	0	0	1	- 4.8 dB
1	0	0	0	1	0	- 4.6 dB
1	0	0	0	1	1	- 4.4 dB
1	0	0	1	0	0	- 4.2 dB
1	0	0	1	0	1	- 4.0 dB
1	0	0	1	1	0	- 3.8 dB
1	0	0	1	1	1	- 3.6 dB
1	0	1	0	0	0	- 3.4 dB
1	0	1	0	0	1	- 3.2 dB
1	0	1	0	1	0	- 3.0 dB
1	0	1	0	1	1	- 2.8 dB
1	0	1	1	0	0	- 2.6 dB
1	0	1	1	0	1	- 2.4 dB
1	0	1	1	1	0	- 2.2 dB
1	0	1	1	1	1	- 2.0 dB
1	1	0	0	0	0	- 1.8 dB
1	1	0	0	0	1	- 1.6 dB
1	1	0	0	1	0	- 1.4 dB
1	1	0	0	1	1	- 1.2 dB
1	1	0	1	0	0	- 1.0 dB
1	1	0	1	0	1	- 0.8 dB
1	1	0	1	1	0	- 0.6 dB
1	1	0	1	1	1	- 0.4 dB
1	1	1	0	0	0	- 0.2 dB
1	1	1	0	0	1	0.0 dB
1	1	1	0	1	0	+ 0.2 dB
1	1	1	0	1	1	+ 0.4 dB
1	1	1	1	0	0	+ 0.6 dB
1	1	1	1	0	1	+ 0.8 dB
1	1	1	1	1	0	+ 1.0 dB
1	1	1	1	1	1	+ 1.2 dB

08 VR5 (5bit) GAIN SET : -3.2～+3.0dB (0.2dB step)

bit7	6	5	4	3	2	1	0
			(1)	(0)	(0)	(0)	(0)
-	-	-	VR54	VR53	VR52	VR51	VR50

VR5

VR54	VR53	VR52	VR51	VR50	GAIN
0	0	0	0	0	-3.2 dB
0	0	0	0	1	-3.0 dB
0	0	0	1	0	-2.8 dB
0	0	0	1	1	-2.6 dB
0	0	1	0	0	-2.4 dB
0	0	1	0	1	-2.2 dB
0	0	1	1	0	-2.0 dB
0	0	1	1	1	-1.8 dB
0	1	0	0	0	-1.6 dB
0	1	0	0	1	-1.4 dB
0	1	0	1	0	-1.2 dB
0	1	0	1	1	-1.0 dB
0	1	1	0	0	-0.8 dB
0	1	1	0	1	-0.6 dB
0	1	1	1	0	-0.4 dB
0	1	1	1	1	-0.2 dB
1	0	0	0	0	0.0 dB
1	0	0	0	1	+0.2 dB
1	0	0	1	0	+0.4 dB
1	0	0	1	1	+0.6 dB
1	0	1	0	0	+0.8 dB
1	0	1	0	1	+1.0 dB
1	0	1	1	0	+1.2 dB
1	0	1	1	1	+1.4 dB
1	1	0	0	0	+1.6 dB
1	1	0	0	1	+1.8 dB
1	1	0	1	0	+2.0 dB
1	1	0	1	1	+2.2 dB
1	1	1	0	0	+2.4 dB
1	1	1	0	1	+2.6 dB
1	1	1	1	0	+2.8 dB
1	1	1	1	1	+3.0 dB

09 VR6 (2bit) GAIN SET : -18.0～+0.0dB (6.0dB step)

bit7	6	5	4	3	2	1	0
						(0)	(0)
-	-	-	-	-	-	VR61	VR60

VR6

VR61	VR60	GAIN
0	0	-18 dB
0	1	-12 dB
1	0	- 6 dB
1	1	0 dB

0A VR7 (3bit) GAIN SET : -21.0～+0.0dB (3.0dB step)

bit7	6	5	4	3	2	1	0
					(0)	(0)	(0)
-	-	-	-	-	VR72	VR71	VR70

VR7

VR72	VR71	VR70	GAIN
0	0	0	-21 dB
0	0	1	-18 dB
0	1	0	-15 dB
0	1	1	-12 dB
1	0	0	- 9 dB
1	0	1	- 6 dB
1	1	0	- 3 dB
1	1	1	0 dB

0B VR8 (3bit) GAIN SET : -21.0～+0.0dB (3.0dB step) and HANDS-FREE PASS

bit7	6	5	4	3	2	1	0
				(0)	(0)	(0)	(0)
-	-	-	-	SWHF	VR82	VR81	VR80

VR8

VR82	VR81	VR80	GAIN
0	0	0	-21 dB
0	0	1	-18 dB
0	1	0	-15 dB
0	1	1	-12 dB
1	0	0	- 9 dB
1	0	1	- 6 dB
1	1	0	- 3 dB

Hands-Free Switch Select

SWHF	0	Normal (EXP out)
	1	Hands-Free Pass (HFIN)

10 DTMF HIGH FREQ

bit7	6	5	4	3	2	1	0
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
DTH7	DTH6	DTH5	DTH4	DTH3	DTH2	DTH1	DTH0

11 DTMF LOW FREQ

bit7	6	5	4	3	2	1	0
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
DTL7	DTL6	DTL5	DTL4	DTL3	DTL2	DTL1	DTL0

The frequency of each DTMF high and low is determined as follows;

f = 1.2 MHz / (Register Value + 1) / 16

Example	DTX7	DTX0	(X=L or H)	Actual	Error (%)
1209 Hz	00111101		(61)	1209.7 Hz	+0.06
1336 Hz	00110111		(55)	1339.3 Hz	+0.25
1477 Hz	00110010		(50)	1470.6 Hz	-0.43
1633 Hz	00101101		(45)	1630.4 Hz	-0.16
697 Hz	01101011		(107)	694.4 Hz	-0.37
770 Hz	01100000		(96)	773.2 Hz	+0.42
852 Hz	01010111		(87)	852.3 Hz	+0.04
941 Hz	01001111		(79)	937.5 Hz	-0.37

12 SWITCH, DTMF and SIDETONE CONTROL

bit7	6	5	4	3	2	1	0
		(0)	(0)	(0)	(0)	(0)	(0)
-	-	SW16	LIMSW	SW3	SW12	DTMFH	DTMFL

bit0	0	DTMF Low OFF
	1	DTMF Low ON
1	0	DTMF High OFF
	1	DTMF High ON
2	0	RX Tone OFF
	1	RX Tone ON
3	0	TX Voice
	1	TX Tone
4	0	LIMIT ON
	1	LIMIT OFF
5	0	Sidetone ON
	1	Sidetone MUTE

13 SAT CONTROL and VR3 GAIN SET

bit7	6	5	4	3	2	1	0
(1)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
VR33	VR32	VR31	VR30	SW9	SW8	SCC1	SCC0

VR3

bit1, 0	00	5970 Hz
	01	6000 Hz
	1x	6030 Hz
2	0	RECOVERED SAT
	1	GENERATED SAT
bit3	0	SAT Transpond OFF
	1	SAT Transpond ON

VR3

VR33	VR32	VR31	VR30	GAIN
0	0	0	0	-13.6 dB
0	0	0	1	-13.4 dB
0	0	1	0	-13.2 dB
0	0	1	1	-13.0 dB
0	1	0	0	-12.8 dB
0	1	0	1	-12.6 dB
0	1	1	0	-12.4 dB
0	1	1	1	-12.2 dB
1	0	0	0	-12.0 dB
1	0	0	1	-11.8 dB
1	0	1	0	-11.6 dB
1	0	1	1	-11.4 dB
1	1	0	0	-11.2 dB
1	1	0	1	-11.0 dB
1	1	1	0	-10.8 dB
1	1	1	1	-10.6 dB

14 DA1 OUTPUT VOLTAGE

bit7	6	5	4	3	2	1	0
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10

15 DA2 OUTPUT VOLTAGE

bit7	6	5	4	3	2	1	0
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

16 DA3 OUTPUT VOLTAGE

bit7	6	5	4	3	2	1	0
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
DA37	DA36	DA35	DA34	DA33	DA32	DA31	DA30

The output voltage of DAC1, 2 and 3 are defined as follows; (x: DAC No.)

DAx7	DAx6	DAx5	DAx4	DAx3	DAx2	DAx1	DAx0	OUTPUT
0	0	0	0	0	0	0	0	0.020000 VDD
0	0	0	0	0	0	0	1	0.023765 VDD
≀	≀	≀	≀	≀	≀	≀	≀	≀ 0.003765 VDD Step ≀
1	1	1	1	1	1	1	0	0.976235 VDD
1	1	1	1	1	1	1	1	0.980000 VDD

17 COMPANDOR LINEARITY ADJUST

bit 7	6	5	4	3	2	1	0
(1)	(0)	(0)	(0)	(1)	(0)	(0)	(0)
CMP3	CMP2	CMP1	CMP0	EXP3	EXP2	EXP1	EXP0
COMPRESSOR				EXPANDER			

COMPRESSOR (MIC2=-52dBV)

CMP3	CMP2	CMP1	CMP0	ADJUST
0	0	0	0	-2.4 dB
0	0	0	1	-2.1 dB
0	0	1	0	-1.8 dB
0	0	1	1	-1.5 dB
0	1	0	0	-1.2 dB
0	1	0	1	-0.9 dB
0	1	1	0	-0.6 dB
0	1	1	1	-0.3 dB
1	0	0	0	0.0 dB
1	0	0	1	+0.3 dB
1	0	1	0	+0.6 dB
1	0	1	1	+0.9 dB
1	1	0	0	+1.2 dB
1	1	0	1	+1.5 dB
1	1	1	0	+1.8 dB
1	1	1	1	+2.1 dB

EXPANDER (EXPIN=-32dBV)

EXP3	EXP2	EXP1	EXP0	ADJUST
0	0	0	0	-3.2 dB
0	0	0	1	-2.8 dB
0	0	1	0	-2.4 dB
0	0	1	1	-2.0 dB
0	1	0	0	-1.6 dB
0	1	0	1	-1.2 dB
0	1	1	0	-0.8 dB
0	1	1	1	-0.4 dB
1	0	0	0	0.0 dB
1	0	0	1	+0.4 dB
1	0	1	0	+0.8 dB
1	0	1	1	+1.2 dB
1	1	0	0	+1.6 dB
1	1	0	1	+2.0 dB
1	1	1	0	+2.4 dB
1	1	1	1	+2.8 dB

*These adjust levels are reference data to adjust the linearity and not guaranteed.

18 PROGRAMMABLE I/O DIRECTION (P8, P9)

bit7	6	5	4	3	2	1	0
						(0)	(0)
-	-	-	-	-	-	IO9	IO8

bit x	0	Input
	1	Output

19 PROGRAMMABLE I/O WRITE DATA (P8, P9)

bit7	6	5	4	3	2	1	0
						(0)	(0)
-	-	-	-	-	-	PO9	PO8

20 PROGRAMMABLE I/O DIRECTION (P0～P7)

bit7	6	5	4	3	2	1	0
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0

bitx	0	Input
	1	Output

21 PROGRAMMABLE I/O WRITE DATA (P0～P7)

bit7	6	5	4	3	2	1	0
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0

22 TIMER1 PRESET VALUE

bit7	6	5	4	3	2	1	0
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
T17	T16	T15	T14	T13	T12	T11	T10

23 TIMER2 PRESET VALUE

bit7	6	5	4	3	2	1	0
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
T27	T26	T25	T24	T23	T22	T21	T20

24 TIMER1 CONTROL

bit7	6	5	4	3	2	1	0
		(0)	(0)	(0)	(0)	(0)	(0)
-	-	T1POL	T1RPT	T1CK1	T1CK0	T1CTRL1	T1CTRL0
				TIMER1 MAIN CLOCK SELECT		TIMER1 CONTROL	

TIMER1 CONTROL

bit1, 0	00	Stop TIMER1 and Keep The Current Value
	10	Load The Current Value to the Read Register
	01	TIMER1 Start from The Initial Value
	11	TIMER1 Start from The Current Value

TIMER1 MAIN CLOCK

bit3, 2	00	12.5kHz
	01	6.25kHz
	10	3.125kHz
	11	1.5625kHz

bit4	0	Normal
	1	Repeat Automatically
bit5	0	TEXP1 pin goes "H" at expire
	1	TEXP1 pin goes "L" at expire

25 TIMER2 CONTROL

bit7	6	5	4	3	2	1	0
		(0)	(0)	(0)	(0)	(0)	(0)
-	-	T2POL	T2RPT	T2CK1	T2CK0	T2CTRL1	T2CTRL0
				TIMER2 MAIN CLOCK SELECT		TIMER2 CONTROL	

TIMER2 CONTROL

bit1, 0	00	Stop TIMER2 and Keep The Current Value
	10	Load The Current Value to the Read Register
	01	TIMER2 Start from The Initial Value
	11	TIMER2 Start from The Current Value

TIMER2 MAIN CLOCK

bit3, 2	00	781.25Hz
	01	390.625Hz
	10	195.3125Hz
	11	97.65625Hz

bit4	0	Normal
	1	Repeat Automatically
bit5	0	TEXP2 pin goes "H" at expire
	1	TEXP2 pin goes "L" at expire

26 DRX INTERVAL

bit7	6	5	4	3	2	1	0
		(0)	(0)	(0)	(0)	(0)	(0)
-	-	DRX5	DRX4	DRX3	DRX2	DRX1	DRX0

DRX5	DRX4	DRX3	DRX2	DRX1	DRX0	Interval Time
0	0	0	0	0	0	1ms
0	0	0	0	0	1	2ms
≀	≀	≀	≀	≀	≀	≀ 1ms step ≀
1	1	1	1	1	0	63ms
1	1	1	1	1	1	64ms

27 AFC CONTROL

bit7	6	5	4	3	2	1	0
-	-	-	-	-	-	(0)	(0)
						AFCSTRT	AFCON

bit 0	0	AFC Circuit OFF
	1	AFC Circuit ON
1	0	AFC Counter Stop
	1	AFC Counter Start

28 SYSTEM CONTROL2

bit7	6	5	4	3	2	1	0
-	-	-	(0)	(0)	(0)	(0)	(0)
			HYS1	HYS2	DEMSW	WDMSW	SATSW

bit 0	0	VSS
	1	CMP2OUT
1	0	VSS
	1	CMP1OUT
2 *	0	WNSW(3) selects AMP8 out at Narrow Mode
	1	WNSW(3) selects AMP3 out at Narrow Mode

*This register is available at Narrow Mode.
(WNSW(3) selects AMP3 out fixedly at Wide Mode).

CMP3 hysteresis level (typ)

bit3, 4	00	-27.2dBV
	01	-33.2dBV
	10	-39.2dBV
	11	No hysteresis

30 DATA PROCESSOR (DP) CONTROL

bit7	6	5	4	3	2	1	0
	(0)	(0)	(0)	(0)	(0)	(0)	(1)
-	MSCM1	MSCM0	DPM4	DPM3	DPM2	DPM1	DPM0
	MSCM Mode		DP Mode				

DATA PROCESSOR MODE

bit0	0	ALL Mode Disable
	1	ALL Mode Enable
bit1	0	MSCM Mode Disable
	1	MSCM Mode Enable
bit2	0	CFM Mode Disable
	1	CFM Mode Enable
bit3	0	OHM Mode Disable
	1	OHM Mode Enable
bit4	0	SPM Mode Disable
	1	SPM Mode Enable

MSCM Mode

bit6, 5	00	OFF
	01	MIN1 Check
	10	
	11	MIN1 & MIN2 Check

31 DATA RECOVERY (DR) CONTROL

bit7	6	5	4	3	2	1	0
-	-	-	-	(0)	(0)	(1)	(0)
				COEFS1	COEFS0	COEFF1	COEFF0
				Data Recovery Slow Coefficient		Data Recovery Fast Coefficient	

Slow Coefficient

bit3, 2	00
	01
	10
	11

Fast Coefficient

bit1, 0	00
	01
	10
	11

40 INTERRUPT MASK REGISTER I (0: Un-Mask, 1: Mask) and INTERRUPT CONDITION

bit0 (0)	DATA PROCESSOR INTERRUPT	:Occur the INTERRUPT (refer to other chapter)
bit1 (0)	TX BUFFER EMPTY	:Occur the BUFFER EMPTY (*1)
bit2 (0)	TX ARBITRATION	:Occur the TX arbitration
bit3 (0)	TXIP	:Change the status [TXIP←→Not TXIP] (*2)
bit4 (0)	FCC WORD SYNC	:Change the status [WORD SYNC←→Not WORD SYNC]
bit5 (0)	B/I	:Change the status [Busy←→Idle]
bit6 (0)	TIMER1 EXPIRE	:Expire
bit7 (0)	TIMER2 EXPIRE	:EXPire

*1) Except CLEAR TX BUFFER, TX ABORT and TX Arbitration

41 INTERRUPT MASK REGISTER I (0: Un-Mask, 1: Mask) and INTERRUPT CONDITION

bit0 (0)	RX DATA READY	:Occur the RX data ready
bit1 (0)	UNCORRECTABLE ERROR	:Occur the uncorrectable error
bit2 (0)	FVC DOTTING	:Detect the FVC DOTTING
bit3 (0)	FVC WORD SYNC	:Change the status [WORD SYNC←→Not WORD SYNC]
bit4 (0)	FVC MESSAGE BEING RECEIVED	:Mute the RX voice pass automatically
bit5 (0)	SAT DETECT/LOST	:Change the status [DETECT←→LOST]
bit6 (0)	AFC COUNTER FINISHED	:AFC COUNTER Expire
bit7 (0)	DRX	:Change the status [MATCHED←→Not MATCHED]

50 TEST MODE (RESERVED)

51 TEST MODE (RESERVED)

COMMANDS (WRITE)

Please write 8 bits suitable data in following address (60～6A) those command is required.

60 TXCTRL SET : TXCTRL pin goes "H" by force.

61 TXCTRL RESET : TXCTRL pin goes "L" by force.

62 TX ABORT : Data transmission is stopped at once.

63 RX MUTE RESET : RX voice pass mute, that is set by "RX MUTE ENABLE" & FVC DOTTING DETECT, is released and also the DOTTING DETECTOR is reset.

64 CLEAR TX BUFFER : TX DATA (address 76～7A) are cleared.

65 RESTART WORD SYNC : WORD SYNC goes into Out-of-frame by force.

66 RXCTRL SET : RXCTRL pin goes "H" by force.

67 RXCTRL RESET : RXCTRL pin goes "L" by force.

68 TX BUFFER HOLD : Data transmission is hold.

69 TX START : Data transmission starts.

6A RESET : All register data are reset.

DATA REGISTER (WRITE)

70 MIN1 (23 - 16)

bit7	6	5	4	3	2	1	0
MIN1 (23 - 16)							

71 MIN1 (15 - 8)

bit7	6	5	4	3	2	1	0
MIN1 (15 - 8)							

72 MIN1 (7 - 0)

bit7	6	5	4	3	2	1	0
MIN1 (7 - 0)							

73 MIN2 (33 - 26)

bit7	6	5	4	3	2	1	0
MIN2 (33 - 26)							

74 MIN2 (25 - 24)

bit7	6	5	4	3	2	1	0
MIN2 (25, 24)		-	-	-	-	-	-

75 DCC (2 BIT)

bit7	6	5	4	3	2	1	0
DCC (1, 0)		-	-	-	-	-	-

76 TX DATA (35 - 28)

77 TX DATA (27 - 20)

78 TX DATA (19 - 12)

79 TX DATA (11 - 4)

7A TX DATA (3 - 0)

bit7	6	5	4	3	2	1	0
TX DATA (3 - 0)				-	-	-	-

STATUS WORDS (READ)

80 DATA PROCESSOR STATUS

BIT7	6	5	4	3	2	1	0
(0)	(x)	(x)	(x)	(x)	(x)	(x)	(x)
DPS7	DPS6	DPS5	DPS4	DPS3	DPS2	DPS1	DPS0

DPS7	DPS0	
0	xxx xxxx	
1001	xxxx	SPM
1010	NAWC	OHM
1011	xxxx	CFM
1100	xx01	MSCM 1 Word
1100	xx10	MSCM 2 Word
1100	xx11	MSCM on and after 3rd Word
1101	xxxx	All

NAWC: Number of Additional Word Coming

MSB goes "1" when an event occurs and is reset to "0" by either read "DATA PROCESSOR STATUS" (address 80) or receiving the next message.

81 STATUS WORD 1

bit0(1)	TX BUFFER EMPTY
bit1(0), bit2(0)	TX ARBITRATION (2bit)
bit3(0)	TXIP
bit4(0)	FCC WORD SYNC
bit5(1)	B/I
bit6(1)	TIMER1 EXPIRE
bit7(1)	TIMER2 EXPIRE

bit0	0	TX Buffer Full
	1	TX Buffer Empty
bit2, 1	0x	
	10	Receive Busy bit before 56th bit
	11	Receive Idle bit till 104th bit
bit3	0	
	1	Transmission in Progress
bit4	0	
	1	FCC Word Synchronization Achieved
bit5	0	Idle
	1	Busy
bit6	0	
	1	Timer 1 Expire
bit7	0	
	1	Timer 2 Expire

82 STATUS WORD 2

bit0 (0) RX DATA READY
bit1 (0), bit2 (0) } ERROR STATUS (2bit)
bit3 (0) FVC DOTTING
bit4 (0) FVC WORD SYNC
bit5 (0) FVC MESSAGE BEING RECEIVED (RX MUTE)
bit6 (0) SAT DET
bit7 (0) DRX

bit0	0	
	1	Receive Data Ready
bit2, 1	00	No Error
	01	1 bit Error Correction being performed
	10	2 bit Error Correction being performed
	11	Uncorrected Error
bit3	0	
	1	FVC Dotting Pattern being detected
bit4	0	
	1	FVC Word Synchronization being achieved
bit5	0	
	1	Receive Pass Mute
bit6	0	No SAT Signal
	1	SAT Signal Detected
bit7	0	
	1	First 3(or2) consecutive Word being matched

83 EVENT REGISTER 1

bit0 (0) DATA PROCESSOR INTERRUPT
bit1 (0) TX BUFFER EMPTY
bit2 (0) TX ARBITRATION
bit3 (0) TXIP
bit4 (0) FCC WORD SYNC
bit5 (0) B/I
bit6 (0) TIMER1 EXPIRE
bit7 (0) TIMER2 EXPIRE

84 EVENT REGISTER 2

bit0 (0) RX DATA READY
bit1 (0) UNCORRECTABLE ERROR
bit2 (0) FVC DOTTING
bit3 (0) FVC WORD SYNC
bit4 (0) FVC MESSAGE BEING RECEIVED (RX MUTE)
bit5 (0) SAT DETECT/LOST
bit6 (0) AFC COUNTER FINISHED
bit7 (0) DRX

*Please refer to the recommended sequence to know the interrupt factors through the EVENT REGISTER1&2 when interrupt is occurred at page 66.

85 PROGRAMMABLE I/O DATA

bit7	6	5	4	3	2	1	0
PI (7 - 0)							

86 TIMER1 STATUS

bit7	6	5	4	3	2	1	0
T1 (7 - 0)							

87 TIMER2 STATUS

bit7	6	5	4	3	2	1	0
T2 (7 - 0)							

88 AFC COUNTER DATA (HIGH)

bit7	6	5	4	3	2	1	0
AFC (15 - 08)							

89 AFC COUNTER DATA (LOW)

bit7	6	5	4	3	2	1	0
AFC (07 - 00)							

8A PROGRAMMABLE I/O DATA

bit7	6	5	4	3	2	1	0
-	-	-	-	-	-	PI9	PI8

DATA REGISTER (READ)

90 SPM1 (1)

bit7	6	5	4	3	2	1	0
SPM (27 - 20)							

91 SPM1 (2)

bit7	6	5	4	3	2	1	0
SPM (19 - 12)							

92 SPM1 (3)

bit7	6	5	4	3	2	1	0
SPM (11 - 4)							

93 SPM1 (4)

bit7	6	5	4	3	2	1	0
SPM (3 - 0)				-	-	ERROR (Note)	

Note:

00	No Error Correction Occurred
01	1 Bit Error Correction Occurred
10	2 Bit Error Correction Occurred
11	Unable to Correct

94-97 SPM2 (1-4)

98-9B OHM1 (1-4)

9C-9F OHM2 (1-4)

A0-A3 OHM3 (1-4)

A4-A7 OHM4 (1-4)

A8-AB OHM5 (1-4)

AC-AF OHM6 (1-4)

B0-B3 OHM7 (1-4)

B4-B7 OHM8 (1-4)

B8-BB OHM9 (1-4)

BC-BF OHM10 (1-4)

C0-C3 OHM11 (1-4)

C4-C7 OHM12 (1-4)

C8-CB OHM13 (1-4)

CC-CF OHM14 (1-4)

D0-D3 CFM (1-4)

D4-D7 1st MSCM WORD (1-4)

D8-DB 2nd MSCM WORD (1-4)

DC-DF ON AND AFTER 3rd MSCM WORD (1-4)

E0-E3 RX DATA (1-4)

Circuit Description

■ Power Management

The AK2336A has six modes of operation, described in the Register Map "POWER DOWN MODE CONTROL" (address 00) for a meticulous power management. So its power consumption is only 1.4mA (TYP) at the "RX DATA Mode", when VDD is 3V. The AK2336A can handle FOCC data by itself and the conjunctive micro-controller could be in sleep mode during Idle mode. Therefore, the total stand by time could be extended as long as 1.5 times of the conventional solution.

■ Data Transmitter

Wideband RECC/RVC Data

The AK2336A provides the following treatments to the 38 bits incoming data (Message:36 bits + DCC:2 bits).

1) BCH Encode
2) Dotting Pattern
3) Synchronization Word
4) 7 bits Coded DCC (RECC only)
5) 48 bits code word
6) Message Construction
7) Manchester Encode

Narrow RVC Data

The AK2336A provides the following treatments to the 36 bits incoming data.

1) BCH Encode
2) NRZ Synchronization Word
3) 48 bits code word
4) Message Construction
5) Manchester Encode (Data Word only)

The AK2336A is transparent to the 36 bits data of Reverse Control Channel and Wideband /Narrow Reverse Voice Channel.

RECC Data Transmit Timing

Fig-7 shows Reverse Control Channel (RECC) data transmit timing.

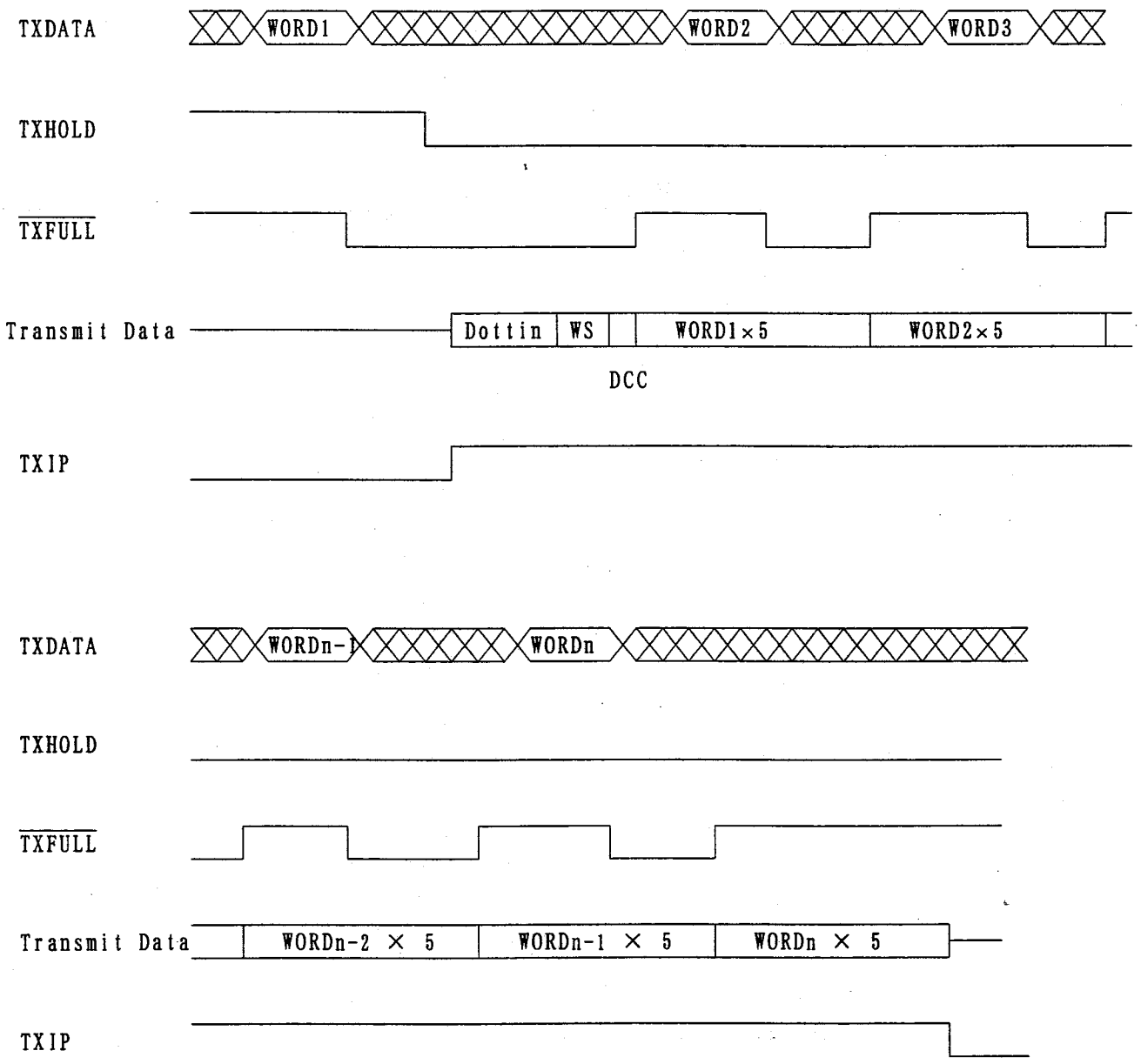
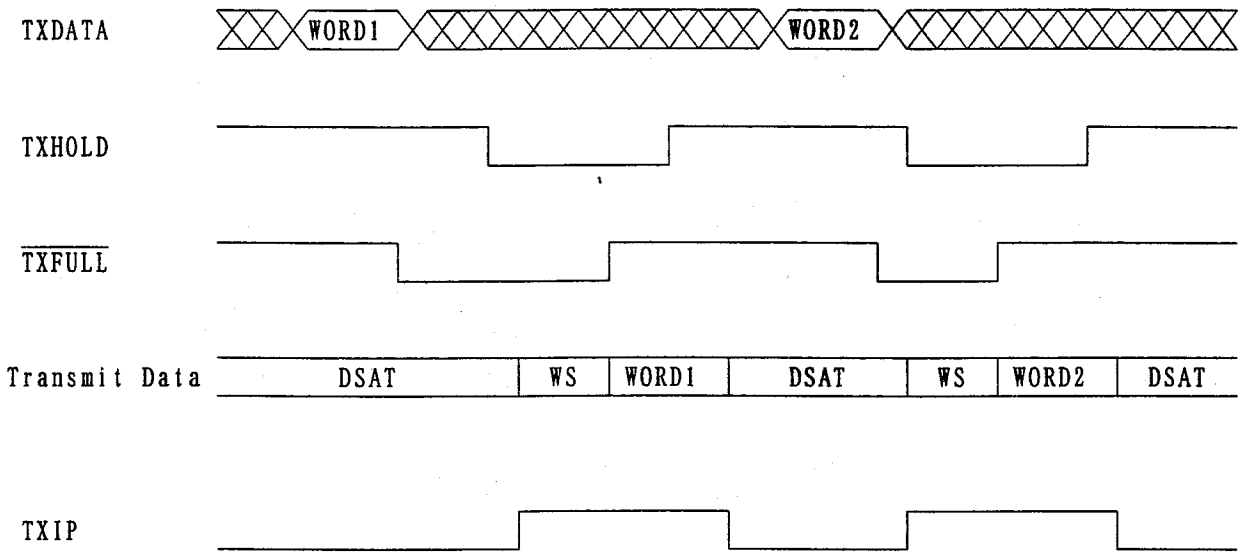


Fig-7 RECC Data Transmit Timing

Narrow RVC Data Transmit Timing

Fig-8 shows Narrow Reverse Voice Channel data transmit timing.



*DSAT phase is maintained so that when it is discontinued for transmission of data and sync words it is at the proper phase.

Fig-8 Narrow RVC Data Transmit Timing

DSAT/DST Generator

The AK2336A can generate seven valid DSAT/DST(24 bit) patterns. One of them, that was selected from the control register, is generated repeatedly, when Narrow Analog Mode is selected from the control register. When the polarity(DSAT↔DST) changes is desired from the control register(address 03) at Narrow Analog Mode, polarity will not be changed until next allowable phase, which is given as a Bit-Mask. For each mask bit that is set, a polarity inversion is allowed on that bit.
When DSAT/DST pattern changes is desired from the control register at Narrow Analog Mode, also the polarity that is the same address is set at the same time. And then the pattern and polarity will changed within 5ms.
NOTE: When the TXINV(address 01, bit1) change will be desired from the control register, the transmit data polarity is change immediately.

RECC Access Arbitration

TXCTRL pin goes "L" and INTERRUPT pin goes "H" simultaneously in order to stop transmission, if B/I bit alters to "Busy" from "Idle" by 56th bit or remains "Idle" until 104th bit after the transmission start.
The AK2336A adds unmodulated carrier(MODOUT pin output goes AGND level) automatically after transmitting the last data and TXIP goes "L" to inform no data transmission in progress.

■ Receiver

Wideband FOCC/FVC Data

The AK2336A performs the following treatments and outputs 28 bit data through the receive buffer.

1) Bit synchronization and word synchronization
2) Busy/Idle bit extraction
3) Majority Voting
4) Error Correction

The AK2336A is transparent to 28 bits data of FOCC and FVC.
When "DATA PROCESSOR ENABLE" (address 02) is set to "H", AK2336A Data Processor performs as described in the next chapter "Data Processor".

Narrow FVC Data

The AK2336A quantize the received data signal and outputs it without any processing.

DATA RECOVERY

The Data Recovery block performs clock recovery, manchester decoding and data regeneration. There are two mode of operation in clock recovery; high speed pull-in mode and low jitter mode. Once the word sync is detected, PLL goes to low jitter mode automatically.

DOTTING DETECTOR

The Dotting Detector block detect 32 bit continuous Dotting Pattern in FVC and generate interrupt. If "RX AUTO MUTE ENABLE" (addles 01) is set, receive voice circuits are muted after frame synchronization automatically. The external controller have to write address 67 (RXCTRL RESET) to be released from the mute and also the Dotting Detector block is reset.

WORD SYNC

The Word Sync block performs the frame synchronization and Busy/Idle bit extraction. The Word Sync block goes into In-frame mode after two consecutive Sync Word detection and goes into Out-of-frame mode after five consecutive miss-detection.

REVERSE CONTROL CHANNEL STATUS

The status of the reverse control channel is determined by register setting of "Busy/Idle MODE SELECT" (address 02)

"B/I MODE SELECT" = 1 : BUSY/IDLE detect by 1 bit data directly
"B/I MODE SELECT" = 0 : BUSY/IDLE detect by continuous 2 bit data

MAJORITY VOTING

Forward Control Channel;
The Majority Voting block performs bit-wise majority decision on five words of system A or B according to the Serving System (A/B) register after valid Word Sync detection.
Forward Voice Channel;
The Majority Voting block performs bit-wise majority decision on five consecutive word after the just before valid Word Sync detection.

ERROR CORRECTION

The Error Correction block corrects up to two bits error according to the control register by 12 parity bit in majority voted 40 bit data. If the more error (that is set correctional bit by register) occurs, it generates interrupt for uncorrection.

RECEIVE BUFFER

The Receive Buffer maintains corrected 28 bits data. RXRDY pin goes to "H" when the data is ready to read. RXRDY goes to "L" after reading the data or after majority voting of the next word being completed. The AK2336A over-writes the buffer when new data is received, even the previous data is not read yet.

■ Data Processor

The AK2336A Data Processor monitors Overhead Message and Control Message of Forward Control Channel (FOCC), and generates interrupt in proper manner. Therefore, the micro-controller may be in sleep mode until the AK2336A generates the interrupt. The AK2336A stores all the data needed during Idle Mode, and the micro-controller can read the data, which are received during sleeping, from the data register (address 90～DF) of the AK2336A after interrupt occurs.
This unique feature makes it possible to save the total power consumption during Idle Mode and could extend the standby time as long as 1.5 times of the conventional solution.

Rx Data Mode Operation

The AK2336A Data Processor has five modes of operation and each mode is independently set by "DP CONTROL" (address 30) except the folowing condition.

(1) Either OHM Train Mode or SPM mode is selectable. If both mode are selected, SPM mode is neglected because SPM mode is a subset of OHM Train mode.
(2) Both CFM mode and MSCM mode are selectable independently.
(3) If All mode is selected, the other mode is neglected.
(4) OHM Train mode, SPM mode and MSCM mode processing are not to be done, if CFM is received

NOTE: The Data Processor must be disabled (address 02, "RECEIVE DATA CONTROL") once, whenever the Data Processor mode is altered.

The interrupt condition is different in each mode as shown below.

(1) OHM Train Mode

Interrupt Conditions:
- Both SPM1 and SPM2 reception
  &
- OHM, whose END field = 1, reception
  &
- Different OHM(after 2nd OHM)

(2) SPM mode

Interrupt Condition:
- Both SPM1 and SPM2 reception
  &
- Different SPM(after 2nd SPM)

(3) MSCM Mode

Interrupt Conditions:

If MSCM mode is MIN1,
- MIN1r=MIN1p (One Word Page) reception
- MIN1r=MIN1p and MSCM (Except One Word Page) reception
- on and after MSCM3 reception

If MSCM mode is MIN1 & MIN2,
- MIN1r=MIN1p and MIN2r=MIN2p (Except One Word Page) reception
- on and after MSCM3 reception

If MSCM mode is OFF, (no MIN check)
- One Word Page reception
- MSCM1 and MSCM2 reception
- on and after MSCM3 reception

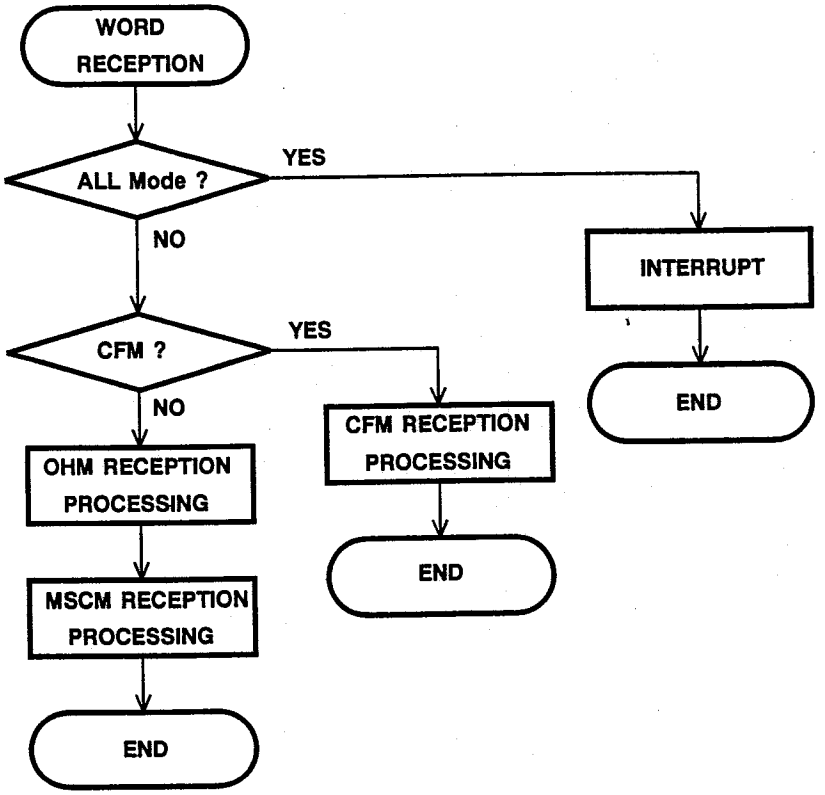
(4) CFM Mode

Interrupt Conditions:
- First CFM reception
- Different CFM detection

(5) ALL Mode

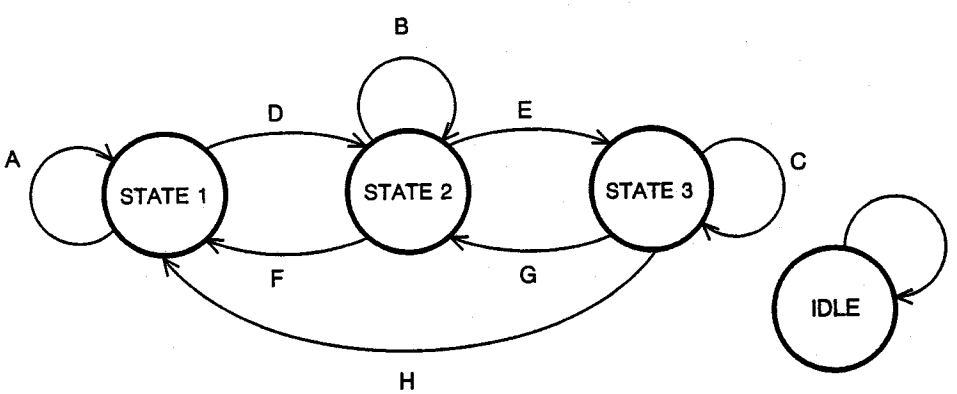
Interrupt Conditions:
- Every word reception

The flow chart of the data processing is described bellow;



The state diagram of each processing is described below.

(1) OHM RECEPTOIN PROCESSING



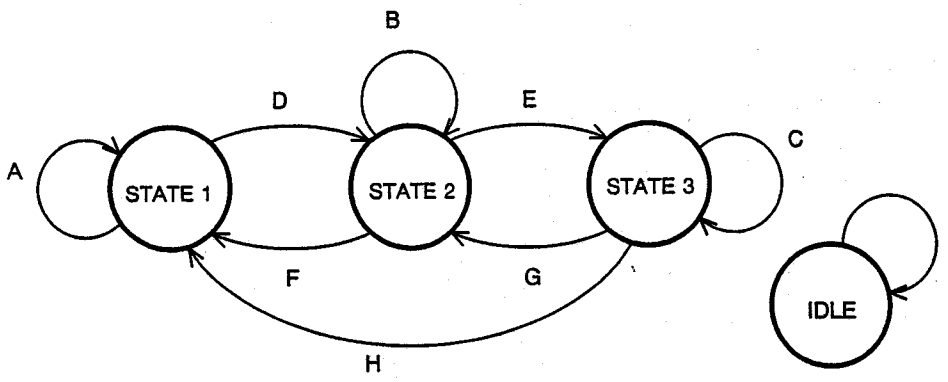
STATE 1: WAIT FOR SPM1
STATE 2: WAIT FOR SPM2
STATE 3: WAIT FOR END

```
//      IF (SPM = ON or OHM TRAIN = ON)
            CF ← ON                          /* CF: Compare Flag */
        NEXT STATE "STATE 1"

        IF (SPM = OFF and OHM TRAIN = OFF)
        NEXT STATE "IDLE"
```

```
"STATE 1"
        IF (MESSAGE = SPM1)
            IF (SPM1r ≠ SPM1s) {
                CF ← ON
                SPM1s ← SPM1r
            }
            NEXT STATE "STATE 2"                    /* STATE TRANSITION D */
        ELSE
            NEXT STATE "STATE 1"                    /* STATE TRANSITION A */

"STATE 2"
        IF (MESSAGE = SPM1)
            IF (SPM1r ≠ SPM1s) {
                CF ← ON
                SPM1s ← SPM1r
            }
            NEXT STATE "STATE 2"                    /* STATE TRANSITION B */

        IF (MESSAGE = SPM2)
            IF (SPM2r ≠ SPM2s) {
                CF ← ON
                SPM2s ← SPM2r
            }
            AW ← 1                                  /* AW: Additional Word */

        IF (OHM TRAIN = ON)
                IF (END FIELD = 1 and CF = ON) {
                    INTERRUPT ID ← OHM TRAIN
                    INTERRUPT
                    CF ← OFF
                    NEXT STATE "STATE 1"            /* STATE TRANSITION F */
                }
                ELSE
                    NEXT STATE "STATE 3"            /* STATE TRANSITION E */
            ELSE {
                    IF (CF = ON) {
                        INTERRUPT ID ← SPM
                        INTERRUPT
                        CF ← OFF
                    }
                NEXT STATE "STATE 1"                /* STATE TRANSITION F */
                    }
        ELSE
            NEXT STATE "STATE 1"                    /* STATE TRANSITION F */

"STATE 3"
        IF (MESSAGE = SPM1)
            IF (SPMr ≠ SPMs) {
                CF ← ON
                SPMs ← SPMr
```

```
        NEXT STATE "STATE 2"                    /* STATE TRANSITION G */

    IF (MESSAGE = SPM2)
        NEXT STATE "STATE 1"                    /* STATE TRANSITION H */

    IF (MESSAGE = MSCM)
        NEXT STATE "STATE 3"                    /* STATE TRANSITION C */

    IF (BCH ERROR)
        AW ← AW + 1
            IF (AW = 15)
                NEXT STATE "STATE 1"            /* STATE TRANSITION H */
            ELSE {
                CF ← ON
                OHMs(AW) ← OHMr
            }
                NEXT STATE "STATE 3"            /* STATE TRANSITION C */

    IF (MESSAGE = OHM and ≠ SPM1, SPM2, CFM)
            AW ← AW + 1
            IF (OHMr ≠ OHMs(AW)) {
                CF ← ON
                OHMs(AW) ← OHMr
            }
            IF (END FIELD =1 and CF = ON) {
                INTERRUPT ID ← OHM TRAIN

                INTERRUPT
                CF ← OFF
                NEXT STATE "STATE 1"            /* STATE TRANSITION H */
            }
            ELSE
                    IF (AW = 15)
                        NEXT STATE "STATE 1"    /* STATE TRANSITION H */
                    ELSE
                        NEXT STATE "STATE 3"    /* STATE TRANSITION C */
```

(2) MSCM RECEPTION PROCESSING



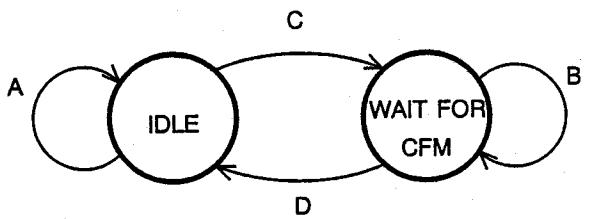
STATE 1: WAIT FOR MSCM1
STATE 2: WAIT FOR MSCM2
STATE 3: WAIT FOR ON AND AFTER MSCM3

```
IF (MSCM = ON)
    NEXT STATE "STATE 1"

IF (MSCM = OFF)
    NEXT STATE "IDLE"


"STATE 1"
        IF (MESSAGE = MSCM1)
                IF (((MIN CHECK = MIN1 or MIN1&2) and MIN1r = MIN1p)
                or MIN CHECK = OFF)
                    MSCM1s ← MSCM1r
                    NEXT STATE "STATE 2"              /* STATE TRANSITION D */
                ELSE
                    NEXT STATE "STATE 1"              /* STATE TRANSITION A */

        IF (MESSAGE = 1 WORD PAGE)
                IF ((MIN CHECK = MIN1 and MIN1r = MIN1p) or MIN CHECK = OFF) {
                    MSCM1s ← MSCM1r
                    INTERRUPT ID ← MSCM
                    MSCM ID ← 1 WORD

                    INTERRUPT
                    NEXT STATE "STATE 1"              /* STATE TRANSITION A */
                }

        IF (MESSAGE = ON AND AFTER MSCM2)
            NEXT STATE "STATE 1"                      /* STATE TRANSITION A */

"STATE 2"
        IF (MESSAGE = MSCM1)
```

```
                    or MIN CHECK = OFF)
                        MSCM1s ← MSCM1r
                        NEXT STATE "STATE 2"              /* STATE TRANSITION B */
                    ELSE
                        NEXT STATE "STATE 1"              /* STATE TRANSITION F */

                IF (MESSEGE = 1 WORD PAGE)
                    IF ((MIN CHECK = MIN1 and MIN1r = MIN1p)
                    or MIN CHECK = OFF) {
                        MSCM1s ← MSCM1r
                        INTERRUPT ID ← MSCM
                        MSCM ID ← 1 WORD
                        INTERRUPT
                        NEXT STATE "STATE 1"              /* STATE TRANSITION F */
                    }

                IF (MESSAGE = ON AND AFTER MSCM2)
                    IF (((MIN CHECK = MIN1 or MIN1&2) and MIN2r = MIN2p)
                    or MIN CHECK = OFF) {
                        MSCM2s ← MSCM2r
                        INTERRUPT ID ← MSCM
                        MSCM ID ← 2 WORD
                        INTERRUPT
                        NEXT STATE "STATE 3"              /* STATE TRANSITION E */
                    }
                    ELSE
                        NEXT STATE "STATE 1"              /* STATE TRANSITION F */

                ELSE
                    NEXT STATE "STATE 1"                  /* STATE TRANSITION F */

            "STATE 3"
                IF (MESSAGE = MSCM1)
                    IF (((MIN CHECK = MIN1 or MIN1&2) and MIN1r = MIN1p)
                    or MIN CHECK = OFF)
                        MSCM1s ← MSCM1r
                        NEXT STATE "STATE 2"              /* STATE TRANSITION G */
                    ELSE
                        NEXT STATE "STATE 1"              /* STATE TRANSITION H */

                IF (MESSEGE = 1 WORD PAGE)
                    IF ((MIN CHECK = MIN1 and MIN1r = MIN1p)
                    or MIN CHECK = OFF) {
                        MSCM1s ← MSCM1r
                        INTERRUPT ID ← MSCM
                        MSCM ID ← 1 WORD
                        INTERRUPT
                        NEXT STATE "STATE 1"              /* STATE TRANSITION H */
                    }

                IF (MESSAGE = ON AND AFTER MSCM2)
```

```
                INTERRUPT ID ← MSCM
                MACM ID ← ON AND AFTER WORD 3
                INTERRUPT
                NEXT STATE "STATE 3"                    /* STATE TRANSITION C */

            ELSE
                NEXT STATE "STATE 1"                    /* STATE TRANSITION H */
```

(3) CFM RECEPTION PROCESSING

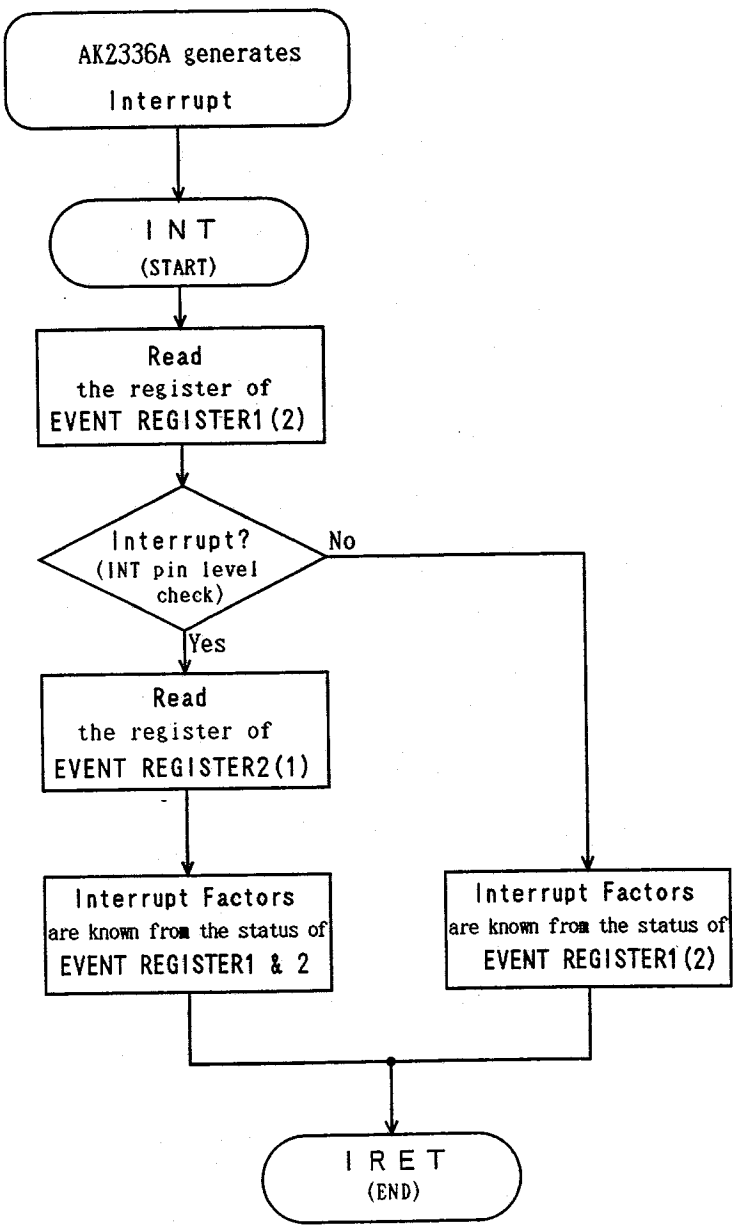



```
    "IDLE"
            IF (MESSAGE = CFM)
                NEXT STATE "IDLE"                       /* STATE TRANSITION A */

            IF (CFM = ON)
                CF ← ON
                NEXT STATE "WAIT FOR CFM"               /* STATE TRANSITION C */

    "WAIT FOR CFM"
            IF (MESSAGE = CFM)
                    IF (CFMr ≠ CFMs) {
                        CF ← ON
                        CFMs ← CFMr
                    }
                    IF (CF = ON) {
                        INTERRUPT ID ← CFM
                        INTERRUPT
                        CF ← OFF
                    }
                NEXT STATE "WAIT FOR CFM"               /* STATE TRANSITION B */

            IF (CFM = OFF)
                NEXT STATE "IDLE"                       /* STATE TRANSITION D */
```

■ μC interface sequence at interrupt

Following is the recommended sequence sample to know the interrupt factors through the EVENT REGISTER1&2 when interrupt is occurred.

The INT pin goes to high when interrupt is occurred, then that pin goes to low when the all interrupt factors are read through the EVENT REGISTER(1/2).
However, the output level(polarity) of INT pin when interrupt is occurred depends on the register(Add.01/bit6) data. The INT pin status at above case is shown at being set Add.01/bit6 to "0".
Each of EVENT REGISTER(1/2) must be started reading only when interrupt is occurred.
Each of EVENT REGISTER(1/2) must not be started reading when interrupt is not occurred.



■ SAT Signal Reception and Transponding

The AK2336A has a on-chip SAT signal receiver and transponder. The receive SAT signal frequency is determined to specify one SAT frequency out of three by the control register.

The AK2336A does not support the SAT phase angle adjustment.

■ Serial Interface

Control Register, Status Register and Data Register of AK2336A are read through serial interface. The serial interface timing is shown in figure Fig-8.

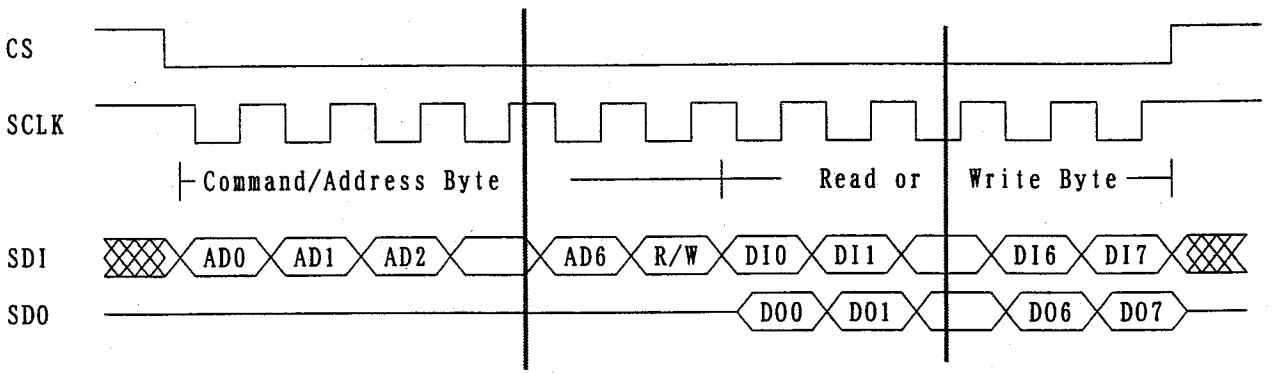


Fig-8 Serial Interface Timing 1

If SCLK is clocked continuously, AK2336A increments the address automatically and input/output next address data as shown in figure Fig-9.

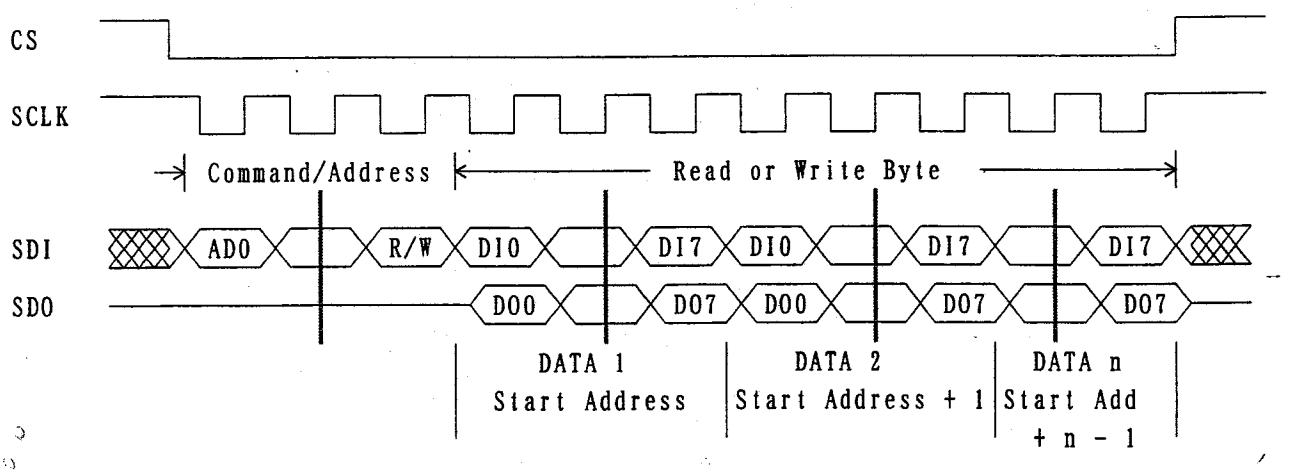


Fig-9 Serial Interface Timing 2

* Parallel Interface also has the same feature.

■ Uncommitted DAC／OP-AMP／Timer

DAC

The AK2336A has three on-chip 8 bits linear DACs.

Resolution : 8bit linear
Output Voltage : 0.02×VDD(00)～0.98×VDD(FF)
DNL : ≦ ±1/2 LSB (No Load)
Settling Time : ≦ 10μs
Output Current : I_{OUT}=50μA(MAX)

OP-AMP

The AK2336A has an uncommitted OP-AMP (AMP7).

Timer

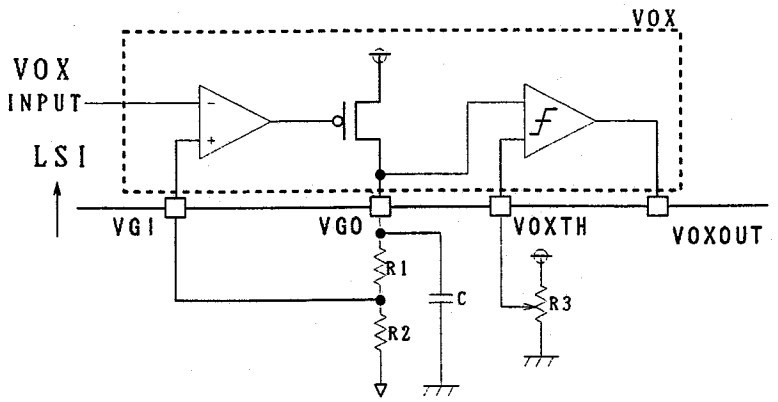
The AK2336A has two uncommitted 8 bits Timers. The main clock and preset value of the timer are set from the control register. Also, the timers have a repeat mode. For example: The initial timer value is set to 50. At the point that the timer reaches 0, it generates an interrupt and TEXP1/2 pin goes to "Hi". At a same time, it resets to 50 and starts to count down automatically. TEXP1/2 pin goes to "Lo" after one main clock cycle.
Note, the interrupt line has to stay in the interrupt state until the event register with the timer are read.

T1: Clock ..... 12.5kHz, 6.25kHz, 3.125kHz or 1.5625kHz
Counter Value ..... 0～255

T2: Clock ..... 781.25Hz, 390.625Hz, 195.3125Hz or 97.65625Hz
Counter Value ..... 0～255

■ VOX

The VOX circuit of the AK2336A is shown bellow. The sensitivity, attack time and recovery time of the circuit are defined by external resistors and a capacitor.



Operation; The signal at VGO is described as belows;

$$(1/2\ VDD) + \{(R1+R2)/R2\} * V_{O-P}$$

V_{O-P} described above is the voltage of VOX INPUT's V_{O-P}.
And VOXOUT is determined by comparing VGO with VOXTH that is set by R3.
ATTACK/DECAY TIME are under the control of external capacitor C.

■Automatic Frequency Control (AFC)

AK2336A provides a controlling voltage for VCXO. The μC determines the control voltage from counts of the 1.2MHz and the 2nd IF (typ 450kHz) clocks. The μC writes the control voltage of the D/A converter to the register. AK2336A D/A converts the register value and output it. AK2336A provides the following for AFC. Figure in the next page shows the block diagram of the AFC.

1. AFC block diagram description

- AFC Input Buffer for the 2nd IF(450kHz)
- 4bit Shift Register(450kHz)
- 2bit Shift Register(1.2MHz)
- AFC (16bit) counter clocked by 450kHz
- 1 sec counter clocked by 1.2MHz
- 8 bit D/A converter

2. Operational sequence

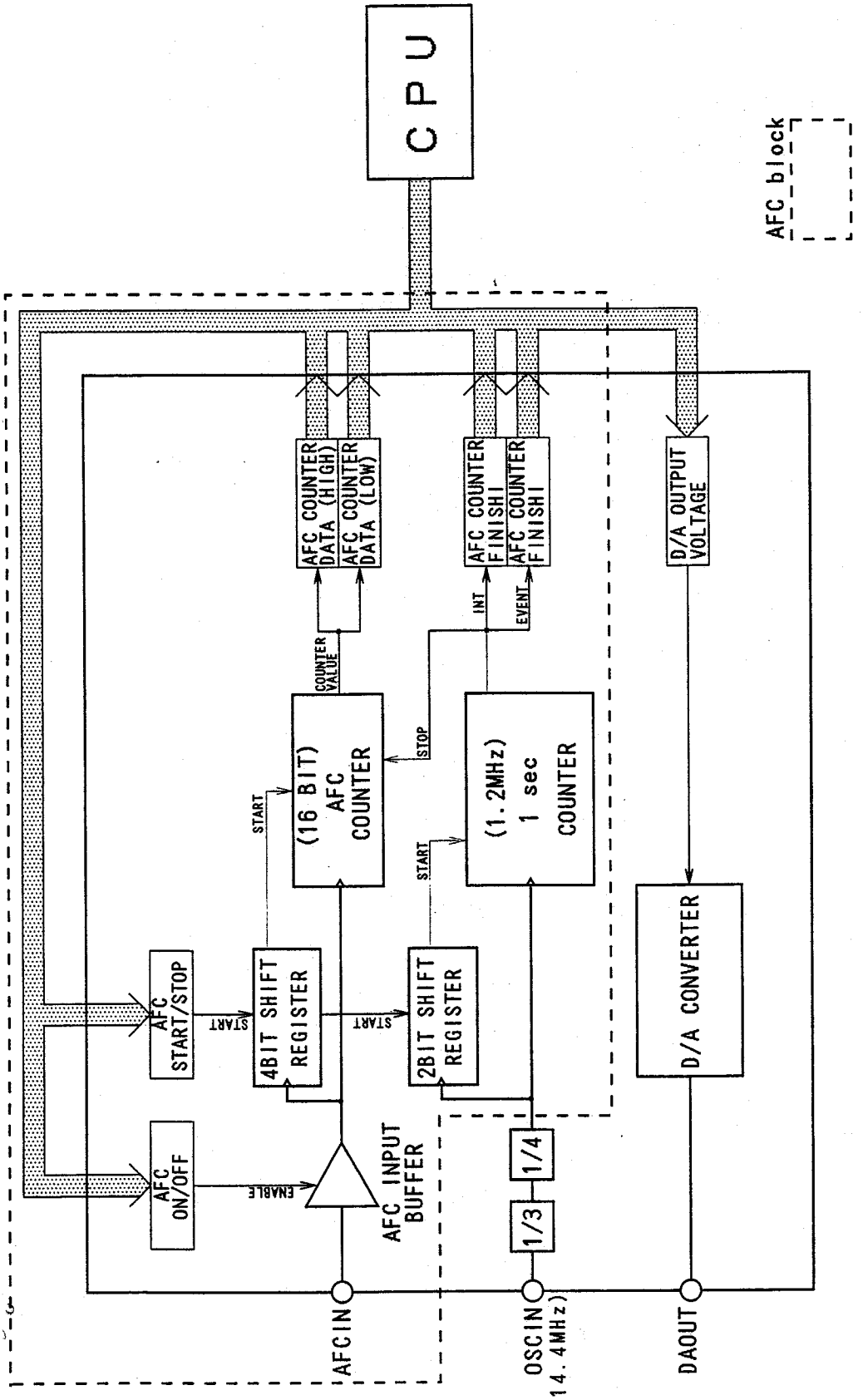
Pre - SET

1 Power ON.
2 System Reset.
3 Enable D/A and AMP7.
4 Set the D/A output to the center level.
5 Enable AFC INPUT BUFFER(by setting the AFC ON/OFF bit = "1").
AFC INPUT BUFFER must be enabled at least 5ms prior to the AFC start.

AFC START

①Start AFC (by setting the AFC START/STOP bit = "1").
②After four (4) 450kHz clocks, AFC COUNTER and 2 BIT SHIFT REGISTER starts.
③And then after two (2) 1.2MHz clocks, 1 sec COUNTER starts.
④After 1 sec, AFC COUNTER stops and generates a interrupt to μC.
⑤μC reads the EVENT REGISTER and then reads AFC COUNTER DATA register.
⑥AK2336A stops AFC automatically (by setting AFC START/STOP bit = "0") and resets the counter value.
⑦In consideration of the counter value, μC writes the control voltage of the D/A converter to the register. Go to ①.
⑧Disable AFC (by setting the AFC ON/OFF bit = "0").

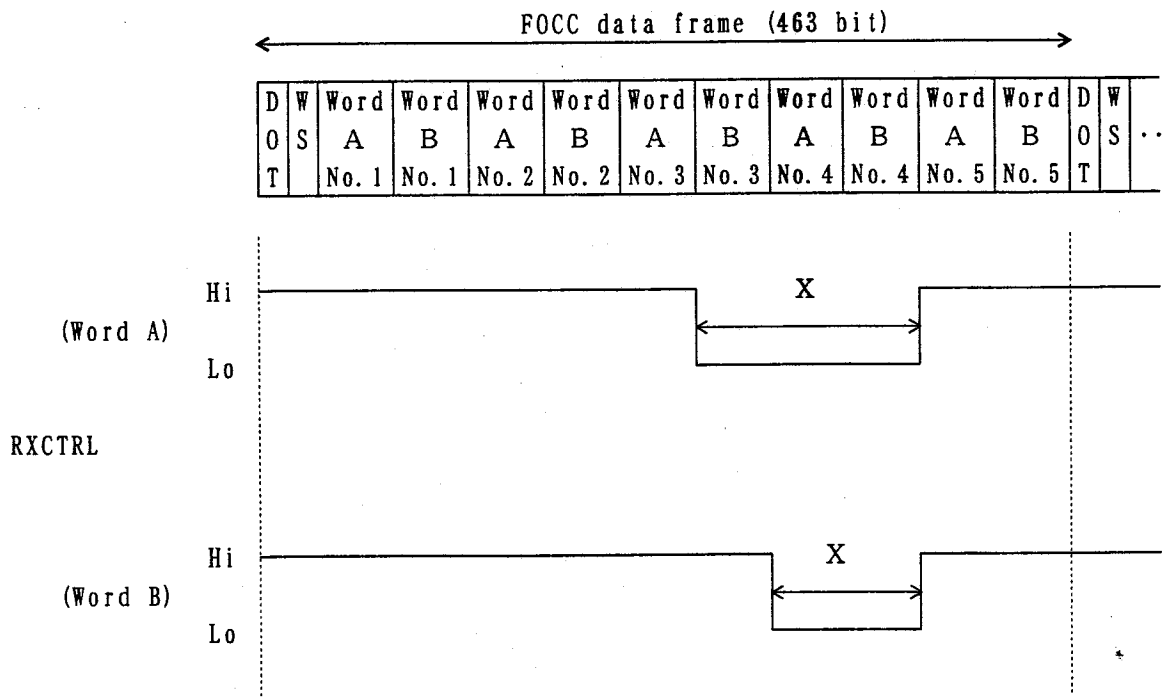
*AFC is not restarted (by setting the AFC START/STOP bit = "1") without reading the last AFC COUNTER DATA(Add.88&89) register data.
If that case is required, please set the AFC START/STOP bit = "0" or read the last AFC COUNTER DATA(Add.88&89) register data before restarting.


CPU
AFC block
AFC COUNTER DATA (HIGH)
AFC COUNTER DATA (LOW)
AFC COUNTER FINISHI
AFC COUNTER FINISHI
D/A OUTPUT VOLTAGE
INT
EVENT
COUNTER VALUE
STOP
START
(16 BIT) AFC COUNTER
(1.2MHz) 1 sec COUNTER
AFC START/STOP
4BIT SHIFT REGISTER
2BIT SHIFT REGISTER
D/A CONVERTER
AFC ON/OFF
ENABLE
AFC INPUT BUFFER
1/4
1/3
AFCIN
OSCIN (14.4MHz)
DAOUT

■DISCONTINUOUS RECEPTION (DRX)

Regarding to the FOCC, AK2336A performs bit-wise majority decision on repeated five words normally. However, when DISCONTINUOUS RECEPTION(DRX) is set from the control register(address 01), if the first three* received data of the five words are matched, receive data is settled without receiving the rest data. At the same time AK2336A generates a interrupt and RXCTRL pin goes to "Lo". Therefore, RF block in the system could be power down. And then RXCTRL pin go to "Hi" after the time(X) that is set from the control register(address 26) and AK2336A generates a interrupt. If the first three data word are not matched, AK2336A performs bit-wise majority decision normally. RXCTRL pin status is also controlled from the command register(address 66/67) by force.

*The first three or two; that is set from the control register.

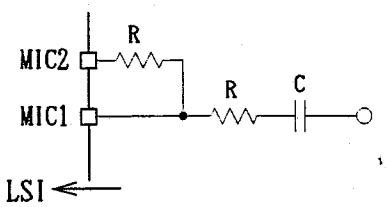


Note:When DRX is set during FOCC reception, DRX takes effect from the next frame data.
At Narrow analog mode, RXCTRL pin is fixed with "Hi" level.

Application Circuit Example

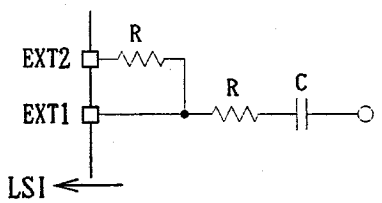
External circuit examples

1.AMP1



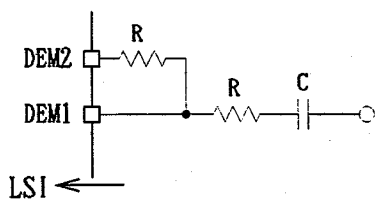
R: 100KΩ
C: 0.1μF

2.AMP2



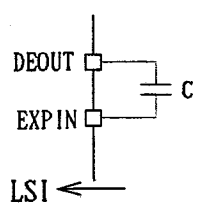
R: 100KΩ
C: 0.1μF

3.AMP3/8



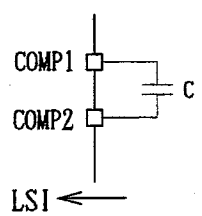
R: 100KΩ
C: 0.1μF (AMP3)
0.33μF (AMP8)

4.AC Coupling Capacitor



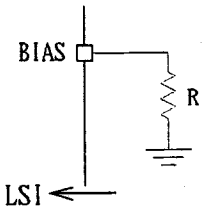
C: 0.047μF ±50%

5.Capacitor For Compressor



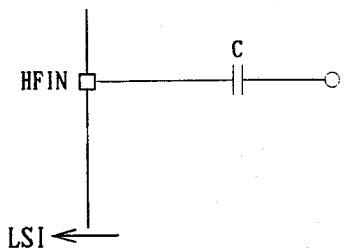
C: 0.047μF ±50%

6. Bias-current Setting Resistor



R: 61KΩ (VDD=3V±10%) ±5%
R: 100KΩ (VDD=5V±10%) ±5%

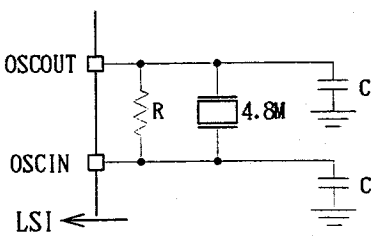
7. HFIN Input



C: 0.1μF ±20%

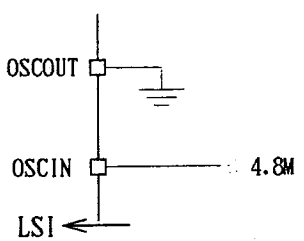
8. Main Clock Input

(1) Crystal Oscillator

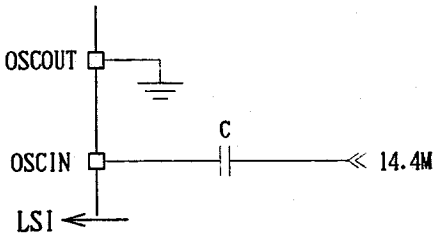


C: 22pF ±20%
R: 1MΩ

(2) 4.8M Input

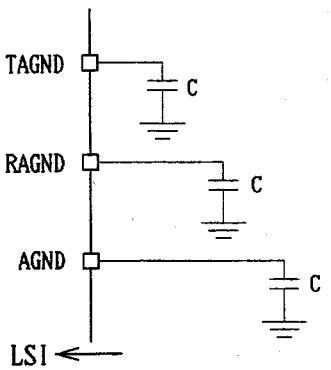


(3)14.4M Input



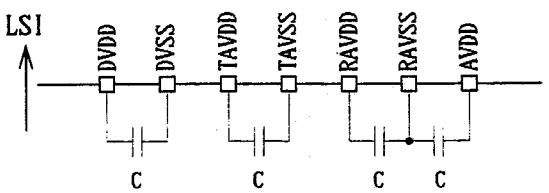
C: 100pF ±20%

9.AGND Stabilization Capacitor



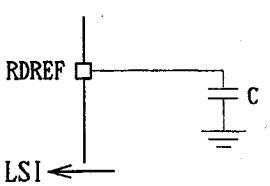
C: 1μF (≧0.8μF)

10.Power Supply Stabilization Capacitor



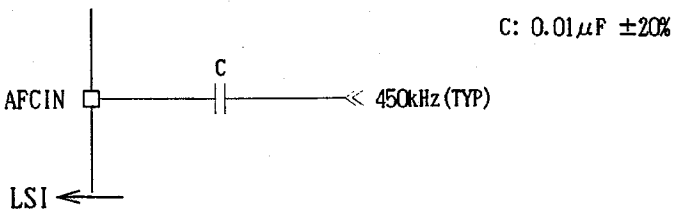
C: 0.1μF

11.CMP3 Capacitor For Offset Cancellation



C: 1μF ±20%

1 2.AFC 2nd IF signal input



Supplement

■Analog Characteristics that Depend on the Power Supply Voltage

Analog characteristics in the AK2336A data sheet are specified at VDD=3V.
Analog characteristics described below are in proportion to the supply voltage.

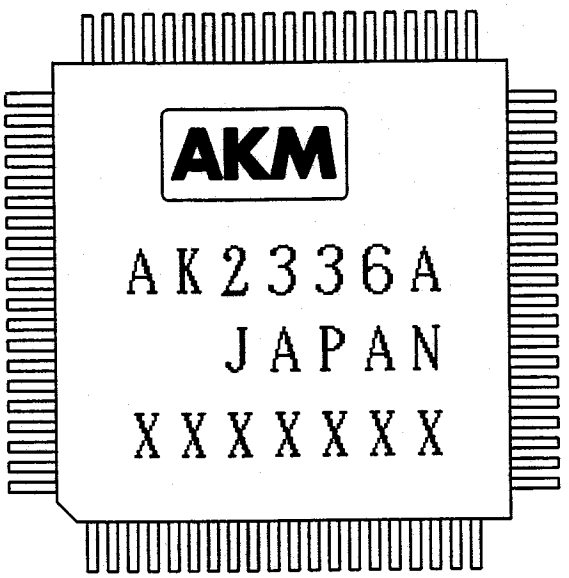
Difference from VDD=3.0V : 20log(VDD/3) [dB]

Item	VDD=3.0V	VDD=4.0V	VDD=5.0V
Compandor Unity Gain Level (TYP)	-12.0dBV	-9.5dBV	-7.56dBV
Limiter Level (TYP)	-8.2dBV	-5.7dBV	-3.76dBV
SAT Output Level (TYP)	-25.2dBV	-22.7dBV	-20.76dBV
Data (AMPS/TACS) Output Level (TYP)	-13.2dBV	-10.7dBV	-8.76dBV
Data (NAMPS) Output Level (TYP)	-34.3dBV	-31.8dBV	-29.9dBV
Data (NTACS) Output Level (TYP)	-32.3dBV	-29.8dBV	-27.9dBV
DTMF Output Level (TYP)	-13.2dBV	-10.7dBV	- 8.76dBV
SAT Detect Level (MIN)	-35.2dBV	-32.7dBV	-30.76dBV
DAC Output Level (TYP)	0.06V～2.94V	0.08V～3.92V	0.10V～4.90V

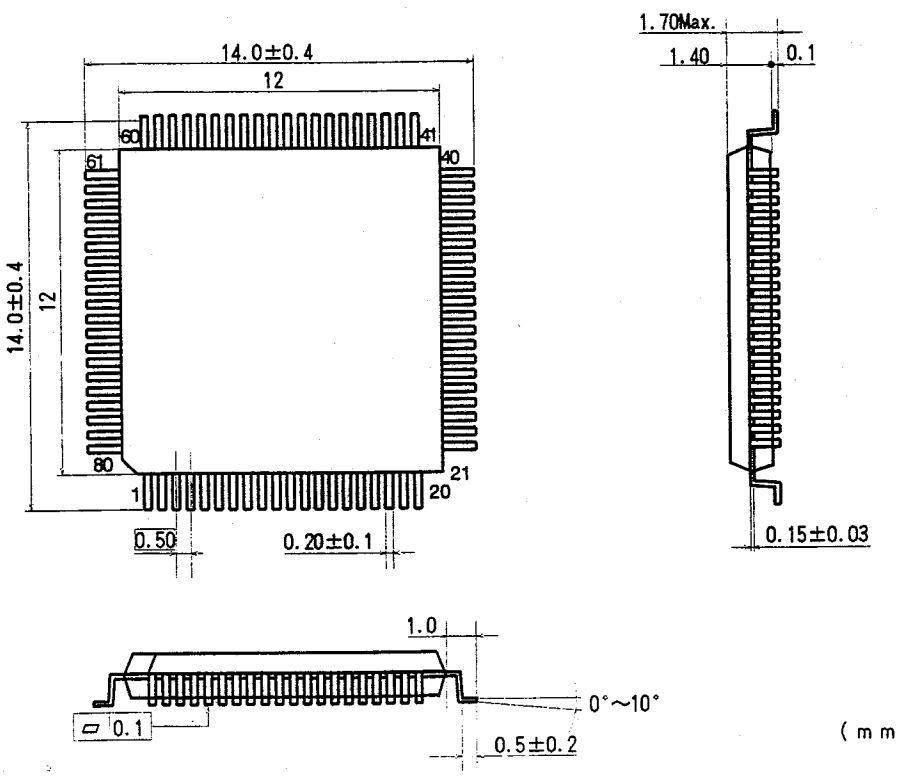
Package

■ Marking

(1) Pin #1 indication
(2) Date Code : XXXXXX (7 Digits)
(3) Marketing Number : AK2336A
(4) Country of Origin : JAPAN
(5) Asahi Kasei Logo



■ Package Outline



(mm)

AKD2336

AK2336/AK2336A Evaluation Board

General Description

AKD2336 is the AMPS/NAMPS/TACS/NTACS base band processor, AK2336/AK2336A, evaluation board.
The power supply for the board is either 3V±10% or 5V±10%. As there are 4.8MHz crystal on the board, it is not necessary to input the main clock.
There are external circuits of input/output amplifiers and BNC connectors for analog interface on the board.
There are external circuits of receiver amplifiers (RECAMP). RECP/RECN output is the differential output of REC1 signal. Therefore, the signal quality can be evaluated only with connecting the ceramic receiver to RECP/RECN.
DTMF output is inputted to transmitter and receiver on the board and these levels are adjustable by external trimmer.
Universal area for your own circuits is available.

Features

- ☐ AMPS/NAMPS/TACS/NTACS base band processor, AK2336/AK2336A, evaluation board
- ☐ Analog interface: BNC connector
- ☐ Digital interface: 20 pin connector and 10 pin connector
- ☐ Power supply: 3V±10% or 5V±10%
- ☐ On board 4.8MHz crystal for main clock or 14.4MHz TCXO clock input
- ☐ Trimmer for TX/RX DTMF tone level adjustment
- ☐ Trimmer for VOX detect level adjustment
- ☐ Serial/Parallel CPU interface
- ☐ Programmable I/O available (At serial interface mode)
- ☐ Universal area for your own circuits

□ CPU Interface

CPU interface has two mode of operation. One is parallel mode and another is serial mode. At serial mode, P/$\overline{S}$ pin should be set "L" by DIP switch described in the next chapter and four signals (SDI, SDO, $\overline{CS}$, SCLK) are controlled through the 20 pin connector.
At parallel mode, P/$\overline{S}$ pin should be set "H" by DIP switch described in the next chapter. Three signals (R/$\overline{W}$, $\overline{DS}$, ALE) are controlled through the 20 pin connector and AD0/P0 ~ AD7/P7 are controlled through the 10 pin connector. When AD0/P0 ~ AD7/P7 are controlled through the 10 pin connector, SW1/00 ~ SW1/07 should be set at the center point.
The pin assignment of the 20 pin connector and 10 pin connector are described in 「**Input/Output Pin on The Board and Their Name**」.

□ Clock Input

There are three mode of clock input.

(1) 4.8MHz oscillator mode; There is a 4.8MHz crystal on the board.
It is necessary to set switches described in the next chapter.

(2) 4.8MHz clock input mode; Input 4.8MHz clock at MCLKIN(BNC) pin, and set switches described in the next chapter.

(3) 14.4MHz clock input mode; Input 14.4MHz TCXO output at MCLKIN(BNC) pin, and set switches described in the next chapter.

□ Input/Output Pin on The Board and Their Name

Input/Output pins for evaluation are on the board as BNC connectors, the 20 pin connector, 10 pin connector or test pins. Their names are the same as AK2336/AK2336A pin assignment except 4 pins described below;

MICIN(BNC)	Transmitter mic amplifier(AMP1)'s input
EXTIN(BNC)	Transmitter external input amplifier(AMP2)'s input
DEMIN1(BNC)	Receiver amplifier(AMP3)'s input
DEMIN2(BNC)	Receiver amplifier(AMP8)'s input
EXPTESTIN(BNC)	Expander's input at evaluation mode

Digital output pins are connected to test pins, the 20 pin connector or 10 pin connector.
The pin assignment of the 20 pin connector and 10 pin connector are as follows;

10 PIN CONNECTOR:

PIN No.	PIN NAME
No. 1	GND
No. 2	NC
No. 3	AD1/P1
No. 4	AD0/P0
No. 5	AD3/P3
No. 6	AD2/P2
No. 7	AD5/P5
No. 8	AD4/P4
No. 9	AD7/P7
No. 10	AD6/P6

20 PIN CONNECTOR:

PIN No.	PIN NAME	FUNCTION (Parallel Mode / Serial Mode)
No. 1	GND	GND (0V)
No. 2	NC	
No. 3	TXCTRL	RF Transmitter control
No. 4	SATOUT	Receive SAT signal output
No. 5	SATDET	Receive SAT detect output
No. 6	VOXOUT	VOX output
No. 7	RXDATA	Receive Wide/Narrow data output
No. 8	RXRDY	Receive data ready
No. 9	P8	I/O port
No. 10	P9	I/O port
No. 11	INT	Interrupt output
No. 12	RXCTRL	RF Receiver control
No. 13	TEXP1	Timer 1 expire output
No. 14	TEXP2	Timer 2 expire output
No. 15	ALE/SDI	Address Latch Enable / Serial Data Enable
No. 16	SDO	– / Serial Data Output
No. 17	R/$\overline{W}$/SCLK	Read/Write Select / Serial Data Clock
No. 18	$\overline{DS}$/ $\overline{CS}$	Data Strobe Enable / Chip Select Enable
No. 19	NC	
No. 20	CLKOUT	4.8MHz clock output

□ Programmable I/O Port

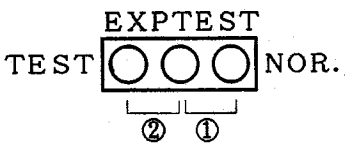
SW1/00 ~ SW1/07 are switches for setting AD0/P0~AD7/P7 pins at input mode. AD0/P0~AD7/P7 are set either by SW1/00 ~ SW1/07 or through the 10 pin connector. When setting through the 10 pin connector, SW1/00 ~ SW1/07 should be set at the center point. These switches should be set at the center point normally, and AD0/P0~AD7/P7 pins are available as programmable I/O ports.

□ RX・TXDTMF Level Adjustment

DTMF tone at DTMFOUT pin is inputted to RTONE and TONEIN by setting J.P. described in the next chapter. RXDTMF level is adjusted by RXDTMF trimmer and TXDTMF level is by TXDTMF trimmer at this time.

J. P. & Switch Description

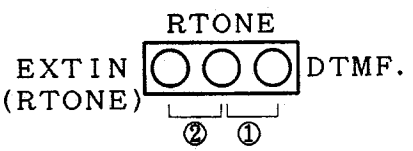
1. EXPANDOR INPUT SELECT J.P. (for evaluating the EXPANDOR)



①------- NORMAL MODE (Input is DEOUT)

②------- EVALUATION MODE (Input is EXPTESTIN)

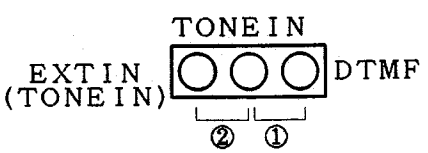
2. RTONE INPUT SELECT J.P.



①------- DTMF from DTMFOUT (Level is adjusted by RXDTMF trimmer)

②------- Input is RTONE

3. TONEIN INPUT SELECT J.P.



①------- DTMF from DTMFOUT (Level is adjusted by TXDTMF trimmer)

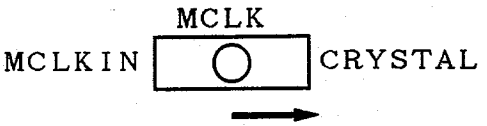
②------- Input is TONEIN

4. RESET SW. (PUSH BUTTON)

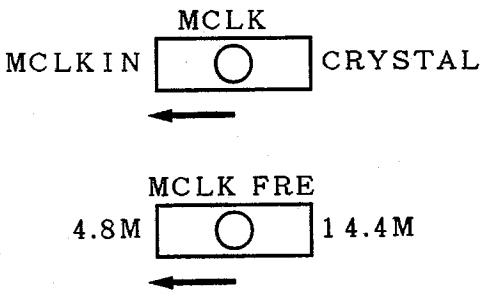
PUSH ------- All register data reset

7. MAIN CLOCK

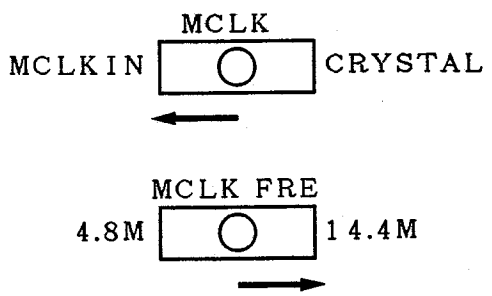
(1) CRYSTAL OSCILLATOR MODE



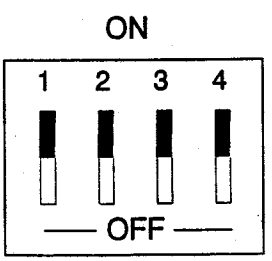
(2) 4.8M INPUT MODE



(3) 14.4M INPUT MODE

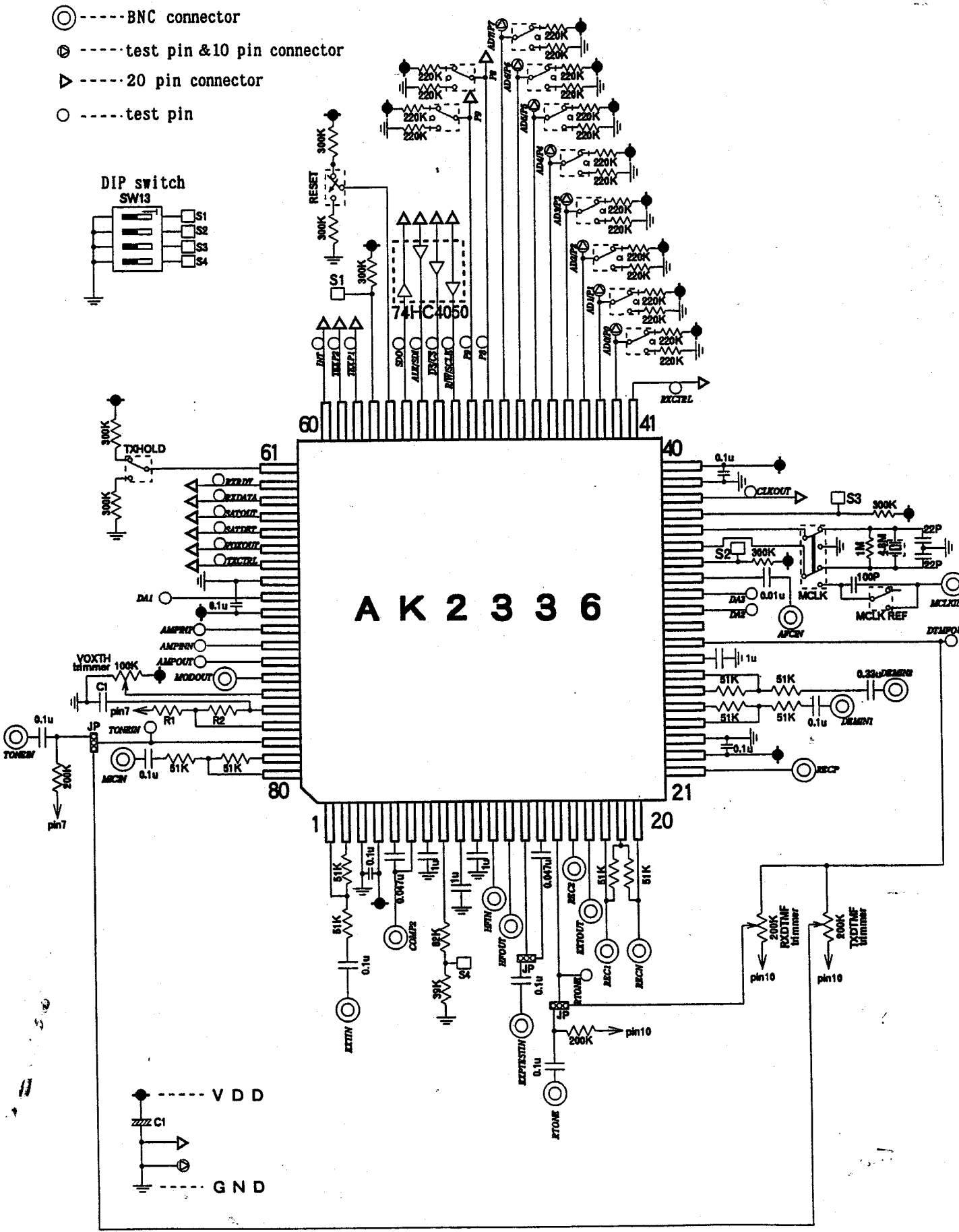


8. DIP SWITCH MODE SET



		ON	OFF
1	CPU interface mode	Serial	Parallel
2	MCLK select	14.4MHz	4.8MHz
3	4.8MHz clk output	Enable	Disable
4	Supply voltage	3V±10%	5V±10%

Board Schematic



Board Layout