FEATURES

- Serial data: up to 1.25 Gb/s
- ECL 100K/10KH compatible parallel data inputs/outputs
- Standard ECL power supplies: V_{EE} = -5.2 V ± 0.26 V, V_{TT} = -2.0 V ± 0.1 V
- VS8010: 8 bit Mux/Demux and SONET frame detection and recovery
- VS8011: 8 bit Mux
- VS8012: 8 bit Demux and SONET frame detection and recovery
- Compatible with STS-3 to STS-24 SONET applications

FUNCTIONAL DESCRIPTION

Introduction

The VS8010, VS8011 and VS8012 are high speed SONET compatible 8-bit data conversion devices capable of serial data rates up to 1.25 Gb/s. The VS8010 series can be used for STS-3 through STS-24 SONET applications.

The VS8010 Series are fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high speed and low power dissipation. These products are packaged in a ceramic 52 pin leaded or leadless chip carrier. Refer to Section 6, "Packaging" for a complete description of this package.

VS8010

The VS8010 integrates an 8:1 multiplexer, 1:8 demultiplexer, and SONET frame detection and recovery circuitry all on one chip.

8:1 Multiplexer Circuit

The 8:1 multiplexer accepts 8 parallel ECL data inputs ***[D(1:8)]*** at rates up to 155 Mb/s and multiplexes them into a single bit stream at speeds up to 1.25 Gb/s. The parallel data inputs are clocked into the input registers with ***BYCLK***, an ECL input operating at up to 155 MHz. The high speed clock input ***(CLKI)*** is divided by 8 ***(CLK8)*** and used to synchronize the parallel data to the timing generator. ***CLK8*** then loads the parallel data into the buffer registers. An on-chip circuit detects internal set up and hold violations caused by improperly related ***BYCLK*** and ***CLK8*** falling edges. An external signal ***(SYNC)*** may be used to correct ***CLK8*** phase by 180°. ***SYNC*** is high. If a setup or hold violation has been detected, a ***SYNC*** input causes ***CLK8*** to be inverted on the next ***BYCLK*** falling edge, thereby guaranteeing a safe ***CLK8*** and ***BYCLK*** relationship. If no setup and hold violation has been detected ***SYNC*** has no impact on the circuit.

The high speed differential clock input is brought on-chip at ***CLKI, CLKIN***. The high speed differential serial data is provided at the ***DO, DON*** outputs. The high speed differential clock signal is transmitted off chip via the high speed outputs ***CO, CON***.

1:8 Demultiplexer Circuit

The 1:8 demultiplexer converts serial data at up to 1.25 Gb/s into an 8-bit parallel data stream at up to 155 Mb/s. The high speed differential serial input is at ***DI, DIN***. Valid parallel data is clocked out by the divide by 8 clock output ***BYCKO***. The demultiplexer also contains SONET frame detection and recovery circuitry.

Frame Recovery Circuit

The frame recovery circuits are enabled by a falling edge on the ***OOFN*** input. Once enabled, the frame recovery circuits start looking for the SONET framing sequence. Once the frame is detected, a confirmation signal is sent off-chip through the low power ECL output ***FP***. The frame detection confirmation signal also disables the frame recovery circuits.

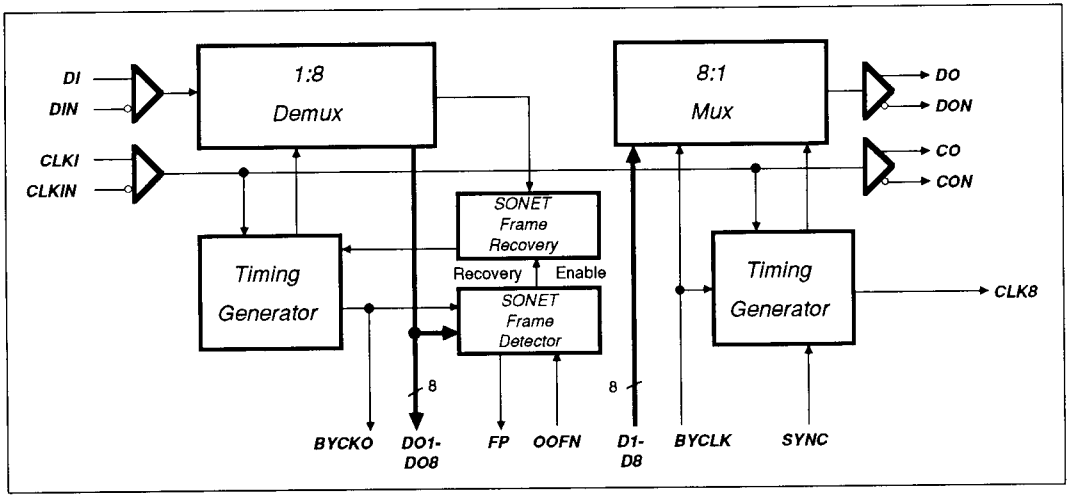
VS8011

The VS8011 is a high speed 8:1 multiplexer. The operation of the VS8011 exactly the same as that of the VS8010 8:1 Multiplexer circuitry described previously.

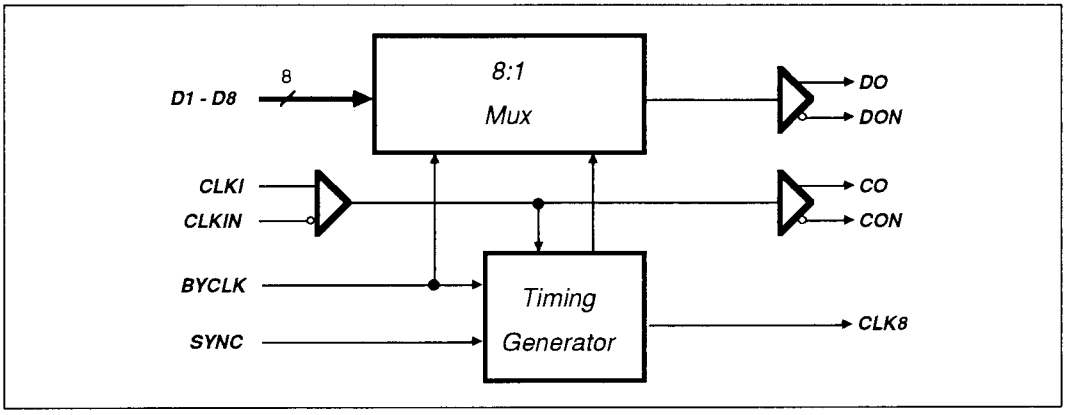
VS8012

The VS8012 integrates a 1:8 Demux and SONET frame recovery and detection circuitry on one chip. The operation of the VS8012 exactly the same as that of the VS8010 1:8 Demultiplexer and Frame Recovery circuits with the following exception. The frame recovery circuits are enabled by a falling edge on the ***OOFN*** ECL input when the additional ***FDIS*** ECL input is low. When the ***FDIS*** input is high the falling edge of ***OOFN*** disables the frame recovery circuit. The ***FDIS*** input is included to provide an alternative means of disabling the frame recovery circuit during device evaluation. In normal operation this input is wired to V_{TT} and the frame recovery circuit is disabled when serial F1's and F2's appear at the high speed differential serial data input ***(DI, DIN)***.

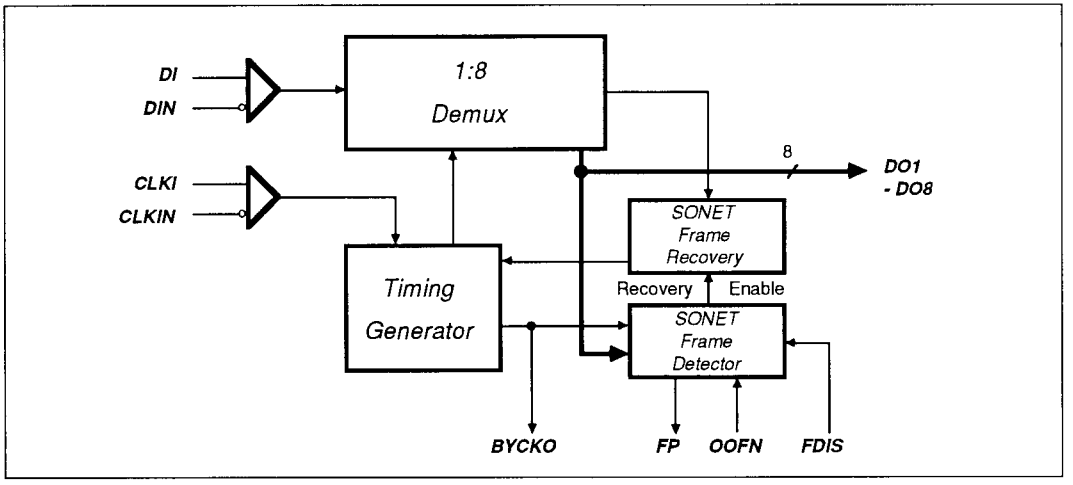
VS8010 BLOCK DIAGRAM



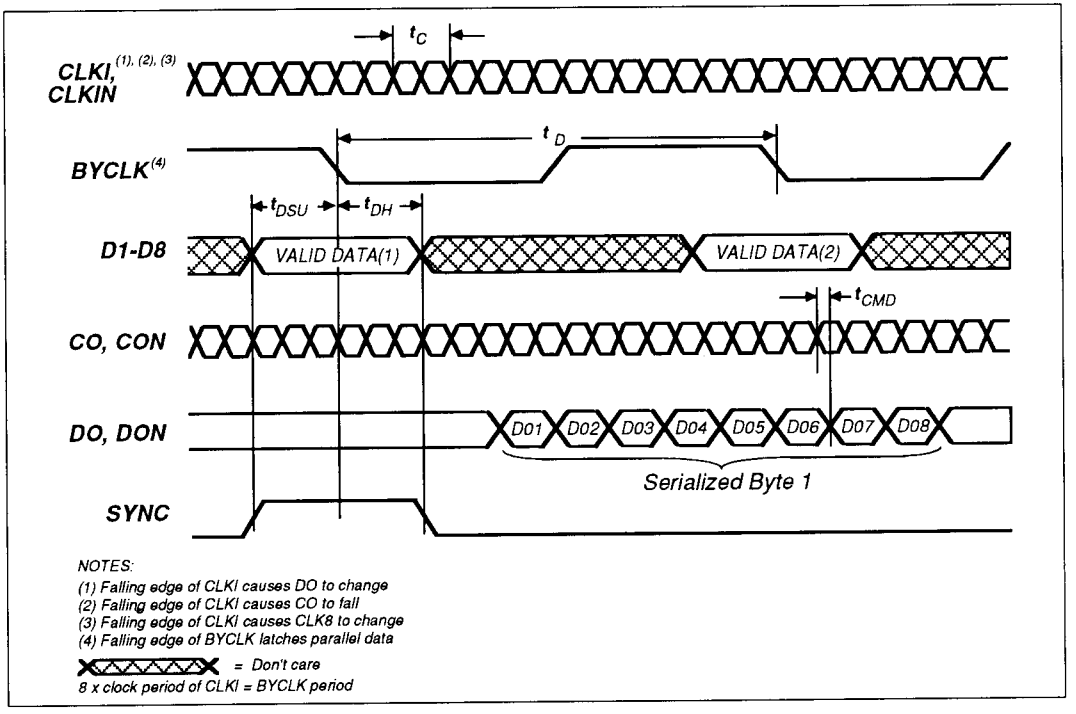
VS8011 BLOCK DIAGRAM



VS8012 BLOCK DIAGRAM



MULTIPLEXER WAVEFORMS (VS8010, VS8011)



NOTES:
(1) Falling edge of CLKI causes DO to change
(2) Falling edge of CLKI causes CO to fall
(3) Falling edge of CLKI causes CLK8 to change
(4) Falling edge of BYCLK latches parallel data

= *Don't care*

8 x clock period of CLKI = BYCLK period

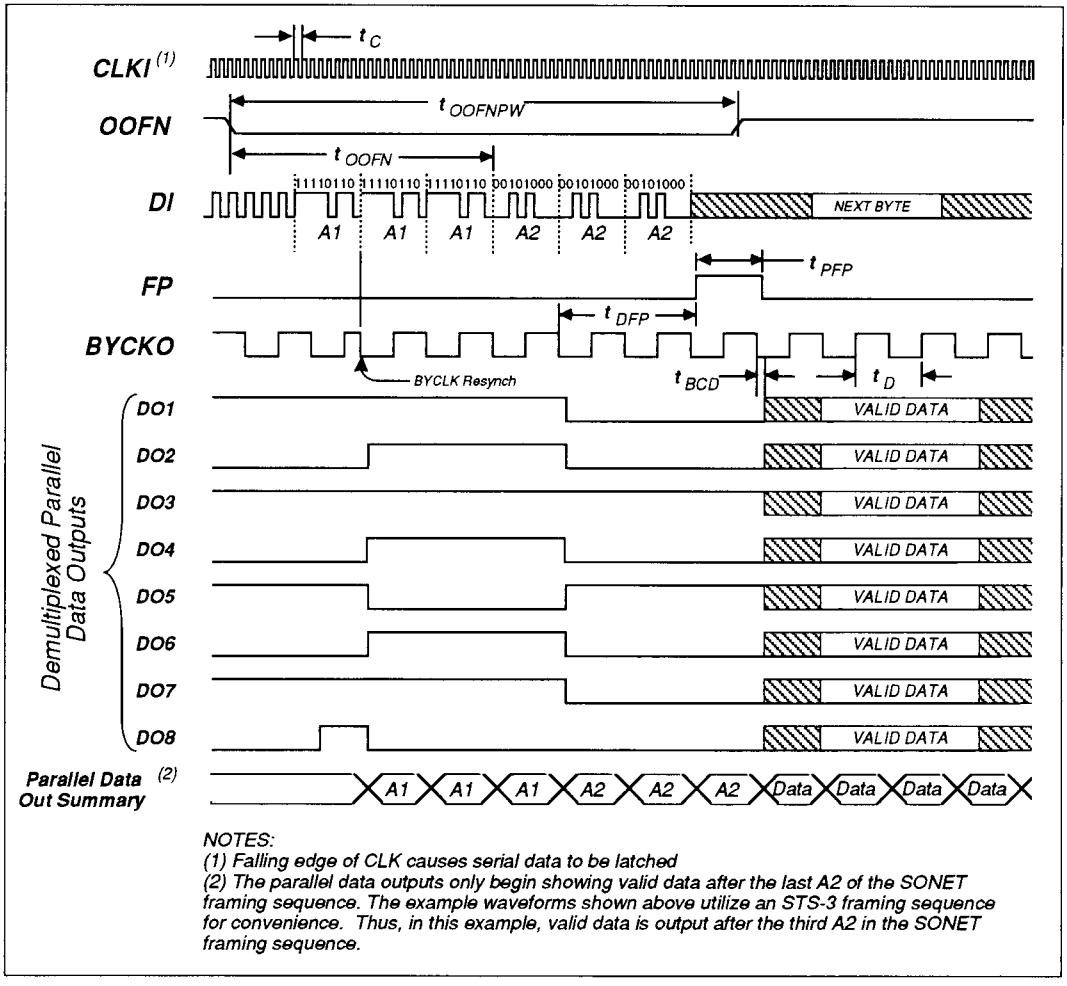
MULTIPLEXER AC CHARACTERISTICS (VS8010, VS8011)

(Over recommended operating conditions.)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
t_C	Clock period *	0.8	—	—	ns
t_D	BYTE clock period ($t_D = t_C$ x 8)	6.4	—	—	ns
t_{DSU}	Parallel data set-up time with respect to BYCLK	2.0	—	—	ns
t_{DH}	Data hold time with respect to BYCLK	1.0	—	—	ns
t_{CMD}	High speed clock output (CO, CON) to muxed data output (DO, DON) timing	—	500	—	ps
jitter	CLKI, CLKIN to DO, DON max-min, (HIGH to LOW), same part, same pin at constant conditions	—	<50	—	ps

** The parts are guaranteed by design to operate from DC to a maximum frequency of 1.25 GHz.*

DEMULTIPLEXER WAVEFORMS (VS8010, VS8012)



NOTES:
(1) Falling edge of CLK causes serial data to be latched
(2) The parallel data outputs only begin showing valid data after the last A2 of the SONET framing sequence. The example waveforms shown above utilize an STS-3 framing sequence for convenience. Thus, in this example, valid data is output after the third A2 in the SONET framing sequence.

DEMULTIPLEXER AC CHARACTERISTICS (VS8010, VS8012)

(Over recommended operating conditions.)

Parameter	Description	Min	Typ	Max	Units
t_C	Clock period *	0.8	—	—	ns
t_D	BYTE clock period ($t_D = t_C \times 8$)	6.4	—	—	ns
t_{DFP}	FP rising edge from parallel data output change from F1 to F2 ($t_{DFP} = t_D \times 2$)	—	12.8	—	ns
t_{PFP}	FP pulse width ($t_{PFP} = t_D$)	6.4	—	—	ns
t_{OOFN}	OOFN falling edge before A1 changes to A2 ($t_{OOFN} = t_D \times 4$)	—	25.6	—	ns
t_{OOFNPW}	OOFN pulse width ($t_{OOFNPW} = t_D$)	6.4	—	—	ns
Phase Margin	Serial data phase timing margin with respect to high speed clock input: $Phase\,Margin = \left(\frac{t_{SU} + t_H}{t_C}\right) 360^c$	135	—	—	degrees
t_{BCD}	Falling edge of **BYCKO** to valid parallel data output	t_c	t_c+0.5	t_c+1.5	ns

** If t_C changes, all the remaining parameters change as indicated by the equations.*

VS8010/VS8012 SONET FRAME RECOVERY AND DETECTION

The SONET framing sequence is a string of A1 bytes followed by a string of A2 bytes. (A1 = 11110110 and A2 = 00101000) The first serial bit starts at the left of the byte. The table below shows the number of A1 and A2 bytes in each SONET frame for different line rates. The VS8022 contains a frame recovery circuit and a frame detection circuit.

STS LEVEL	LINE RATE (Mb/S)	# OF A1 BYTES	# OF A2 BYTES
STS-3	155.520	3	3
STS-9	466.560	9	9
STS-12	622.080	12	12
STS-18	933.120	18	18
STS-24	1244.16	24	24
STS-48	2488.32	48	48

Example: STS-24 has 24 A1s and 24 A2s:
$A1_1A1_2A1_3$.....$A1_{24}A2_1A2_2A2_3$.....$A2_{24}$

Frame Recovery Circuit

The VS8010 Series SONET recovery circuits operate from STS-3 to STS-24. The frame recovery circuits look for 3 A1s followed by 3 A2s. The byte clock out ***(BYCKO)*** and parallel byte data out ***(DO_1-DO_8)*** become invalid on the falling edge of ***OOFN*** and become valid when A1 changes to A2. The frame recovery circuits align the received serial data on byte boundaries for demultiplexing by controlling the timing generator. The byte boundary alignment is based on specific A1 and A2 byte recognition.

The VS8010/12 have been designed to recognize 3 A1s followed by 3 A2s, and therefore recognize frames and align on byte boundaries for STS-3 through STS-24 line rates. As shown below, the framing sequence always contains 3 A1s followed by 3 A2s:

STS-24	(24 A1s & 24 A2s)
STS-18	(18 A1s & 18 A2s)
STS-12	(12 A1s &12 A2s)
STS-9	(9 A1s & 9 A2s)
STS-3	(3 A1s & 3 A2s)

The falling edge of ***OOFN*** must occur at least 4 byte clock periods before A1 changes to A2. The pulse width of ***OOFN*** must be at least 1 byte clock period.

Frame Detection Circuit

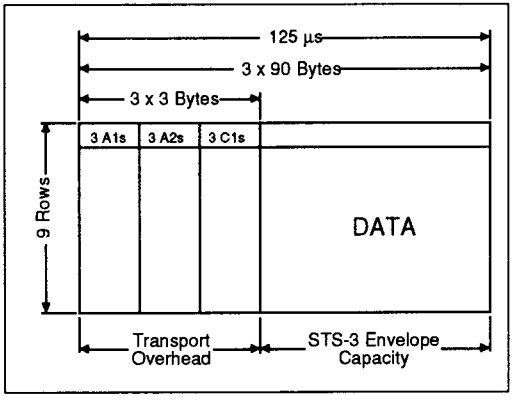
The frame detection circuit monitors the demultiplexed data, and senses the boundary between A1 and A2 bytes. If 3 A1 bytes followed by 3 A2 bytes are detected, then a frame confirmation signal is sent off-chip on the ECL output ***FP***. The rising edge of the ***FP*** pulse occurs 2 byte clock periods after A1 changes to A2 on the demultiplexer parallel data outputs. The ***FP*** pulse width is one byte clock period (refer to demultiplexer waveforms).

The frame detection circuitry also disables the frame recovery circuits once 3 A1 bytes are followed by 3 A2 bytes. The frame detector sends an ***FP*** pulse every frame when 3 A1s are followed by 3 A2s independent of the condition of the input ***OOFN***.

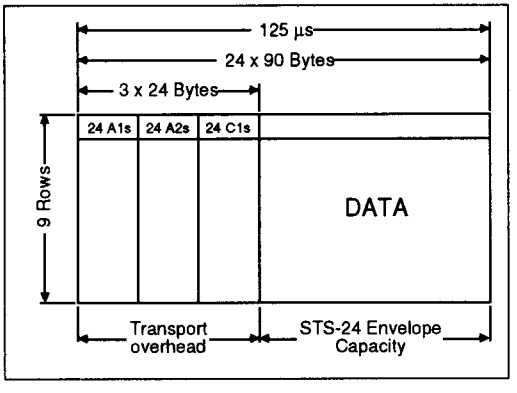
Circuit Operation

The frame recovery circuits are initialized and enabled on the falling edge of the ***OOFN*** ECL input with ***FDIS*** held low. The ***OOFN*** must be at least one byte clock period wide. It must occur at least 4 byte clock periods before the A1/A2 boundary. The circuit requires at least 2 A1 bytes followed by 2 A2 bytes for successful alignment. The first A1 byte is used by the frame recovery circuit to obtain initial word boundary alignment, while the following A1 and 2 A2 bytes are used to reset the frame recovery circuit and maintain alignment for the subsequent bit stream. Frame recovery and output alignment will occur only on the first A1 byte following a ***OOFN*** falling edge input. Frame recognition will occur for each word boundary aligned A1A2A2 sequence in the data stream. Frame recognition is signaled by a one byte clock period high pulse on the ***FP*** ECL output pin. This ***FP*** pulse will appear one byte period after the second A2 byte appears on the parallel data output pins.

STS-3 FRAME



STS-24 FRAME



NOTE: A1s & A2s: SONET framing sequence
C1s: STS Frame ID

ABSOLUTE MAXIMUM RATINGS [1]

Power Supply Voltage (V_{TT}) ..... -3.0 V to +0.5 V
Power Supply Voltage (V_{EE}) ..... V_{TT} +0.7 V to -6.0 V
ECL Input Voltage Applied [2], (V_{ECLIN}) ..... -2.5 V to +0.5 V
High Speed Input Voltage Applied [2], (V_{HSIN}) ..... V_{EE} - 0.7 V to V_{CC} + 0.7 V
Output Current, I_{OUT}, (DC, output HIGH) ..... -50 mA
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature [3], (T_{STG}) ..... -65° to +150°C

RECOMMENDED OPERATING CONDITIONS

ECL Power Supply Voltage, (V_{TT}) ..... -2.0 V ± 0.1V
Power Supply Voltage, (V_{EE}) ..... -5.2 V ± 0.26 V
Operating Temperature Range [3], (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to +85°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) V_{TT} must be applied before any input signal voltage (V_{ECLIN} and V_{HSIN}) must be greater than V_{TT} - 0.5V.
(3) Lower limit of specification is ambient temperature and upper limit is case temperature.

DC CHARACTERISTICS

ECL Inputs/Outputs

(Over recommended operating range with internal V_{REF}. V_{CC} = GND, output load = 50 Ω to -2.0 V.)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-925	—	-700	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	V_{TT}	—	-1750	mV	
V_{IH}	Input HIGH voltage	-1040	—	-600	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	V_{TT}	—	-1600	mV	Guaranteed LOW signal for all inputs
I_{IH}	Input HIGH current	—	10	200	µA	V_{IN} = V_{IH} max
I_{IL}	Input LOW current	-50	—	—	µA	V_{IN} = V_{IL} min
V_{REF}	ECL input reference, V_{BB} [2]	—	-1.29	—	V	

NOTE: 1) Differential ECL output pins must be terminated identically.
2) V_{REF} input is used to supply external VBB on chip for ECL 10K ECL compatibility.

High Speed Inputs and Outputs: CLKI, CLKIN, DO, DON

(Over recommended operating conditions. V_{CC} = GND, output load = 50 Ω to -2.0 V.)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage	-3.1	-3.0	-2.9	V	Guaranteed HIGH for high speed inputs
V_{IL}	Input LOW voltage	-4.1	-4.0	-3.9	V	Guaranteed LOW for high speed inputs
V_{OH}	Output HIGH voltage	—	-0.9	—	V	Output load, 50 Ω to -2.0 V
V_{OL}	Output LOW voltage	—	-1.8	—	V	Output load, 50 Ω to -2.0 V
ΔV_{OUT}	Output voltage swing	0.6	0.8	1.2	V	Output load, 50 Ω to -2.0 V

NOTES: 1) A reference generator is built into each high speed input, and these inputs are designed to be AC coupled.
2) If a high speed input is used single-ended, a 150pF capacitor must be connected between the unused high speed or complement input and V_{EE}.
3) Differential high speed outputs must be terminated identically.

3

HIGH SPEED DIFFERENTIAL CLOCK (C0,C0N) OUTPUTS (VS8010, VS8011)

V_{EE} = -5.2 ± 0.26 V, V_{CC} = GND, T_C = 0° to 70° C, Output load = 50 Ω to -2.0 V.)

The clock output swing at 1.25 GHz is 400 mVp-p from each output, centered at approximately -1.5 V
The clock output swing at DC is 1.0 Vp-p from each output, centered at approximately -1.5 V

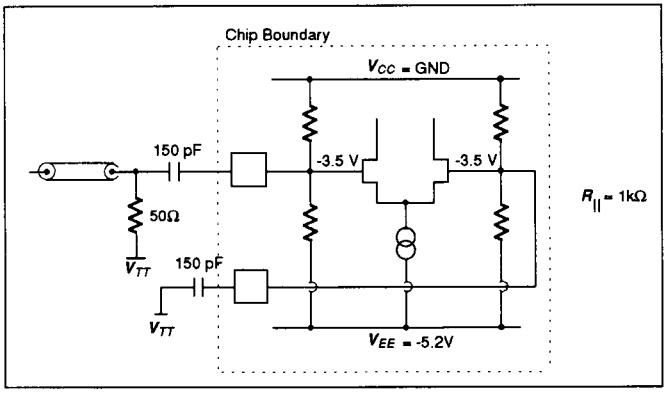
POWER DISSIPATION

(Over recommended operating conditions, V_{CC} = GND, outputs open circuit)

Parameter	Description	VS8010			VS8011			VS8012			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power supply current from V_{EE}	—	380	720	—	300	600	—	300	600	mA
I_{TT}	Power supply current from V_{TT}	—	450	900	—	110	220	—	125	250	mA
P_D	Power dissipation	—	2.9	5.8	—	1.9	3.7	—	2.0	3.8	W

HIGH SPEED INPUTS

High speed inputs (clock or data) provide for AC coupled operation. Internal biasing will position the reference voltage of approxiamtely -3.5 Volts on both the true and complementary inputs. Single-ended, AC coupled operation is illustrated at right.



VS8010 EXAMPLE APPLICATION: STS-24 SYSTEM

The objective of the system is to multiplex and demultiplex 8 data channels at the STS-24 line rate with SONET frame recovery capability. In this example the system is implemented using the two VS8010s as follows:

8:1 Multiplexer

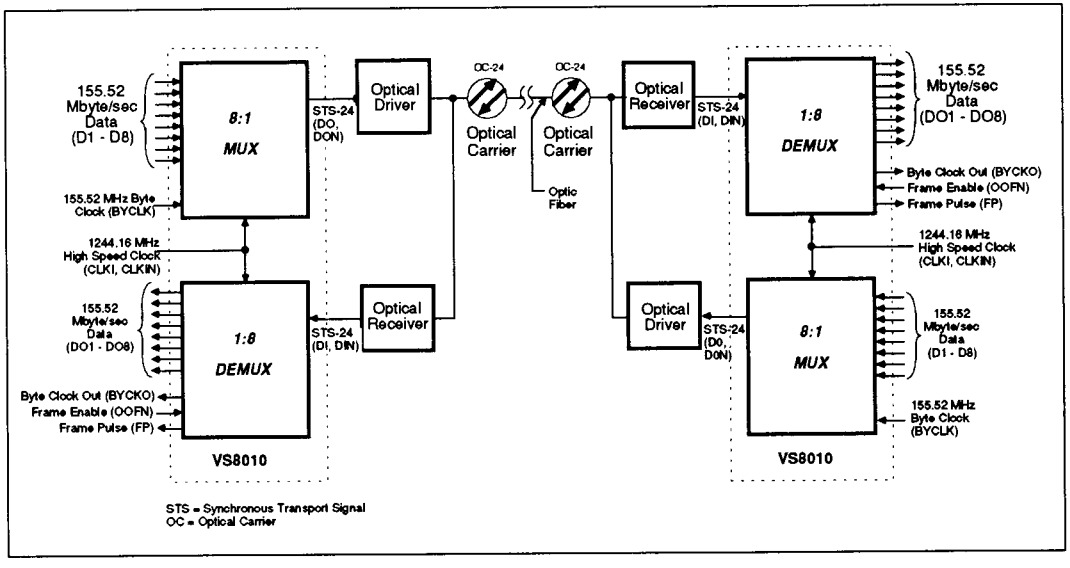
Data at a line rate of 155.52 Mbytes/sec is registered at the inputs using the 155.52 MHz byte clock. The 1244.16 MHz clock is used to generate timing signals for the mutiplexing function. The multiplexed output at 1244.16 Mbits/sec is generated at the serial data output (DO, DON) of the VS8010.

1:8 Demultiplexer

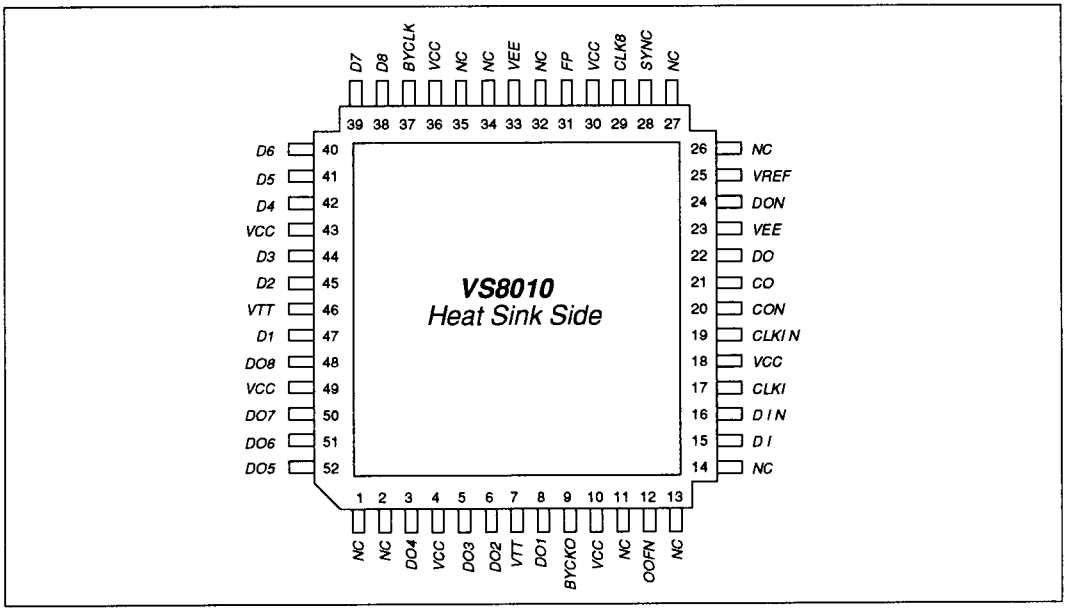
The 1:8 demultiplexer receives serial data at 1244.16 Mbits/sec and generates parallel data at 155.52 Mbytes/sec along with a byte clock output of 155.52 MHz. The demultiplexer also contains the SONET frame recovery and detection circuitry.

During system start-up the ***OOFN*** input receives a falling edge from the system control to recover the SONET frame and align on byte boundaries. Once the frame is aligned, the ***FP*** pulse is generated on every SONET frame. If for any reason the ***FP*** pulse disappears on frame boundaries then this signals the system that the frame synchronization is lost. The system then asserts the ***OOFN*** input (HIGH to LOW) to recover the SONET frame and align on byte boundaries, thus bringing the system back to a synchronized condition. The ***FP*** pulse begins appearing again on every frame.

SONET STS-24 SECTION LEVEL NODE



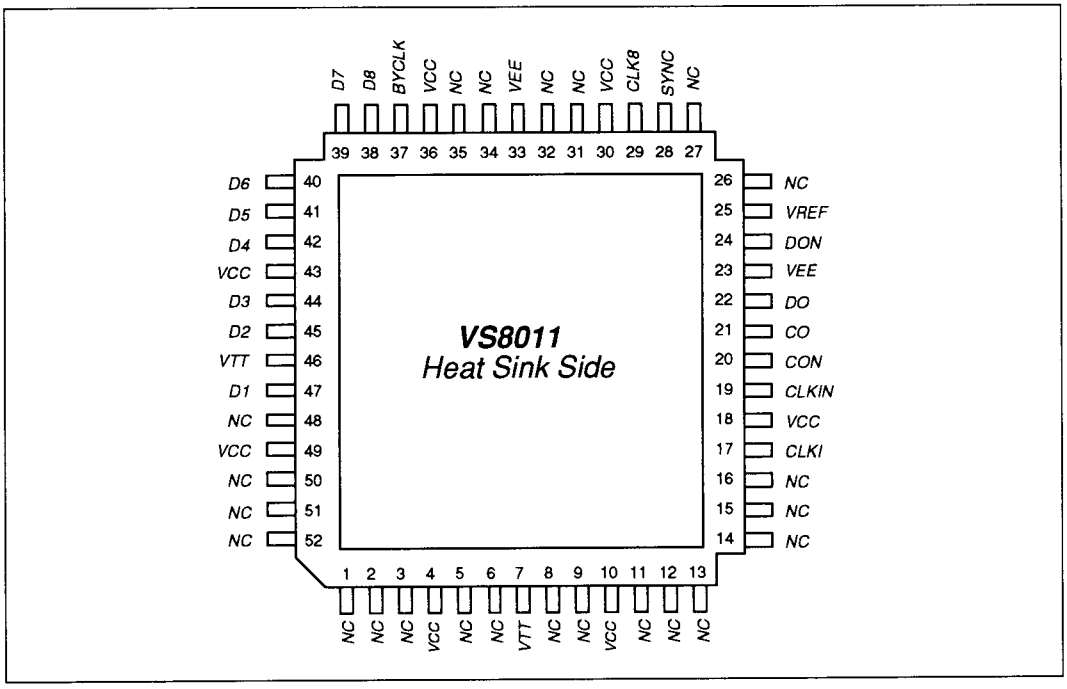
VS8010 PIN DIAGRAM



VS8010 PIN DESCRIPTION

Pin #	Name	I/O	Description
8, 6, 5, 3, 52 - 50, 48	***DO1 - DO8***	O	Parallel ECL data outputs
47, 45, 44, 42 - 38	***D1 - D8***	I	Parallel ECL data inputs
17, 19	***CLKI, CLKIN***	I	High speed differential clock inputs
9	***BYCKO***	O	Divide by 8 clock ECL output
37	***BYCLK***	I	Divide by 8 clock ECL input
22, 24	***DO, DON***	O	High speed serial data output
21, 20	***CO, CON***	O	High speed differential clock output
29	***CLK8***	O	Mux divide by 8 clock ECL output
15, 16	***DI, DIN***	O	High speed differential serial data input
12	***OOFN***	I	Frame recovery enable ECL input
31	***FP***	O	Frame detection confirmation ECL output
28	***SYNC***	I	Mux phase alignment enable ECL input
25	V_{REF}	I	ECL reference level input
4, 10, 18, 30, 36, 43, 49	V_{CC}		Ground connection
7, 46	V_{TT}		-2.0 V supply for internal reference generation & low power logic
23, 33	V_{EE}		-5.2 V supply for high speed logic
1, 2, 11, 13, 14, 26, 27, 32, 34, 35	***NC***		No connection

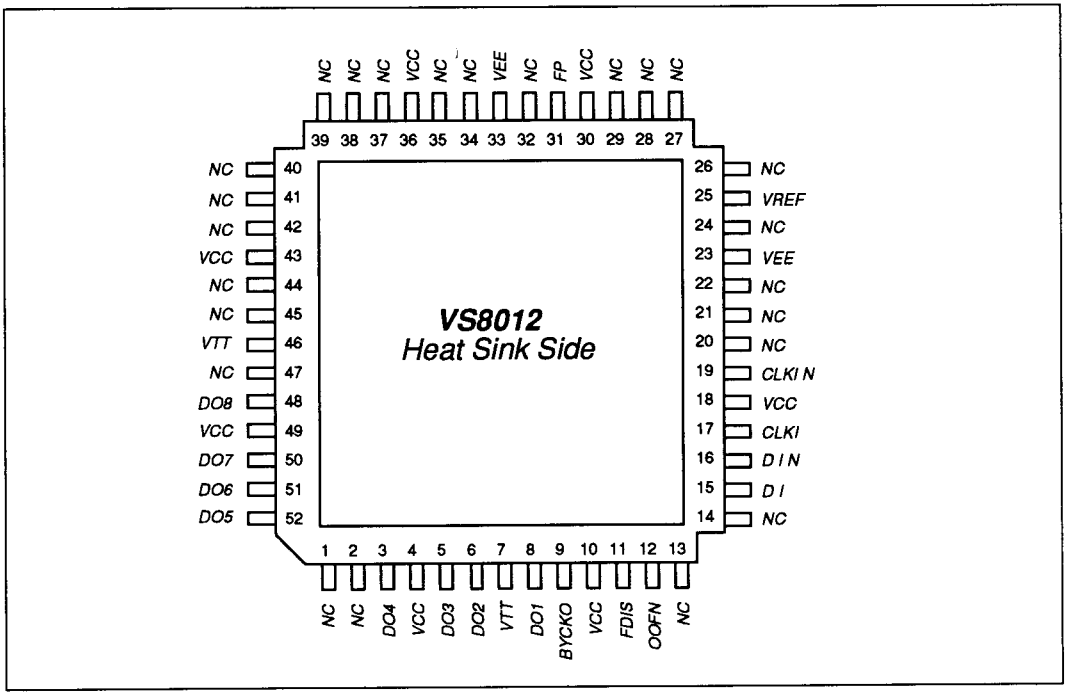
VS8011 PIN DIAGRAM



VS8011 PIN DESCRIPTION

Pin #	Name	I/O	Description
47, 45, 44, 42 - 38	***D1 - D8***	I	Parallel ECL data inputs
17, 19	***CLKI, CLKIN***	I	High speed differential clock inputs
37	***BYCLK***	I	Divide by 8 clock ECL input
22, 24	***DO, DON***	O	High speed serial data output
21, 20	***CO, CON***	O	High speed differential clock output
29	***CLK8***	O	Mux divide by 8 clock ECL output
28	***SYNC***	I	Mux phase alignment enable ECL input
25	V_{REF}	I	ECL reference level input
4, 10, 18, 30, 36, 43, 49	V_{CC}		Ground connection
7, 46	V_{TT}		-2.0 V supply for internal reference generation & low power logic
23, 33	V_{EE}		-5.2 V supply for high speed logic
1 - 3, 5, 6, 8, 9, 11 - 16, 26, 27, 31, 32, 34, 35, 48, 50 - 52	***NC***		No connection

VS8012 PIN DIAGRAM



VS8012 PIN DESCRIPTION

Pin #	Name	I/O	Description
8, 6, 5, 3, 52 - 50, 48	DO1 - DO8	O	Parallel ECL data outputs
17, 19	CLKI, CLKIN	I	High speed differential clock inputs
9	BYCKO	O	Divide by 8 clock ECL output
15, 16	DI, DIN	O	High speed differential serial data input
12	OOFN	I	Frame recovery enable ECL input
11	FDIS	I	Frame recovery disable ECL input
31	FP	O	Frame detection confirmation ECL output
25	V_{REF}	I	ECL reference level input
4, 10, 18, 30, 36, 43, 49	V_{CC}		Ground connection
7, 46	V_{TT}		-2.0 V supply for internal reference generation and low power logic
23, 33	V_{EE}		-5.2 V supply for high speed logic
1, 2, 13, 14, 20 - 22, 24, 26 - 29, 32, 34, 35, 37 - 42, 44, 45, 47	NC		No connection

VS8010DUT BOARD

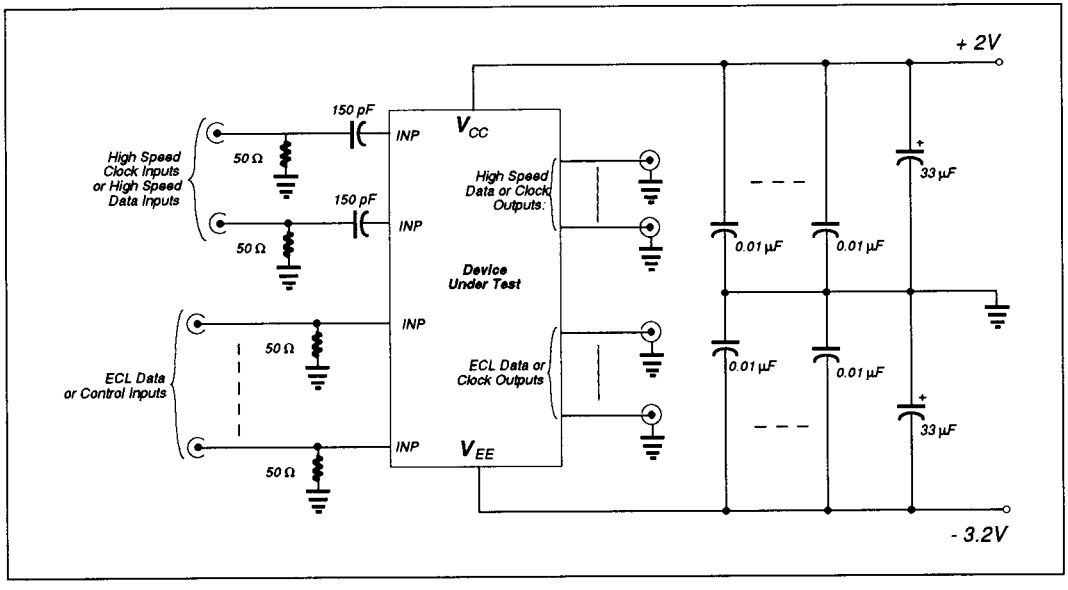
The VS8010DUT is a general purpose circuit board for the VS8010 series which provides a test bed suitable for evaluating the performance characteristics of the VS8010 series in the 52 pin LCC package. The evaluation board is generic to the VS8010 series, and is configured with I/Os which are specific to the VS8010 series.

The figure below is a schematic of this circuit board. This board provides a controlled impedance transmission line for all signals, and suitable decoupling for the power supplies. The signal traces have a characteristic impedance of 50 Ω. All ECL input lines are terminated with 50 Ω (chip resistor) as close to the device package pin as possible. The high speed inputs are also provided with 150 pF blocking capacitors as shown. These capacitors are shorted in applications which require DC connection to these inputs. Signals are launched onto the circuit board and removed by means of SMA coaxial connectors. While the input signals are terminated, the output signals are provided open circuit and are intended to be terminated in the measuring instrument such as an oscilloscope.

Normally, the VS8010 series operates in an ECL environment with standard ECL power buses: Ø V, -2 V, -5.2 V. In order to simplify interface to standard ground referenced test equipment, however, the circuit board power buses are offset so that the shield connectors are at ground voltage. The figure below shows the arrangement of the power supply decoupling capacitors. There is a 33 µF electrolytic capacitor, as well as several 0.01 µF ceramic capacitors across each power bus.

The device socket is an AMP 55227-1 LCC socket and was chosen for minimum inductance and shortest possible stub length. The figure on the next page shows the physical dimensions and the SMA connection labels for the VS8010DUT evaluation board.

VS8010DUT BOARD SCHEMATIC



VS8010DUT DIMENSIONS AND CONNECTION DIAGRAM