

# 1M x 1 CMOS Dynamic RAM

## Static Column

The MCM511002A is a 1.0 $\mu$  CMOS high-speed, dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost. The static column mode feature allows column data to be accessed upon the column address transition when  $\overline{\text{RAS}}$  and  $\overline{\text{CS}}$  are held low, similar to static RAM operation.

The MCM511002A requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300-mil dual-in-line plastic package (DIP), a 300-mil SOJ plastic package, and a 100-mil zig-zag in-line plastic package (ZIP).

- Three-State Data Output
- Common I/O with Early Write
- Static Column Mode
- Test Mode
- TTL-Compatible Inputs and Output
- $\overline{\text{RAS}}$  Only Refresh
- $\overline{\text{CS}}$  Before  $\overline{\text{RAS}}$  Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Output Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time ( $t_{\text{RAC}}$ ): MCM511002A-70 = 70 ns (Maximum)

NOT RECOMMENDED  
FOR NEW DESIGNS

- Low Active Power Dissipation: MCM511002A-80 = 440 mW (Maximum)  
MCM511002A-80 = 385 mW (Maximum)  
MCM511002A-10 = 330 mW (Maximum)
- Low Standby Power Dissipation: 11 mW (Maximum, TTL Levels)  
5.5 mW (Maximum, CMOS Levels)

### MCM511002A



P PACKAGE  
300 MIL PLASTIC  
CASE 707A



J PACKAGE  
300 MIL SOJ  
CASE 822

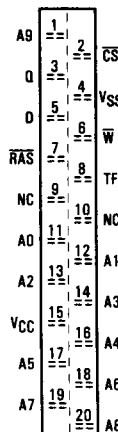


Z PACKAGE  
PLASTIC  
ZIG-ZAG IN-LINE  
CASE 836

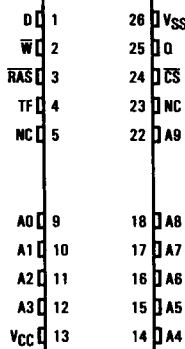
#### PIN NAMES

A0-A9	Address Input
D	Data Input
Q	Data Output
W	Read/Write Enable
$\overline{\text{RAS}}$	Row Address Strobe
CS	Chip Select
VCC	Power (+5 V)
VSS	Ground
TF	Test Function Enable
NC	No Connection

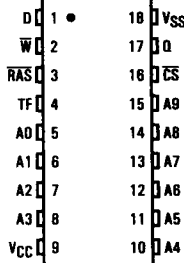
#### ZIG-ZAG IN-LINE



#### SMALL OUTLINE

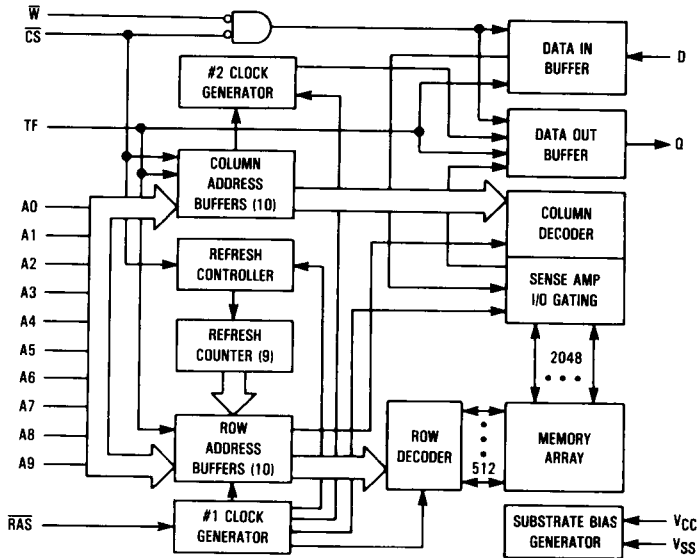


#### DUAL-IN-LINE



#### PIN ASSIGNMENT

**BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS** (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}$	-1 to +7	V
Voltage Relative to $V_{SS}$ for Any Pin Except $V_{CC}$	$V_{in}, V_{out}$	-1 to +7	V
Test Function Input Voltage	$V_{in(TF)}$	-1 to +10.5	V
Data Out Current	$I_{out}$	50	mA
Power Dissipation	$P_D$	600	mW
Operating Temperature Range	$T_A$	0 to +70	$^{\circ}C$
Storage Temperature Range	$T_{stg}$	-55 to +150	$^{\circ}C$

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

(V<sub>CC</sub> = 5.0 V ± 10%, T<sub>A</sub> = 0 to 70°C, Unless Otherwise Noted)

### RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V <sub>CC</sub>	4.5	5.0	5.5	V	1
	V <sub>SS</sub>	0	0	0		
Logic High Voltage, All Inputs	V <sub>IH</sub>	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V <sub>IL</sub>	-1.0	—	0.8	V	1
Test Function Input High Voltage	V <sub>IH</sub> (TF)	V <sub>CC</sub> + 4.5	—	10.5	V	1

### DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V <sub>CC</sub> Power Supply Current MCM511002A-70, t <sub>RC</sub> = 130 ns MCM511002A-80, t <sub>RC</sub> = 150 ns MCM511002A-10, t <sub>RC</sub> = 180 ns	I <sub>CC1</sub>	—	80 70 60	mA	2
V <sub>CC</sub> Power Supply Current (Standby) ( $\overline{RAS} = \overline{CS} = V_{IH}$ )	I <sub>CC2</sub>	—	2.0	mA	
V <sub>CC</sub> Power Supply Current During $\overline{RAS}$ only Refresh Cycles ( $\overline{CS} = V_{IH}$ ) MCM511002A-70, t <sub>RC</sub> = 130 ns MCM511002A-80, t <sub>RC</sub> = 150 ns MCM511002A-10, t <sub>RC</sub> = 180 ns	I <sub>CC3</sub>	—	80 70 60	mA	2
V <sub>CC</sub> Power Supply Current During Static Column Mode Cycle ( $\overline{RAS} = \overline{CS} = V_{IL}$ ) MCM511002A-70, t <sub>SC</sub> = 40 ns MCM511002A-80, t <sub>SC</sub> = 45 ns MCM511002A-10, t <sub>SC</sub> = 50 ns	I <sub>CC4</sub>	—	60 50 40	mA	2, 3
V <sub>CC</sub> Power Supply Current (Standby) ( $\overline{RAS} = \overline{CS} = V_{CC} - 0.2$ V)	I <sub>CC5</sub>	—	1.0	mA	
V <sub>CC</sub> Power Supply Current During $\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle MCM511002A-70, t <sub>RC</sub> = 130 ns MCM511002A-80, t <sub>RC</sub> = 150 ns MCM511002A-10, t <sub>RC</sub> = 180 ns	I <sub>CC6</sub>	—	80 70 60	mA	2
Input Leakage Current (Except TF) (0 V ≤ V <sub>in</sub> ≤ 6.5 V)	I <sub>kg(I)</sub>	-10	10	μA	
Input Leakage Current (TF) (0 V ≤ V <sub>in(TF)</sub> ≤ V <sub>CC</sub> + 0.5 V)	I <sub>kg(I)</sub>	-10	10	μA	
Output Leakage Current ( $\overline{CS} = V_{IH}$ , 0 V ≤ V <sub>out</sub> ≤ 5.5 V)	I <sub>kg(O)</sub>	-10	10	μA	
Test Function Input Current (V <sub>CC</sub> + 4.5 V ≤ V <sub>in(TF)</sub> ≤ 10.5 V)	I <sub>in(TF)</sub>	—	1	mA	
Output High Voltage (I <sub>OH</sub> = -5 mA)	V <sub>OH</sub>	2.4	—	V	
Output Low Voltage (I <sub>OL</sub> = 4.2 mA)	V <sub>OL</sub>	—	0.4	V	

### CAPACITANCE (f = 1.0 MHz, T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit	Notes
Input Capacitance A0-A9, D $\overline{RAS}$ , $\overline{CS}$ , $\overline{W}$ , TF	C <sub>in</sub>	5	pF	4
		7	pF	4
Output Capacitance ( $\overline{CS} = V_{IH}$ to Disable Output)	C <sub>out</sub>	7	pF	4

#### NOTES:

- All voltages referenced to V<sub>SS</sub>.
- Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
- Measured with one address transition per static column mode cycle.
- Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = IΔt/ΔV.

## AC OPERATING CONDITIONS AND CHARACTERISTICS

(V<sub>CC</sub> = 5.0 V ± 10%, T<sub>A</sub> = 0 to 70°C, Unless Otherwise Noted)

### READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM511002A-70		MCM511002A-80		MCM511002A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t <sub>RELREL</sub>	t <sub>RC</sub>	130	—	150	—	180	—	ns	6
Read-Write Cycle Time	t <sub>RELREL</sub>	t <sub>RWC</sub>	155	—	155	—	210	—	ns	6
Static Column Mode Cycle Time	t <sub>AVAV</sub>	t <sub>SC</sub>	40	—	45	—	50	—	ns	
Static Column Mode Read-Write Cycle Time	t <sub>AVAV</sub>	t <sub>SRWC</sub>	70	—	80	—	100	—	ns	
Access Time from RAS	t <sub>RELOV</sub>	t <sub>RAC</sub>	—	70	—	80	—	100	ns	7, 8
Access Time from CS	t <sub>CELOV</sub>	t <sub>CAC</sub>	—	20	—	20	—	25	ns	7, 9
Access Time from Column Address	t <sub>AVQV</sub>	t <sub>AA</sub>	—	35	—	40	—	50	ns	7, 10
Access Time from Last Write	t <sub>WLQV</sub>	t <sub>ALW</sub>	—	65	—	75	—	95	ns	7, 11
CS to Output in Low-Z	t <sub>CELOX</sub>	t <sub>CLZ</sub>	0	—	0	—	0	—	ns	7
Output Buffer and Turn-Off Delay	t <sub>CEHOZ</sub>	t <sub>OFF</sub>	0	20	0	20	0	20	ns	12
Data Out Hold from Address Change	t <sub>AXQX</sub>	t <sub>AOH</sub>	5	—	5	—	5	—	ns	
Data Out Enable from Write	t <sub>WHQV</sub>	t <sub>OW</sub>	—	20	—	20	—	25	ns	
Data Out Hold from Write	t <sub>WHQX</sub>	t <sub>WOH</sub>	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t <sub>T</sub>	t <sub>T</sub>	3	50	3	50	3	50	ns	
RAS Precharge Time	t <sub>REHREL</sub>	t <sub>RP</sub>	50	—	60	—	70	—	ns	
RAS Pulse Width	t <sub>RELREH</sub>	t <sub>RAS</sub>	70	10,000	80	10,000	100	10,000	ns	
RAS Pulse Width (Static Column Mode)	t <sub>RELREH</sub>	t <sub>RASC</sub>	70	100,000	80	100,000	100	100,000	ns	
RAS Hold Time	t <sub>CELREH</sub>	t <sub>RSH</sub>	20	—	20	—	25	—	ns	
CS Hold Time	t <sub>RELCEH</sub>	t <sub>CSH</sub>	70	—	80	—	100	—	ns	
CS Pulse Width	t <sub>CELCEH</sub>	t <sub>CS</sub>	20	10,000	20	10,000	25	10,000	ns	
CS Pulse Width (Static Column Mode)	t <sub>CELCEH</sub>	t <sub>CSC</sub>	20	100,000	20	100,000	25	100,000	ns	
RAS to CS Delay Time	t <sub>RELCEL</sub>	t <sub>RCD</sub>	20	50	20	60	25	75	ns	13
RAS to Column Address Delay Time	t <sub>RELAV</sub>	t <sub>RAD</sub>	15	35	15	40	20	50	ns	14
CS to RAS Precharge Time	t <sub>CEHREL</sub>	t <sub>CRP</sub>	5	—	5	—	5	—	ns	
CS Precharge Time (Static Column Mode Cycle Only)	t <sub>CEHCEL</sub>	t <sub>CP</sub>	10	—	10	—	10	—	ns	
Row Address Setup Time	t <sub>AVREL</sub>	t <sub>ASR</sub>	0	—	0	—	0	—	ns	
Row Address Hold Time	t <sub>RELAX</sub>	t <sub>RAH</sub>	10	—	10	—	15	—	ns	

(continued)

#### NOTES:

- V<sub>IH</sub> min and V<sub>IL</sub> max are reference levels for measuring timing of input signals. Transition times are measured between V<sub>IH</sub> and V<sub>IL</sub>.
- An initial pause of 200 μs is required after power-up followed by 8 RAS cycles before proper device operation is guaranteed.
- The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V<sub>IH</sub> and V<sub>IL</sub> (or between V<sub>IL</sub> and V<sub>IH</sub>) in a monotonic manner.
- AC measurements t<sub>T</sub> = 5.0 ns.
- TF pin must be at V<sub>IL</sub> or open if not used.
- The specifications for t<sub>RC</sub> (min) and t<sub>RWC</sub> (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
- Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V<sub>OH</sub> = 2.0 V and V<sub>OL</sub> = 0.8 V.
- Assumes that t<sub>RCD</sub> ≤ t<sub>RCD</sub> (max).
- Assumes that t<sub>RCD</sub> ≥ t<sub>RCD</sub> (max).
- Assumes that t<sub>RAD</sub> ≥ t<sub>RAD</sub> (max), and/or t<sub>LWAD</sub> ≥ t<sub>LWAD</sub> (max).
- Assumes that t<sub>LWAD</sub> ≤ t<sub>LWAD</sub> (max).
- t<sub>OFF</sub> (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Operation within the t<sub>RCD</sub> (max) limit ensures that t<sub>RAC</sub> (max) can be met. t<sub>RCD</sub> (max) is specified as a reference point only; if t<sub>RCD</sub> is greater than the specified t<sub>RCD</sub> (max) limit, then access time is controlled exclusively by t<sub>CAC</sub>.
- Operation within the t<sub>RAD</sub> (max) limit ensures that t<sub>RAC</sub> (max) can be met. t<sub>RAD</sub> (max) is specified as a reference point only; if t<sub>RAD</sub> is greater than the specified t<sub>RAD</sub> (max), then access time is controlled exclusively by t<sub>AA</sub>.

2

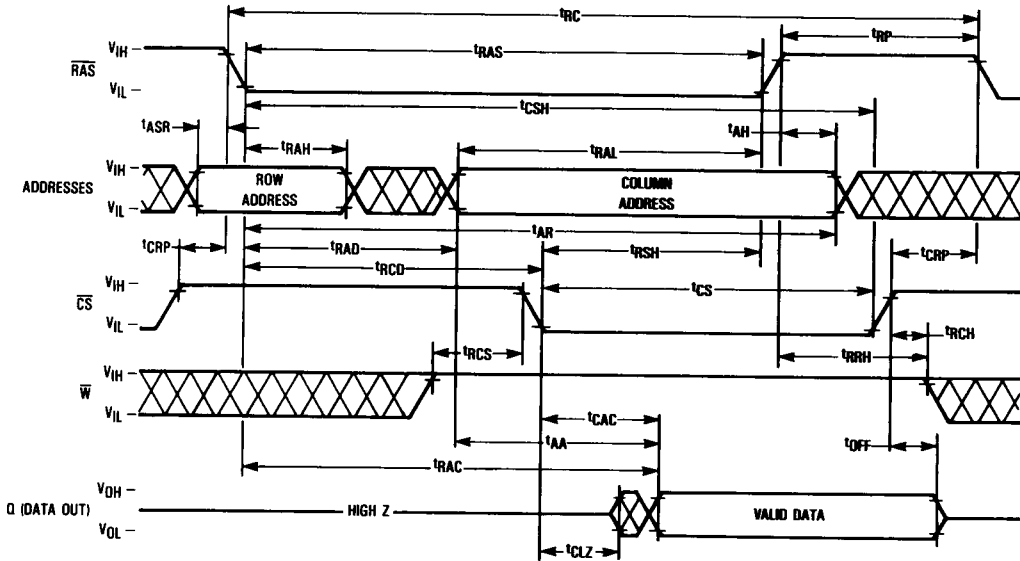
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM511002A-70		MCM511002A-80		MCM511002A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Column Address Setup Time	t <sub>AVCEL</sub>	t <sub>ASCH</sub>	0	—	0	—	0	—	ns	
Column Address Hold Time	t <sub>CELAX</sub>	t <sub>CAH</sub>	15	—	15	—	20	—	ns	
Write Address Hold Time Referenced to RAS	t <sub>RELAX</sub>	t <sub>AWR</sub>	55	—	60	—	75	—	ns	
Column Address Hold Time Referenced to RAS	t <sub>RELAX</sub>	t <sub>AR</sub>	80	—	90	—	115	—	ns	
Column Address to RAS Lead Time	t <sub>AVREH</sub>	t <sub>RAL</sub>	35	—	40	—	50	—	ns	
Column Address Hold Time Referenced to RAS High	t <sub>REHAX</sub>	t <sub>AH</sub>	5	—	5	—	10	—	ns	15
Write Command to CS Lead Time	t <sub>WLCEH</sub>	t <sub>CWL</sub>	20	—	20	—	25	—	ns	
Last Write to Column Address Delay Time	t <sub>WLAV</sub>	t <sub>LWAD</sub>	20	30	20	35	25	45	ns	16
Last Write to Column Address Hold Time	t <sub>WLAX</sub>	t <sub>AHLW</sub>	65	—	75	—	95	—	ns	
Read Command Setup Time	t <sub>WHCEL</sub>	t <sub>RCS</sub>	0	—	0	—	0	—	ns	
Read Command Hold Time	t <sub>CEHWX</sub>	t <sub>RCH</sub>	0	—	0	—	0	—	ns	17
Read Command Hold Time Referenced to RAS	t <sub>REHWX</sub>	t <sub>RRH</sub>	0	—	0	—	0	—	ns	17
Write Command Hold Time	t <sub>CELWX</sub>	t <sub>WCH</sub>	15	—	15	—	20	—	ns	18
Write Command Hold Time Referenced to RAS	t <sub>RELWH</sub>	t <sub>WCR</sub>	55	—	60	—	75	—	ns	
Write Command Pulse Width	t <sub>WLWH</sub>	t <sub>WP</sub>	15	—	15	—	20	—	ns	
Write Command Inactive Time	t <sub>WHWL</sub>	t <sub>WI</sub>	10	—	10	—	10	—	ns	
Write Command to RAS Lead Time	t <sub>WLREH</sub>	t <sub>RWL</sub>	20	—	20	—	25	—	ns	
Data In Setup Time	t <sub>DVCEL</sub>	t <sub>DS</sub>	0	—	0	—	0	—	ns	19
Data In Hold Time	t <sub>CELDX</sub>	t <sub>DH</sub>	15	—	15	—	20	—	ns	19
Data In Hold Time Referenced to RAS	t <sub>RELDX</sub>	t <sub>DHR</sub>	55	—	60	—	75	—	ns	
Refresh Period	t <sub>RVRV</sub>	t <sub>RFSSH</sub>	—	8	—	8	—	8	ms	
Write Command Setup Time (Output Data Disable)	t <sub>WLCEL</sub>	t <sub>WCS</sub>	0	—	0	—	0	—	ns	18
CS to Write Delay	t <sub>CELWL</sub>	t <sub>CWD</sub>	20	—	20	—	25	—	ns	18
RAS to Write Delay	t <sub>RELWL</sub>	t <sub>RWD</sub>	70	—	80	—	100	—	ns	18
Column Address to Write Delay Time	t <sub>AWWL</sub>	t <sub>AWD</sub>	35	—	40	—	50	—	ns	18
CS Setup Time for CS Before RAS Refresh	t <sub>RELCEL</sub>	t <sub>CSR</sub>	10	—	10	—	10	—	ns	
CS Hold Time for CS Before RAS Refresh	t <sub>RELCEH</sub>	t <sub>CHR</sub>	30	—	30	—	30	—	ns	
CS Precharge to CS Active Time	t <sub>REHCEL</sub>	t <sub>RPC</sub>	0	—	0	—	0	—	ns	
CS Precharge Time for CS Before RAS Counter Test	t <sub>CEHCEL</sub>	t <sub>CPT</sub>	40	—	40	—	50	—	ns	
CS Precharge Time	t <sub>CEHCEL</sub>	t <sub>CPN</sub>	10	—	10	—	15	—	ns	
Test Mode Enable Setup Time Referenced to RAS	t <sub>TEHREL</sub>	t <sub>TES</sub>	0	—	0	—	0	—	ns	
Test Mode Enable Hold Time Referenced to RAS	t <sub>REHTEL</sub>	t <sub>TEHR</sub>	0	—	0	—	0	—	ns	
Test Mode Enable Hold Time Referenced to CAS	t <sub>CEHTEL</sub>	t <sub>TEHC</sub>	0	—	0	—	0	—	ns	

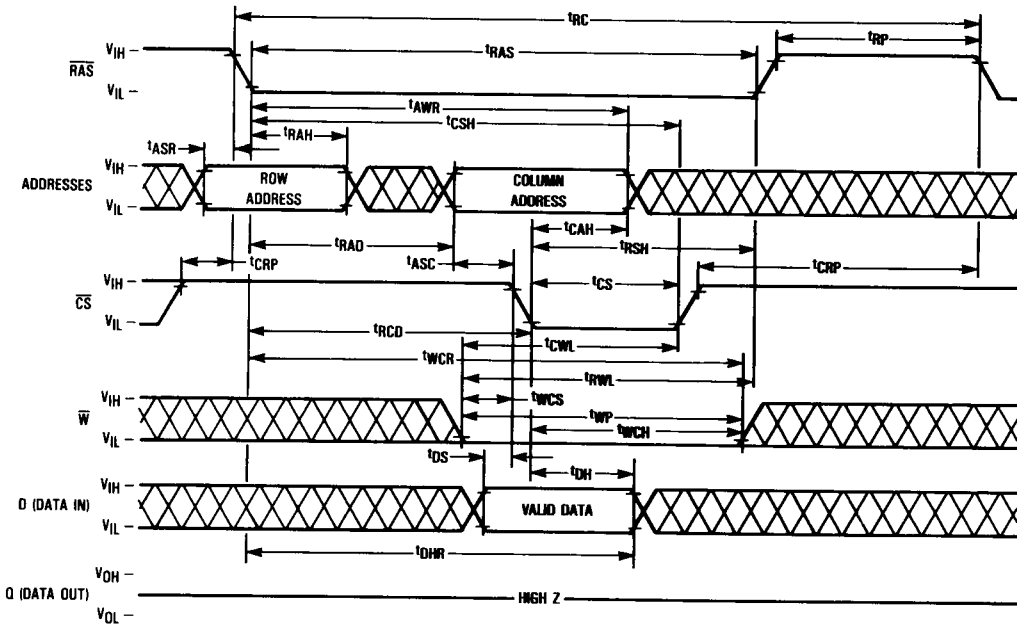
NOTES:

15. t<sub>AH</sub> must be met for a read cycle.
16. Operation within the t<sub>LWAD</sub> limit ensures that t<sub>ALW</sub> can be met. t<sub>LWAD</sub> (max) is specified as a reference point only; if t<sub>LWAD</sub> is greater than the specified t<sub>LWAD</sub> (max) limit, then access time is controlled exclusively by t<sub>AA</sub>.
17. Either t<sub>RRH</sub> or t<sub>RCH</sub> must be satisfied for a read cycle.
18. t<sub>WCS</sub>, t<sub>WCH</sub>, t<sub>RWD</sub>, t<sub>CWD</sub>, and t<sub>AWD</sub> are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t<sub>WCS</sub> ≥ t<sub>WCS</sub> (min) and t<sub>WCH</sub> ≥ t<sub>WCH</sub> (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t<sub>RWD</sub> ≥ t<sub>RWD</sub> (min), t<sub>CWD</sub> ≥ t<sub>CWD</sub> (min), and t<sub>AWD</sub> ≥ t<sub>AWD</sub> (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
19. These parameters are referenced to CS leading edge in early write cycles and to W leading edge in late write or read-write cycles.

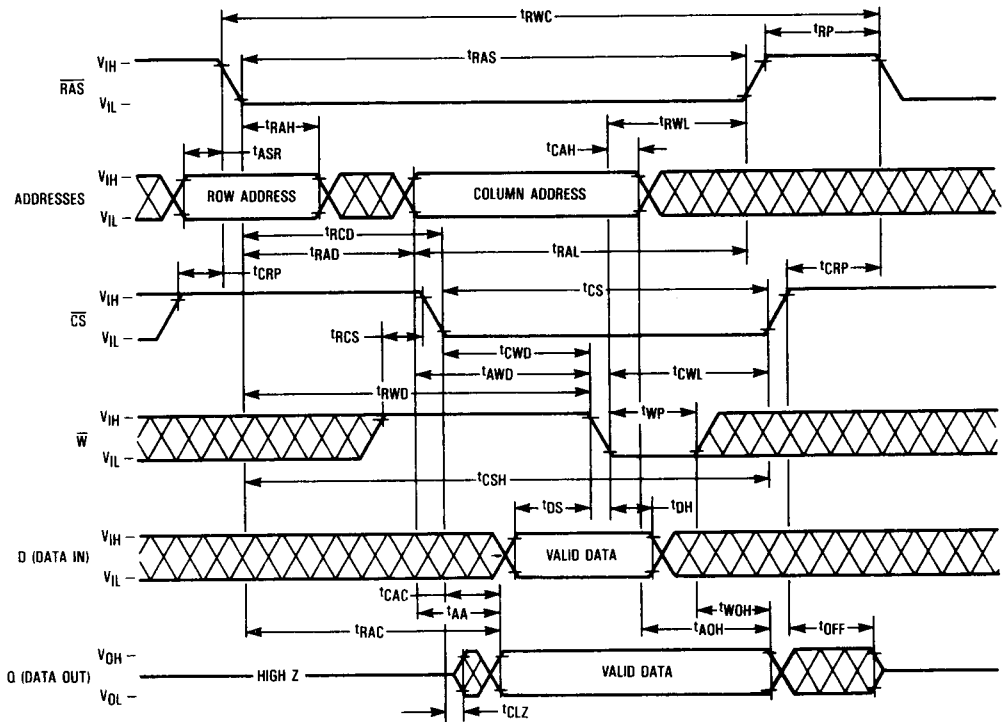
READ CYCLE



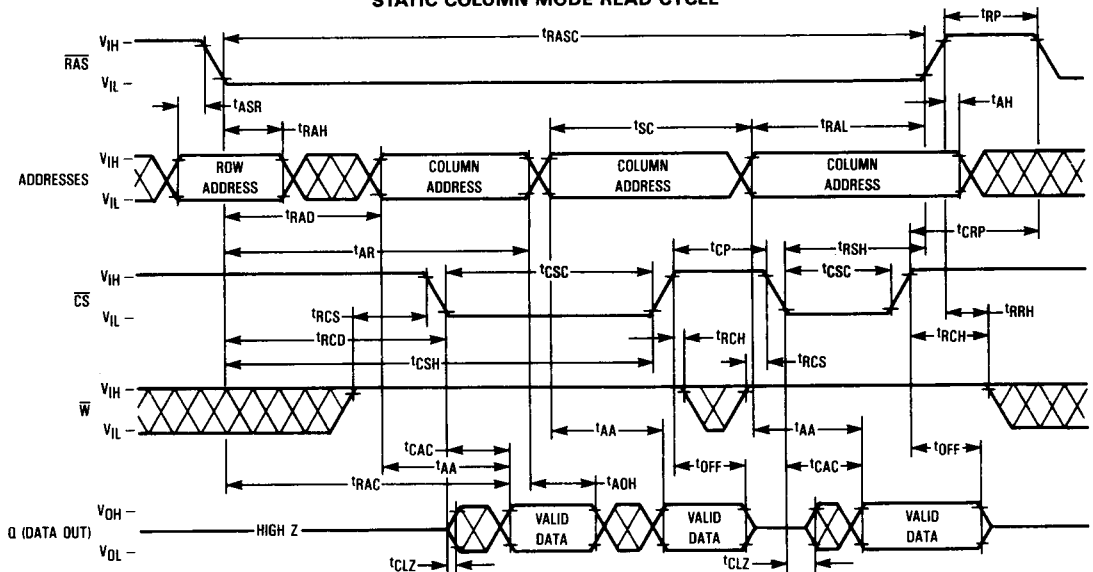
EARLY WRITE CYCLE



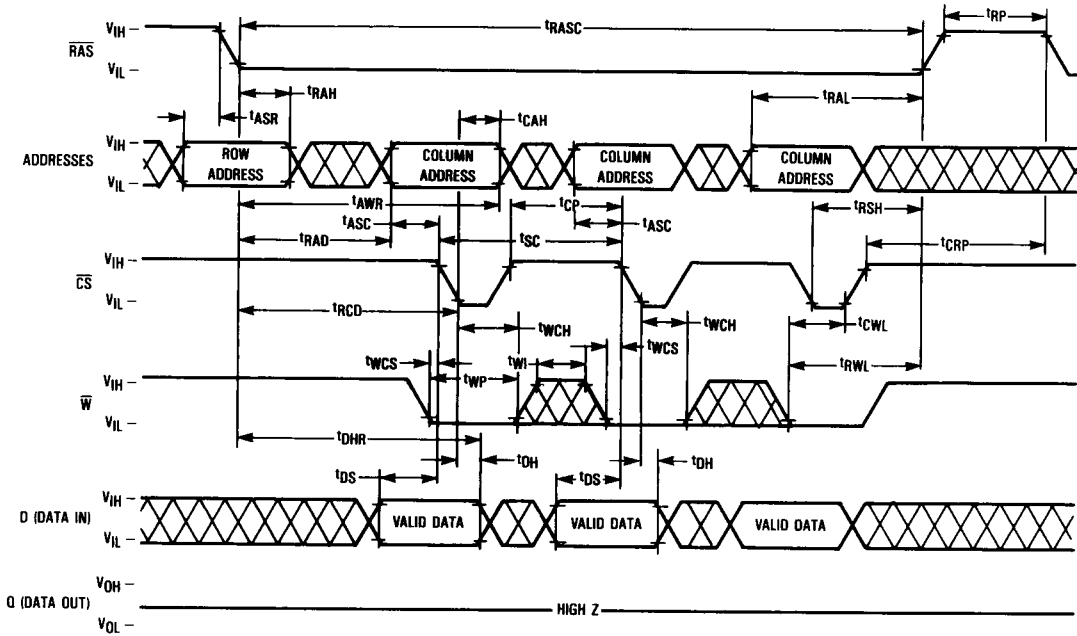
READ-WRITE CYCLE



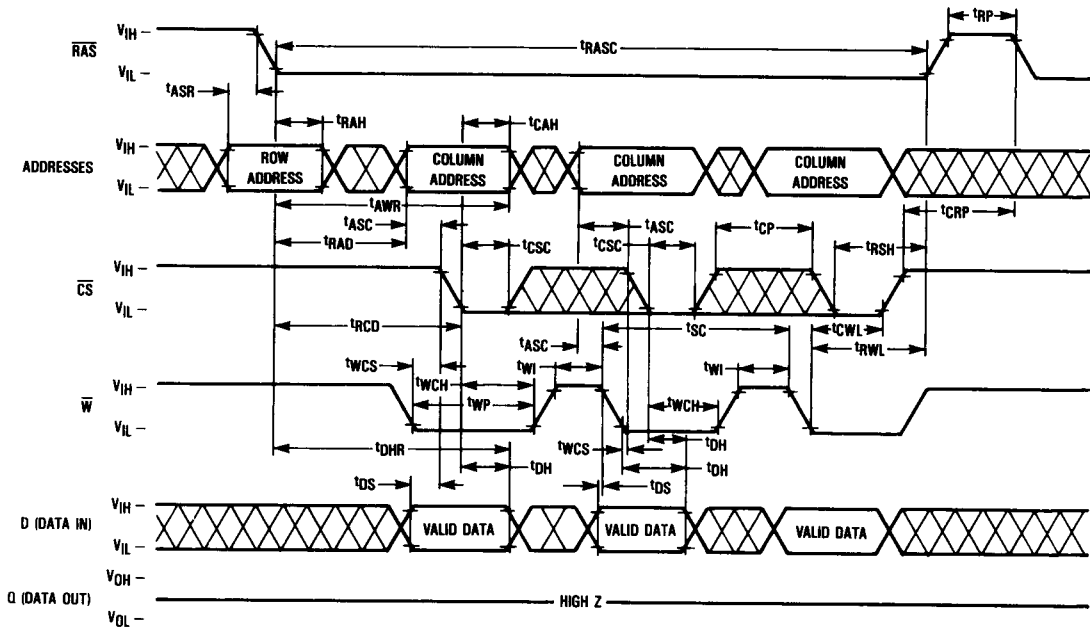
STATIC COLUMN MODE READ CYCLE



STATIC COLUMN MODE EARLY WRITE CYCLE (A)

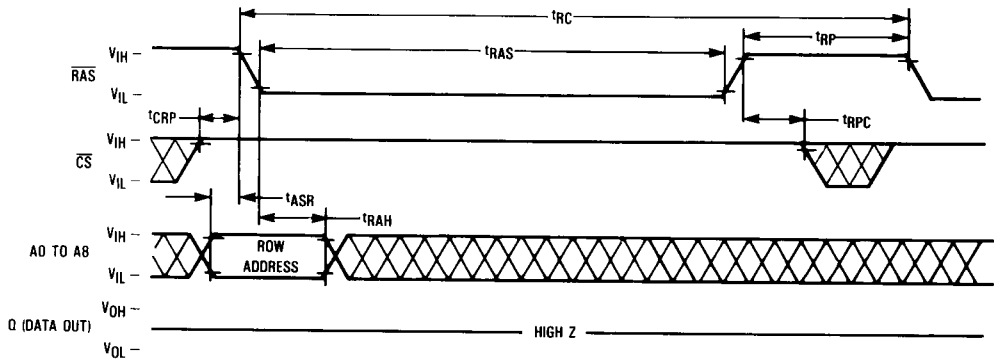


STATIC COLUMN MODE EARLY WRITE CYCLE (B)

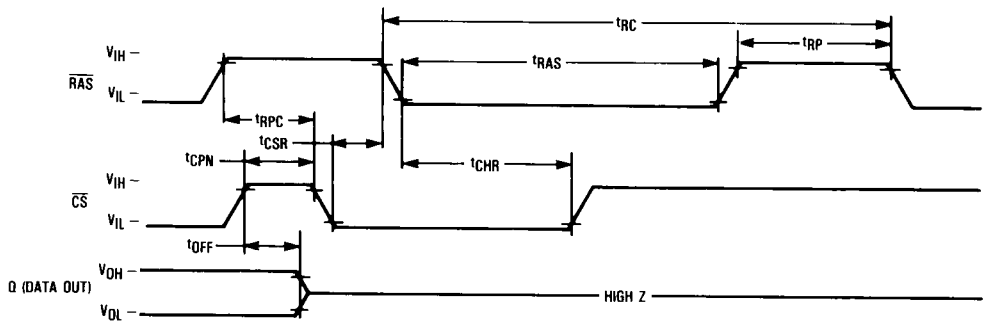




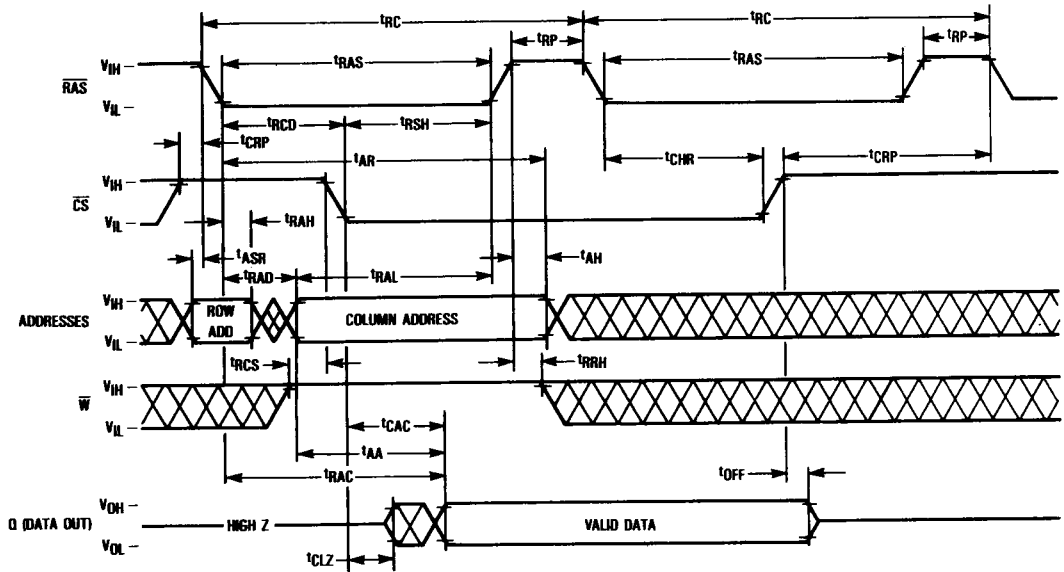
### RAS ONLY REFRESH CYCLE ( $\bar{W}$ and A9 are Don't Care)



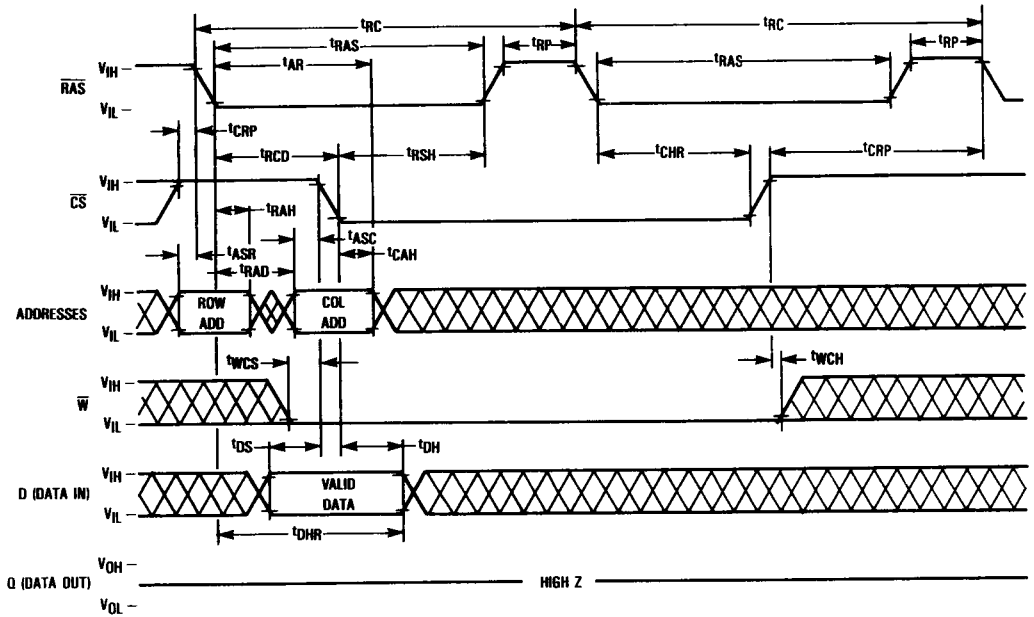
### CS BEFORE RAS REFRESH CYCLE ( $\bar{W}$ and A0 to A9 are Don't Care)



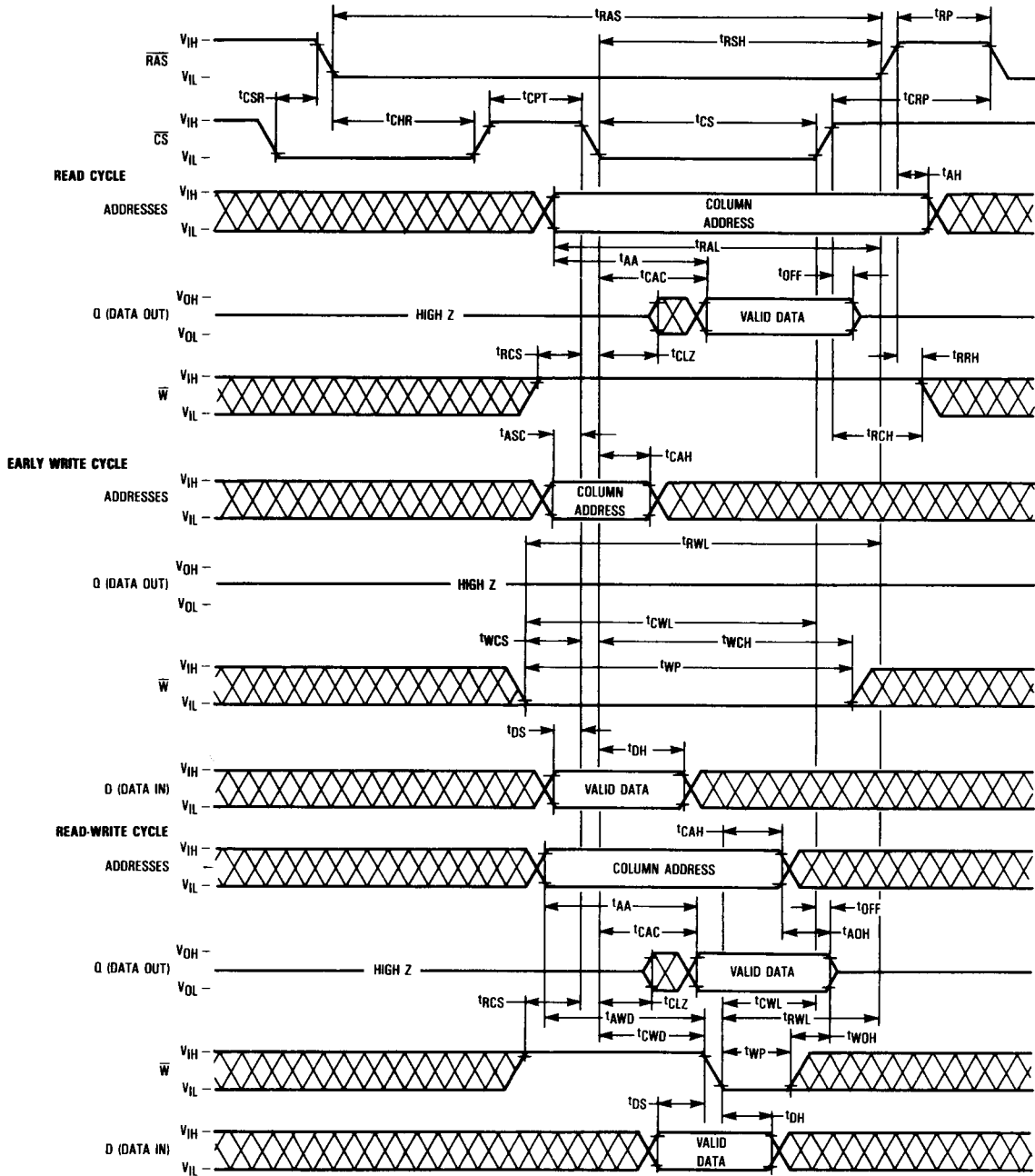
**HIDDEN REFRESH CYCLE (READ)**



**HIDDEN REFRESH CYCLE (EARLY WRITE)**



$\overline{CS}$  BEFORE  $\overline{RAS}$  REFRESH COUNTER TEST CYCLE



2

## DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to assure proper operation.

## ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by the row address strobe ( $\overline{\text{RAS}}$ ) clock, into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device.  $\overline{\text{RAS}}$  active transition latches the row address field. Column addresses are not latched, hence the "static column" designation of this device. Chip select ( $\overline{\text{CS}}$ ) active transition (active =  $V_{IL}$ ,  $t_{RCD}$  minimum) follows  $\overline{\text{RAS}}$  on all read, write, or read-write cycles, and is independent of column address. The static column feature allows greater flexibility in setting up the external external column addresses into the RAM.

There are other variations in addressing the 1M RAM:  $\overline{\text{RAS}}$  only refresh cycle and  $\overline{\text{CS}}$  before  $\overline{\text{RAS}}$  refresh cycle. Both are discussed in separate sections that follow.

## READ CYCLE

The DRAM can be read with four different cycles: random read cycle, read-write cycle, and "static column mode" read, and read-write. The random read cycle is outlined here, while the other cycles are discussed in separate sections.

The random read cycle begins as described in ADDRESSING THE RAM, with  $\overline{\text{RAS}}$  active transition latching the desired row. The write ( $\overline{\text{W}}$ ) input level must be high ( $V_{IH}$ ).  $t_{RCS}$  (minimum) before the  $\overline{\text{CS}}$  active transition, to enable read mode. A valid column address can be provided at any time ( $t_{RAD}$  minimum), independent of the  $\overline{\text{CS}}$  active transition.

Both the  $\overline{\text{RAS}}$  and  $\overline{\text{CS}}$  clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window.  $\overline{\text{CS}}$  must be active and column address must be valid by  $t_{RCD}$  and  $t_{RAD}$  maximums, respectively, to guarantee valid data out (Q) at  $t_{RAC}$  (access time from  $\overline{\text{RAS}}$  active transition). If either  $t_{RCD}$  or  $t_{RAD}$  maximum is exceeded, read access time is determined by the  $\overline{\text{CS}}$  clock active transition ( $t_{CAC}$ ) and/or valid column address ( $t_{AA}$ ).

The  $\overline{\text{RAS}}$  and  $\overline{\text{CS}}$  clocks must remain active for a minimum time of  $t_{RAS}$  and  $t_{CS}$ , respectively, to complete the read cycle. The column address must remain valid for  $t_{AH}$  after  $\overline{\text{RAS}}$  inactive transition to complete the read cycle.  $\overline{\text{W}}$  must remain high throughout the cycle, and for time  $t_{RRH}$  or  $t_{RCH}$  after  $\overline{\text{RAS}}$  or  $\overline{\text{CS}}$  inactive transition, respectively, to maintain the data at that bit location. Once  $\overline{\text{RAS}}$  transitions to inactive, it must remain inactive for a minimum time of  $t_{RP}$  to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the  $\overline{\text{CS}}$  clock is active. When the  $\overline{\text{CS}}$  clock transitions to inactive, the output will switch to High Z.

## WRITE CYCLE

The DRAM may be written with any of four cycles: early write, late write and "static column mode" early write, and read-write. Early and late write modes are discussed here, while static column mode write operations are covered in another section.

A write cycle begins as described in ADDRESSING THE RAM. Write mode is enabled by the transition of  $\overline{\text{W}}$  to active ( $V_{IL}$  level). Early and late write modes are distinguished by the active transition of  $\overline{\text{W}}$  with respect to  $\overline{\text{CS}}$  leading edge. Minimum active time  $t_{RAS}$  and  $t_{CS}$ , and precharge time  $t_{RP}$  apply to write mode, as in the read mode.

An early write cycle is characterized by  $\overline{\text{W}}$  active transition at minimum time  $t_{VCS}$  before  $\overline{\text{CS}}$  active transition. Column address set up and hold times ( $t_{ASC}$ ,  $t_{CAH}$ ), and data in (D) set up and hold times ( $t_{DS}$ ,  $t_{DH}$ ) are referenced to  $\overline{\text{CS}}$  in an early write cycle.  $\overline{\text{RAS}}$  and  $\overline{\text{CS}}$  clocks must stay active for  $t_{RWL}$  and  $t_{CWL}$ , respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because  $\overline{\text{W}}$  active transition precedes or coincides with  $\overline{\text{CS}}$  active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when  $\overline{\text{W}}$  active transition is made after  $\overline{\text{CS}}$  active transition.  $\overline{\text{W}}$  active transition could be delayed for almost 10 microseconds after  $\overline{\text{CS}}$  active transition, ( $t_{RCD} + t_{CWD} + t_{RWL} + 2t_T$ )  $\leq t_{RAS}$ , if other timing minimums ( $t_{RCD}$ ,  $t_{RWL}$ , and  $t_T$ ) are maintained. Column address and D timing parameters are referenced to  $\overline{\text{W}}$  active transition in a late write cycle. Output buffers are enabled by  $\overline{\text{CS}}$  active transition but Q may be indeterminate—see note 18 of AC operating conditions table. Parameters  $t_{RWL}$  and  $t_{CWL}$  also apply to late write cycles.

## READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the WRITE CYCLE section, except  $\overline{\text{W}}$  must remain high for  $t_{CWD}$  and/or  $t_{AWD}$  minimum, to guarantee valid Q before writing the bit.

## STATIC COLUMN MODE CYCLES

Static column mode refers to multiple successive data operations performed at any or all 1024 column locations on the selected row of the 1M dynamic RAM during one  $\overline{\text{RAS}}$  cycle. Read access time of multiple operations ( $t_{AA}$  or  $t_{CAC}$ ) is considerably faster than the regular  $\overline{\text{RAS}}$  clock access time  $t_{RAC}$ . Multiple operations can be performed simply by keeping  $\overline{\text{RAS}}$  active.  $\overline{\text{CS}}$  may be toggled between active and inactive states at any time within the  $\overline{\text{RAS}}$  cycle.

Once the timing requirements for the initial read, write, or read-write cycle are met and  $\overline{\text{RAS}}$  remains low, the device is ready for the next operation. Operations can be intermixed in any order, at any column address, subject to normal operating conditions previously described. Every write operation must be clocked with either  $\overline{\text{CS}}$  or  $\overline{\text{W}}$ , as indicated in static column mode early write cycle timing diagrams A and B. Column address and D timing parameters are referenced to the signal

clocking the write operation.  $\overline{CS}$  must be toggled inactive ( $t_{CP}$ ) to perform a read operation after an early write operation (to turn output on), as indicated in **static column mode read/write mixed cycle timing diagram**. The maximum number of consecutive operations is limited by  $t_{RASC}$ . The cycle ends when  $\overline{RAS}$  transitions to inactive.

## REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically refreshed (recharged) to maintain the correct bit state. Bits in the MCM511002A require refresh every 8 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM511002A. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM511002A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other methods of refresh, **RAS only refresh**,  **$\overline{CS}$  before RAS refresh**, and **hidden refresh** are available on this device for greater system flexibility.

### $\overline{RAS}$ -Only Refresh

$\overline{RAS}$ -only refresh consists of  $\overline{RAS}$  transition to active, latching the row address to be refreshed, while  $\overline{CS}$  remains high ( $V_{IH}$ ) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

### $\overline{CS}$ Before $\overline{RAS}$ Refresh

$\overline{CS}$  before  $\overline{RAS}$  refresh is enabled by bringing  $\overline{CS}$  active before  $\overline{RAS}$ . This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

### Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding  $\overline{CS}$  active at the end of a read or write cycle, while  $\overline{RAS}$  cycles inactive for  $t_{RP}$  and back to active, starts the hidden refresh. This is essentially the execution of a  $\overline{CS}$  before  $\overline{RAS}$  refresh from a cycle in progress (see Figure 1).

## $\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a  **$\overline{CS}$  before  $\overline{RAS}$  refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See  **$\overline{CS}$  before  $\overline{RAS}$  refresh counter test cycle timing diagram**.

The test can be performed after a minimum of eight  $\overline{CS}$  before  $\overline{RAS}$  initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the  **$\overline{CS}$  before  $\overline{RAS}$  refresh counter test, read-write cycle**. Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same column address as in step 2, read "1" out and write "0" into the cell by performing the  **$\overline{CS}$  before  $\overline{RAS}$  refresh counter test, read-write cycle**. Repeat this operation 512 times.
5. Read "0"s which were written at in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

## TEST MODE

Internal organization of this device ( $256K \times 4$ ) allows it to be tested as if it were a  $256K \times 1$  DRAM. Only nine of the ten addresses (A0-A8) are used in test mode; A9 is internally disabled. A test mode write cycle writes data, D (data in), to a bit in each of the four  $256K \times 1$  blocks (B0-B3), in parallel. A test mode read cycle reads a bit in each of the four blocks. If data is the same in all four bits, Q (data out) is the same as the data in each bit. If data is not the same in all four bits, Q is high Z. See truth table and block diagram.

Test mode can be used in any timing cycle, including page mode cycles. The test mode function is enabled by holding the "TF" pin on "super voltage" for the specified period ( $t_{TES}$ ,  $t_{TEHR}$ ,  $t_{TEHC}$ ; see TEST MODE CYCLE).

$$\text{"Super voltage"} = V_{CC} + 4.5 V$$

where

$$4.5 V < V_{CC} < 5.5 V \text{ and maximum voltage} = 10.5 V.$$

A9 is ignored in test mode. In normal operation, the "TF" pin must either be connected to  $V_{IL}$ , or left open.

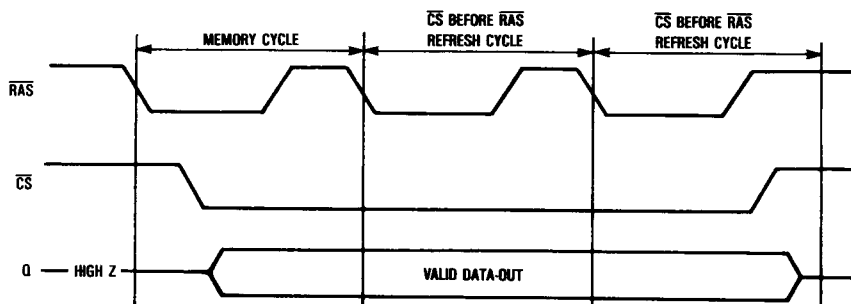
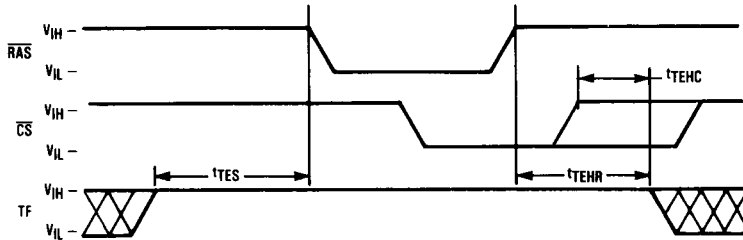


Figure 1. Hidden Refresh Cycle

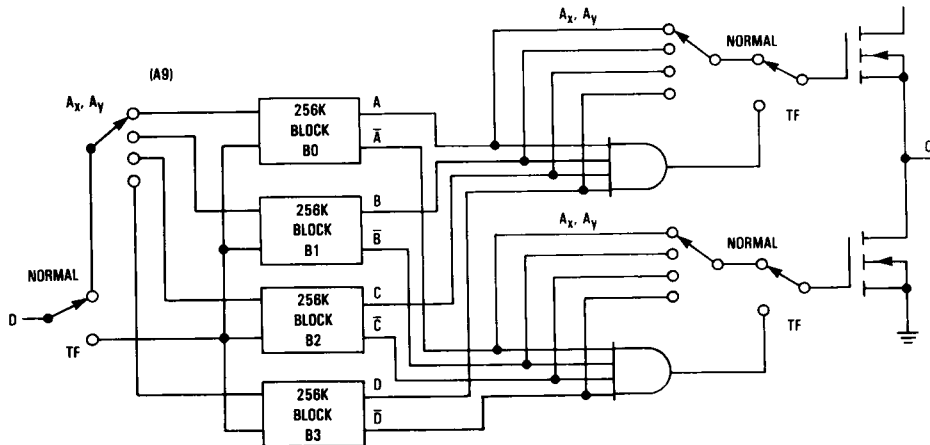
Test Mode Truth Table

D	B0	B1	B2	B3	Q
0	0	0	0	0	0
1	1	1	1	1	1
—	Any Other				High-Z

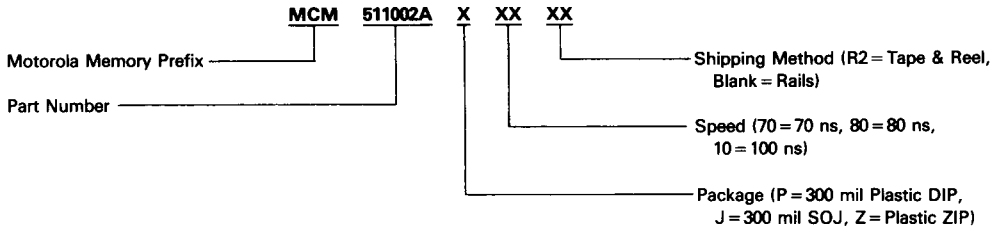
TEST MODE CYCLE



TEST FUNCTION BLOCK DIAGRAM



ORDERING INFORMATION  
(Order by Full Part Number)



Full Part Numbers—MCM511002AP70	MCM511002AJ70	MCM511002AJ70R2	MCM511002AZ70
MCM511002AP80	MCM511002AJ80	MCM511002AJ80R2	MCM511002AZ80
MCM511002AP10	MCM511002AJ10	MCM511002AJ10R2	MCM511002AZ10

NOTE: For mechanical data, please see Chapter 10.