DC to 4 GHz Envelope & TruPwr™ RMS Detector

Preliminary Technical Data

ADL5511

FEATURES

- Envelope Tracking RF Detector
- Separate TruPwr™ RMS Detector
- Excellent temperature stability
- ±0.25 dB envelope detection accuracy vs. temperature
- ±0.25 dB RMS detection accuracy vs. temperature over the top 20 dB of the input range
- Input power dynamic range of 40 dB
- Input frequency range from DC to 4 GHz
- 100 MHz envelope bandwidth
- Envelope delay <5 nS
- Single-supply operation: 4.75 V to 5.25 V

APPLICATIONS

- RMS power and envelope detection of W-CDMA, CDMA2000, LTE, and other complex waveforms
- Drain modulation based power amplifier linearization
- Power amplifier linearization employing envelope-tracking methods

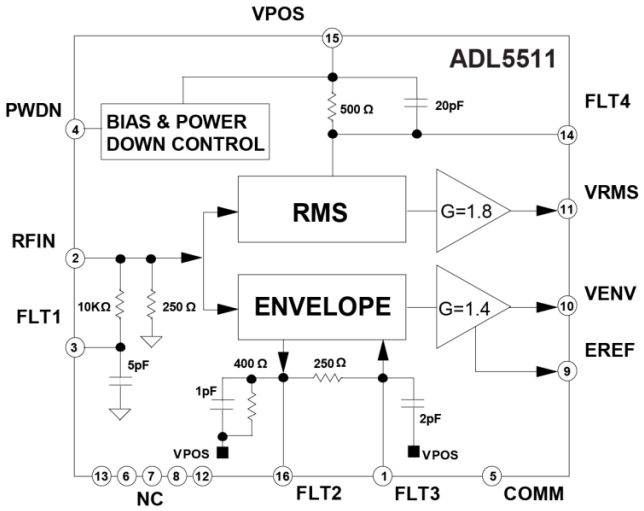

Figure 1. ADL5511 Block Diagram

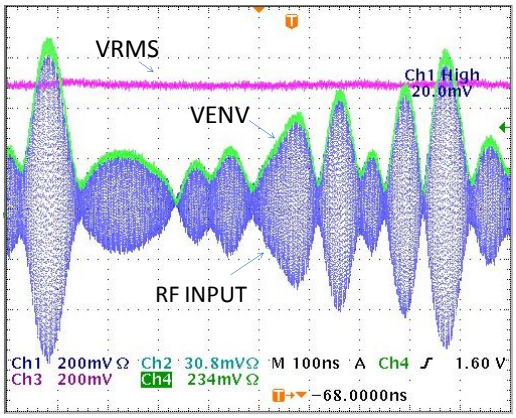

Figure 2. RMS and Envelope Response to a 20 MHz QPSK-based LTE Carrier (Test Model E-TM1_1_20MHz)

GENERAL DESCRIPTION

ADL5511 is an RF Envelope and TruPwr RMS Detector. The envelope output voltage is presented as a voltage that is proportional to the envelope of the input signal. The RMS output voltage is independent of the peak-to-average ratio of the input signal.

The RMS output is a linear-in-V/V voltage with a conversion gain of 1.8 V/V rms at 900 MHz. The envelope output has a conversion gain of 1.4 V/V and is referenced to an internal 1.1 V reference voltage, which is available on the EREF pin.

ADL5511 can operate from DC to 4 GHz on signals with envelope bandwidths up to 100 MHz.

The extracted envelope can be used for PA linearization and efficiency enhancements and the RMS output can be used for true power measurement. The high rms accuracy and fast envelope response are particularly useful for envelope detection and power measurement of broadband, high peak-to-average signals that are used in CDMA2000, W-CDMA and LTE systems.

The ADL5511 operates from −40°C to +125°C and is available in a 16-lead 3mm x 3mm LFCSP package.

Rev. PrD

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

SPECIFICATIONS

T_A = 25°C, V_{POS} = 5 V, C_{FLT4} = 100 nF, 75 Ω shunt termination resistor to ground on (ac-coupled) RFIN, unless otherwise noted.

Table 1.

Parameter	Condition	Min	Typ	Max	Unit
FREQUENCY RANGE	Input RFIN	DC		4000	MHz
RF Input (f = 900 MHz)	Input RFIN to output VRMS and VENV				
RMS CONVERSION	Input RFIN to output VRMS				
Input Range (±1 dB Error)	CW input, −40°C < T_A < +85°C		40		dB
Maximum Input Level	±1 dB error		15		dBm
Minimum Input Level	±1 dB error		-25		dBm
Conversion Gain	V_{RMS} = (Gain × V_{IN}) + Intercept		1.8		V/V rms
Intercept			11		mV
Output Voltage—High Power In	P_{IN} = +10 dBm, 707 mV rms		1.3		V
Output Voltage—Low Power In	P_{IN} = −20 dBm, 22.4 mV rms		50		mV
ENVELOPE CONVERSION	Input RFIN to output (VENV-EREF)				
Input Range (±1 dB Error)	V_S = 5 V		40		dB
Maximum Input Level	±1 dB error		+15		dBm
Minimum Input Level	±1 dB error		-25		dBm
Conversion Gain	CW Input, V_{ENV} = (Gain × V_{IN}) + Intercept		1.4		V/V rms
Intercept			-5		mV
Output Voltage - High Power In	P_{IN} = +10 dBm, 707 mV rms		1		V
Output Voltage - Low Power In	P_{IN} = −20 dBm, 22.4 mV rms		30		mV
Envelope Modulation 3 dB Bandwidth			100		MHz
Envelope Delay	RFIN to VENV		<5		nS
Output Current Drive	Load = 500Ω||10 pF		10		mA
RF Input (f = 1900 MHz)	Input RFIN to output VRMS and VENV				
RMS CONVERSION	Input RFIN to output VRMS				
Input Range (±1 dB Error)	CW input, −40°C < T_A < +85°C		40		dB
Maximum Input Level	±1 dB error		15		dBm
Minimum Input Level	±1 dB error		-25		dBm
Conversion Gain	V_{RMS} = (Gain × V_{IN}) + Intercept		1.9		V/V rms
Intercept			14		mV
Output Voltage—High Power In	P_{IN} = +10 dBm, 707 mV rms		1.3		V
Output Voltage—Low Power In	P_{IN} = −20 dBm, 22.4 mV rms		50		mV
ENVELOPE CONVERSION	Input RFIN to output (VENV-EREF)				
Input Range (±1 dB Error)	V_S = 5 V		40		dB
Maximum Input Level	±1 dB error		+15		dBm
Minimum Input Level	±1 dB error		-25		dBm
Conversion Gain	CW Input, V_{ENV} = (Gain × V_{IN}) + Intercept		1.5		V/V rms
Intercept			-5		mV
Output Voltage—High Power In	P_{IN} = +10 dBm, 707 mV rms		1		V
Output Voltage—Low Power In	P_{IN} = −20 dBm, 22.4 mV rms		25		mV
Envelope Modulation 3 dB Bandwidth			100		MHz
Envelope Delay	RFIN to VENV		<5		nS
Output Current Drive	Load = 500Ω||10 pF		10		mA

Parameter	Condition	Min	Typ	Max	Unit
SHUTDOWN INTERFACE[1]	Pin PWDN				
Logic Level to Enable Power, LOW Condition	4.5 V ≤ V_S ≤ 5.5 V	0		4	V
Logic Level to Disable Power, HI Condition	4.5 V ≤ V_S ≤ 5.5 V	4.9			V
POWER SUPPLIES					
Operating Range	−40°C < T_A < +125°C	4.5		5.5	V
Quiescent Current	RFIN < -10 dBm		25		mA
	RFIN = +15 dBm		50		mA

[1] On pre-release devices, a high on PWDN will disable the device. On the final production version of the ADL5511, a HIGH on this pin will enable the device.

Table 2. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 16	FLT3, FLT2	External Envelope Filter: With pins FLT3 and FLT3 not connected, two internal 320 MHz and 400 MHz low-pass filters (operating in series) remove the RF carrier from the envelope signal. External capacitors (supply-referenced) connected to FLT3 and FLT2 can be used to reduce this corner frequency. See section entitled FLT3 and FLT2 and Envelope Filtering for more information. On pre-release devices, the internal capacitances on FLT3 and FLT2 have values of 1pF and 2pF respectively. On the final production version of the ADL5511, these values will reduce to 0.4pF and 0.8pF respectively. This will increase the default corner frequency to approximately 800 MHz
2	RFIN	RF Input: RFIN should be externally ac-coupled. RFIN has a nominal input impedance of 250 Ω. To achieve a broadband 50 Ω input impedance, an external 75 Ω shunt resistor should be connected between the ac-coupling capacitor and ground .
3	FLT1	A capacitor to ground on this pin can be used to reduce the minimum input frequency below the nominal minimum of 700 MHz. The capacitance on this pin helps to reduce any residual RF carrier presence on the EREF output pin.
4	PWDN	Device Enable/Disable: For pre-release devices, connect pin to ground for normal operation. Connect to VPOS to disable the device. If PWDN is left floating, the device will be enabled. On the production version of the ADL5511, this pin will be renamed to ENBL which should be tied high (or left floating) to enable the device.
5	COMM	Device Ground: Connect to a low impedance ground plane.
6,7,8,12,13	NC	No Connect.
9	EREF	Reference voltage for envelope output: Nominal value is 1.1 V.
10	VENV	Envelope Output: The voltage on this pin represents the envelope of the input signal and is referred to EREF. ENVO can source a current of up to 10 mA. Resistive loads on ENVO should not be less than 500 Ω and capacitive loading should not exceed 10 pF to achieve the specified envelope bandwidth. Lighter loads should be chosen when possible.
11	VRMS	RMS Output Pin: This voltage is ground reference and has a nominal swing of 0V to 4V. VRMS has a linear-in-V/V transfer function with a nominal slope of 3V/V.
14	FLT4	RMS Averaging Capacitor.: Connect between FLT4 and VPOS
15	VPOS	Supply Voltage Pin: Operational range is 4.5 V to 5.5 V with a supply current of 25 mA.

TYPICAL PERFORMANCE CHARACTERISTICS

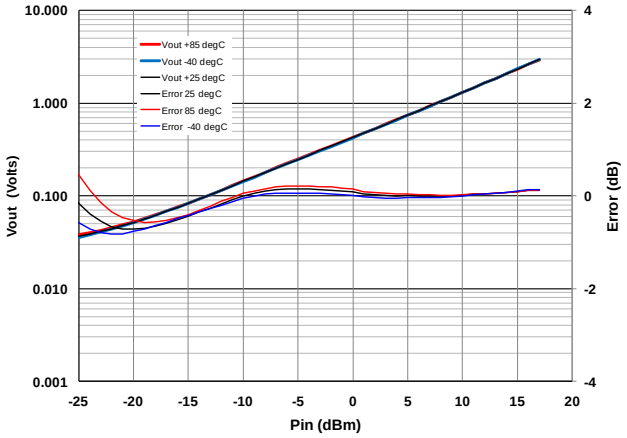

Figure 3. VRMS Output Voltage and Linearity Error vs. Input Power and Temperature at 900 MHz

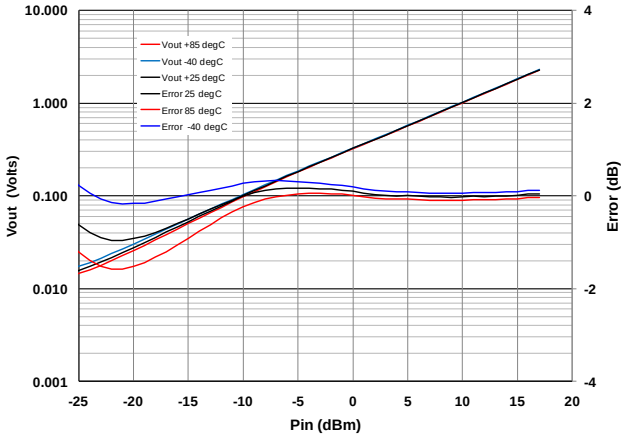

Figure 6. VENV Output Voltage and Linearity Error vs. Input Power and Temperature at 900 MHz

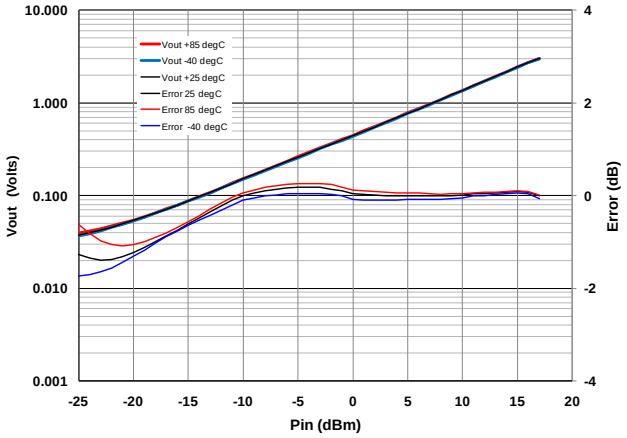

Figure4. VRMS Output Voltage and Linearity Error vs. Input Power and Temperature at 1900 MHz

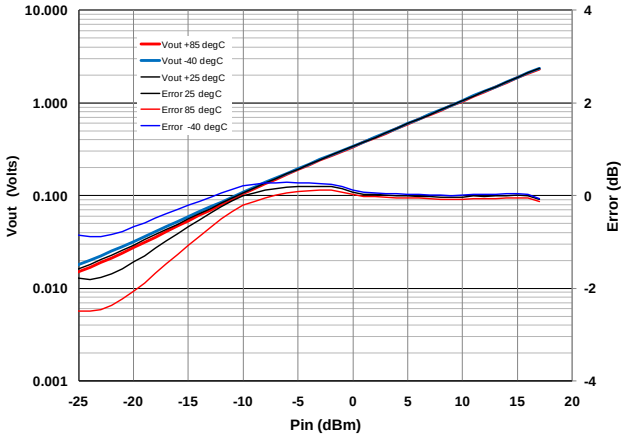

Figure 7. VENV Output Voltage and Linearity Error vs. Input Power and Temperature at 1900 MHz

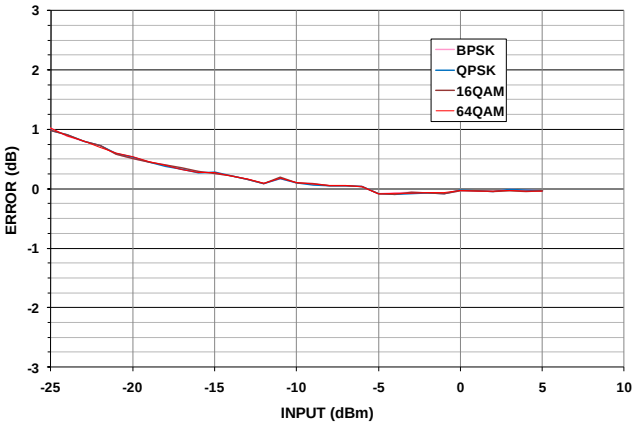

Figure 5. Deviation of VRMS Output with respect to CW response for Various OFDM-based Carriers at 2.35 GHz

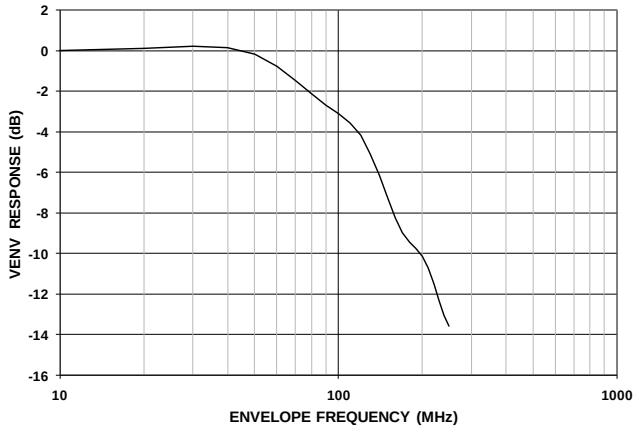

Figure 8. Bandwidth of Envelope Output

BASIC CONNECTIONS

The ADL5511 requires a single supply of 5 V. The supply is connected to the VPOS supply pin. This pin should be decoupled using two capacitors with values equal or similar to those shown in Figure 9. These capacitors should be as close as possible to the VPOS pin.

An external 75 Ω resistor combines with the relatively high RF input impedance of the ADL5511 to provide a broadband 50 Ω match. An ac coupling capacitor should be placed between this resistor and RFIN.

The RMS output voltage is available at the VRMS pin with rms averaging provided by the capacitance on Pin 14 (FLT4). The envelope output is available on Pin 10 VENV and is referenced to the 1.1 V dc voltage on Pin 9 (EREF).

The schematic shown in Figure 9 also represents the basic connections on the Customer Evaluation Board, with additional unpopulated devices omitted for clarity.

FLT3 AND FLT2 AND ENVELOPE FILTERING

With pins FLT3 and FLT3 not connected, two internal 320 MHz and 400 MHz low-pass filters (operating in series) remove the RF carrier from the envelope signal.

So without any external capacitance, the envelope signal sees two filters with corner frequencies of

$$\frac{1}{(2\pi \times 1pF \times 400\,\Omega)} \cong 400\ MHz$$

and

$$\frac{1}{(2\pi \times 2pF \times 250\,\Omega)} \cong 320\ MHz$$

This corner frequency of this filtering can be reduced (e.g. if the RF carrier is less than 400 MHz) by connecting supply referenced capacitors to FLT3 and FLT2. The corner frequencies are then set according to the equations

$$\frac{1}{(2\pi \times (1pF + C_{FLT2}) \times 400\Omega)} = F_{FLT2}$$

and

$$\frac{1}{(2\pi \times (2pF + C_{FLT3}) \times 250\Omega)} = F_{FLT3}$$

These two corner frequencies should be set so that they are approximately equal.

Care should be taken not to make the corner frequency too low. The ADL5511 has an envelope bandwidth of 100 MHz. So if the capacitors on FLT2 and FLT3 are so big that the corner freq goes below 100 MHz, this now sets the envelope bw. So the corner frequency should be set low enough so that the RF carrier is removed without reducing the envelope bandwidth below the desired frequency.

On pre-release devices, the internal capacitances on FLT3 and FLT2 have values of 1pF and 2pF respectively. On the final production version of the ADL5511, these values will reduce to 0.4pF and 0.8pF respectively. This will set the default corner frequency to approximately 800 MHz.

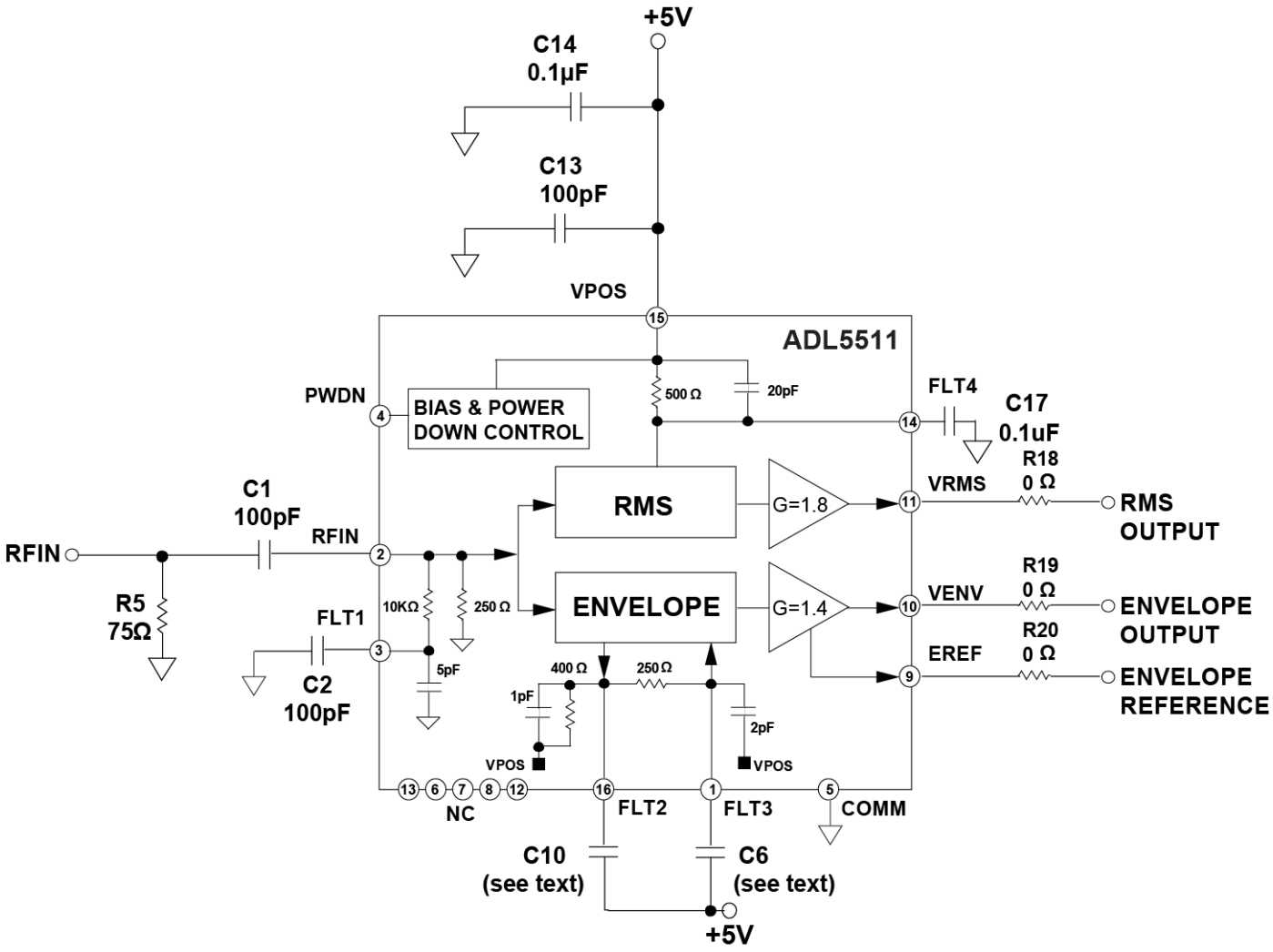

Figure 9. ADL5511 Basic Connections and Customer Evaluation Board Schematic

OUTLINE DIMENSIONS

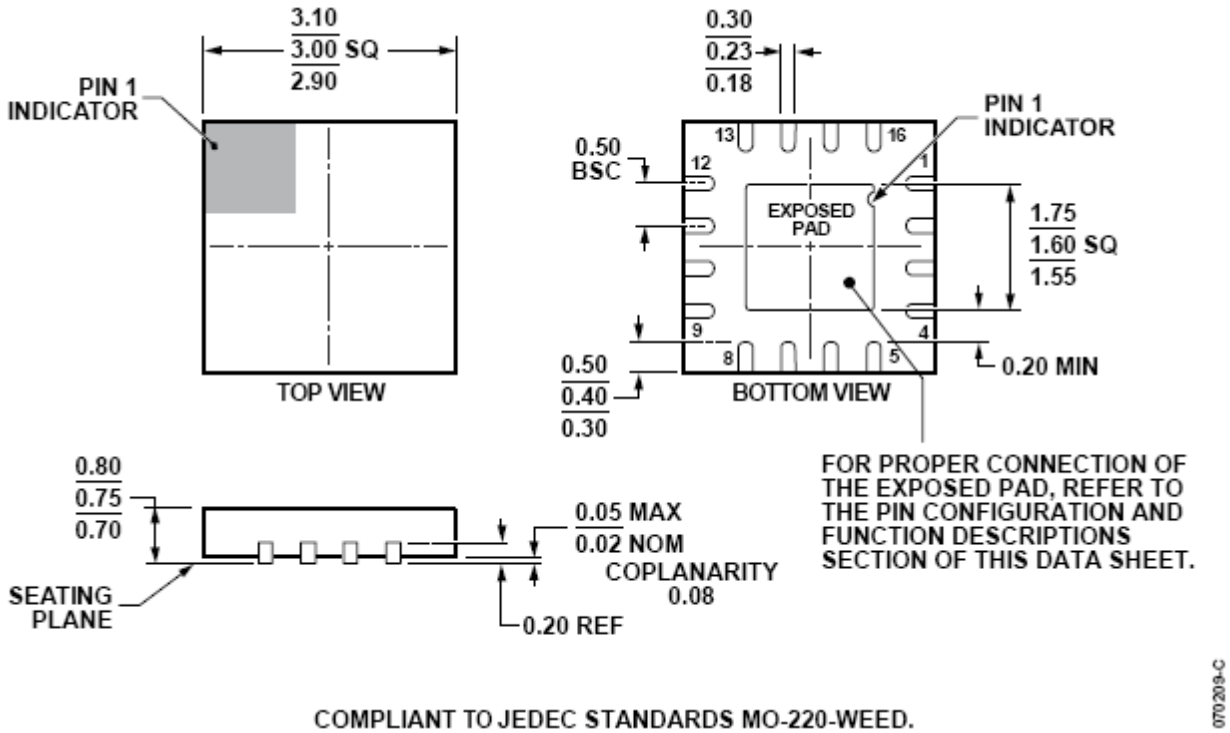

Figure 10. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm x 3 mm Body, Very Thin Quad
(CP-16-22)
Dimensions shown in mm

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5511ACPZ	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package		
ADL5511-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

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