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INNOVATORS IN INTEGRATION

953537

SSI 6070
10-Bit µP Compatible A-to-D Converter

86 orig

Data Sheet

006653

GENERAL DESCRIPTION

Silicon Systems' new SSI 6070 range of successive approximation A to D converters combine several innovations to provide this function in a fully monolithic silicon device. The device consists of a current switching array which requires no trim, successive approximation logic, a 2.5V precision voltage reference, a reference amp, comparator and 3-state output buffers. $\overline{\text{BYTE 1}}$ and $\overline{\text{BYTE 2}}$ inputs control the 10-bit output word format. This can be read as either a 10-bit output word or as an 8-bit and a 2-bit word.

FEATURES

6653 SSI

- **Linearity: ½ LSB or 1 LSB**
- **3-state outputs, TTL compatible**
- **Conversion time 15 µsec typical, 20 µsec guaranteed**
- **Input range as desired**
- **Asynchronous $\overline{\text{START CONVERT}}$ input**
- **+5V, -5V supplies, µP and TTL/CMOS compatible**
- **Commercial or military temperature ranges**
- **Full 8- or 16-bit MICRO-bus interface**
- **Ceramic or plastic packages**

CIRCUIT OPERATION

These devices use the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{\text{SC}}$ input, the STATUS line goes low, and the DAC input is sent to the MSB. The resulting analog output is compared with the unknown analog input signal by the comparator. If the analog input is larger, the MSB is left in the circuit; if not, it is removed. On the second clock pulse this sequence is repeated for the next most significant bit and so on, until all 10 bits have been compared. On the 11th negative clock edge STATUS goes high, indicating the conversion is complete.

During conversion, $\overline{\text{BYTE 1}}$ and $\overline{\text{BYTE 2}}$ inputs should normally be kept high to keep the 3-state buffers in their high Z state. Data can be read out by taking either $\overline{\text{BYTE 1}}$ or $\overline{\text{BYTE 2}}$ low, thus enabling the 3-state outputs. $\overline{\text{BYTE 1}}$ controls the 8 most significant bits, and $\overline{\text{BYTE 2}}$ controls the 2 least significant bits.

CONVERSION TIMING

The SSI 6070 accepts a low-going $\overline{\text{SC}}$ pulse which can be asynchronous to the clock. It will produce valid data between 10.5 and 11.5 clock pulses later, depending on the relative timing of the CLOCK and $\overline{\text{SC}}$ signals.

The SSI 6070 is cleared by a low-going $\overline{\text{SC}}$ pulse, which sets the MSB and resets all the other bits and the STATUS line. While the $\overline{\text{SC}}$ input is low, the MSB is continuously compared with the analog input, but otherwise the comparator is inhibited. After $\overline{\text{SC}}$ goes high again, the MSB decision is made, and the successive approximation routine runs to completion.

$\overline{\text{START CONVERT}}$ can be as short as 100 nsec; however, the MSB must be allowed to settle for at least 625 nsec before the MSB decision is made. To assure this criterion is met even with short $\overline{\text{SC}}$ pulses, the converter waits after $\overline{\text{SC}}$ goes high for a rising clock edge followed by the falling edge. The decision is made on the falling edge of the clock. This assures MSB is allowed to settle for at least half a clock period (625nsec) at maximum clock frequency. The clock-high period and the $\overline{\text{SC}}$ pulse width must comply with this settling time: (clock high time + $\overline{\text{SC}}$ ≥ 625 nsec).

During conversion, the $\overline{\text{SC}}$ input is not locked out; if it is pulsed low at any time, the conversion will restart.

At the end of a conversion, STATUS waits one clock cycle before going high to indicate valid data. Data outputs can be enabled anytime during a conversion and valid data will be available on the rising edge of STATUS.

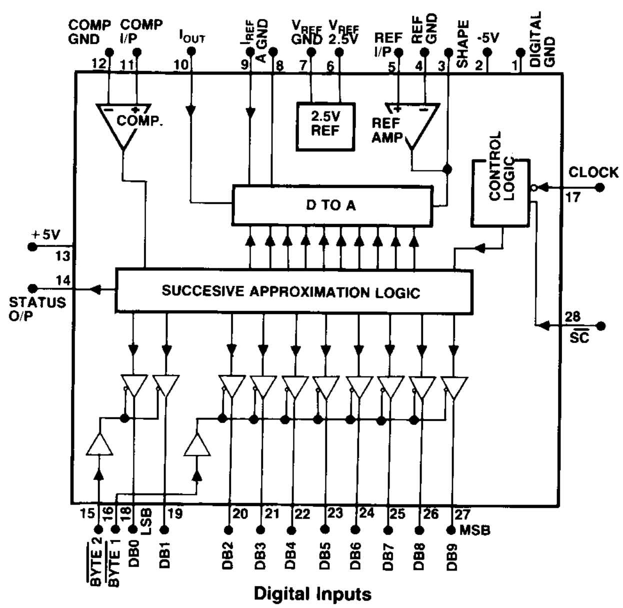


Figure 1 Circuit Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC+} . . . . +7 volts
V_{CC-} . . . . -7 volts
Logic Input Voltage . . . . $+V_{cc}$ and 0 volts
Operating Temperature Range 0 to +70°C 6070 CPE
6070 CDE
-55 to +125°C 6070 MDE
Storage Temperature Range . . . . -55 to +125°C

Ordering Info.	Package	Temp. Range
SSI 6070 CDE	Ceramic 28 Pin Dual In Line	0°C to +70°C
SSI 6070 CPE	Plastic 28 Pin Dual In Line	0°C to +70°C
SSI 6070 MDE	Ceramic 28 Pin Dual In Line	-55°C to +125°C

ELECTRICAL CHARACTERISTICS (at +5 and -5 volts supplies and internal reference unless otherwise stated)

Parameter	Version	T_{amb} = +25°C			Over Spec.		Units	Conditions
		Min.	Typ.	Max.	Min.	Max.		
	6070 MDE							Ceramic
Linearity error				±0.5		±0.5	LSB	
Diff. linearity error				±0.5		±0.5	LSB	Note 1
Unipolar offset			±0.55 ±0.55	±1.0 ±1.0		±1.0 ±1.0	LSB LSB	Ext. Ref. Int. Ref.
Bipolar offset			±0.55 ±0.55	±1.0 ±1.0		±1.0 ±1.0	LSB LSB	Ext. Ref. Int. Ref.
Gain error			±0.55 ±3				LSB LSB	Ext. Ref.* Int. Ref.*
TEMPERATURE COEFFICIENTS (T_{min} to T_{max})								
Unipolar offset			7 typ., 10 max. 7 typ., 10 max.				ppm/°C ppm/°C	Ext. Ref. Int. Ref.
Bipolar offset			7 typ., 10 max. 7 typ., 10 max.				ppm/°C ppm/°C	Ext. Ref. Int. Ref.
Gain			10 typ. 50 typ.				ppm/°C ppm/°C	Ext. Ref. Int. Ref.
	6070 CPE							Ceramic
Linearity error				±1.0		±1.0	LSB	
Diff. linearity error				±0.5		±0.5	LSB	Note 1
Unipolar offset			±0.55 ±0.55	±1.0 ±1.0		±1.0 ±1.0	LSB LSB	Ext. Ref. Int. Ref.
Bipolar offset			±0.55 ±0.55	±1.0 ±1.0		±1.0 ±1.0	LSB LSB	Ext. Ref. Int. Ref.
Gain error			±0.55 ±3				LSB LSB	Ext. Ref.* Int. Ref.*

(continued on page 4) *See Note 4

Table 1
THE FOLLOWING IS A TABLE OF VALUES TO GIVE EXAMPLES OF THE FOLLOWING EQUATIONS:

$V_{IN max}$	$V_{IN min}$	V_{REF}	R1(1)	R2(1)	R3	R4	R5	R6(1)
+2.5	-2.5	2.5	5K	1.25K	5K	2.5K	2.5K	∞
+2.5	-2.5	5*	10K	1.25K	10K	5.0K	2.5K	5.0K
+2.5	0	2.5	5K	1.25K	5K	∞	1.25K	∞
+5.0	0	2.5	5K	1.25K	5K	∞	2.5K	2.5K
+4.0	-2.0	2.5	5K	1.25K	5K	3.75K	3.0K	5.0K
+4.0	-2.0	12*	24K	1.25K	24K	3.75K	3.0K	5.0K
+10	-10	2.5	5K	1.25K	5K	2.5K	10K	3.33K
+10	0	2.5	5K	1.25K	5K	∞	5K	1.66K

Note 1: Nearest preferred value may be used for R1, R2 and R6
Note 2: External reference

For unipolar operation where R4 approaches (∞) and a zero adjustment is required, contact the factory for details.

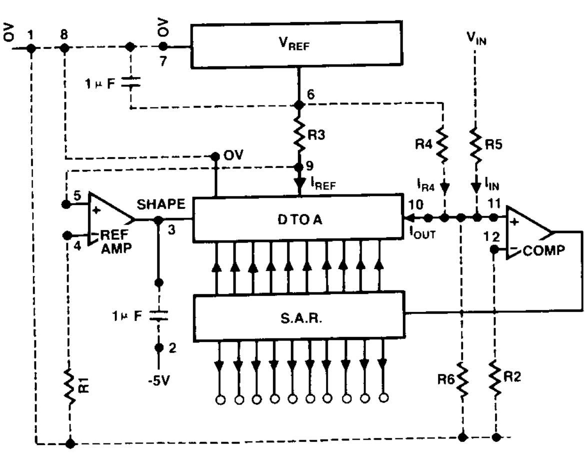


Figure 2 External Component Connections

CONTINUOUS CONVERSION

This converter can be made to cycle by inverting the STATUS output and feeding it back to the $\overline{SC}$ input. To assure the converter starts reliably after power up, an initial start pulse is required. This is done by using a NOR gate and feeding it with a positive going pulse derived from a simple RC timing network that gives a single pulse whenever power is applied. Propogation delay of the NOR gate determines the period over which STATUS remains high, during which time data can be stored in latches. The time available for storing data can be increased by inserting one or more delays in the inverter path.

CALCULATION OF EXTERNAL RESISTORS

V_{IN} max is the voltage for logic output to be all ONEs. V_{IN}min is the voltage for all ZEROs at the output:

$$I_{OUT} = IR4 + I_{IN} = \frac{V_{REF}}{R4} + \frac{V_{IN}}{R5}$$

I_{OUT} = ZERO when $V_{IN} = V_{IN}$ min $\qquad \frac{V_{IN}\ min}{R5} = \frac{-V_{REF}}{R4}$

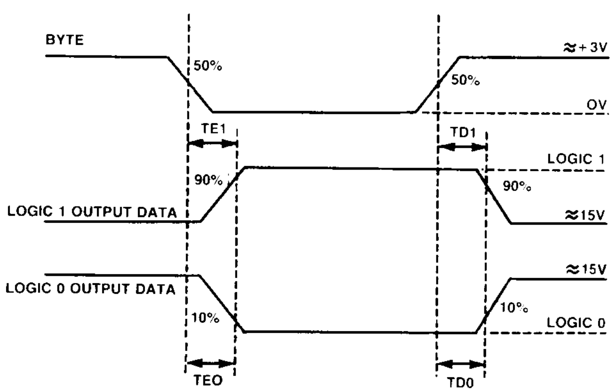
$$R4 = \frac{-V_{REF}\ R5}{V_{IN}\ min}$$

$$I_{OUT}FS = 2mA \text{ when } V_{IN} = V_{IN}\ max$$

$$\frac{V_{IN}\ max}{R5} + \frac{V_{REF}}{R4} = I_{OUT}FS$$

$$\frac{-V_{IN}\ min}{R5} + \frac{V_{IN}\ max}{R5} = I_{OUT}FS$$

$$R5 = \frac{V_{IN}\ max - V_{IN}\ min}{I_{OUT}FS}$$



TE = BYTE ENABLE DELAY TIME (CL = 50pF)
TD = BYTE DISABLE DELAY TIME (CL = 10pF)

Figure 3 Timing Chart

It is important for gain stability that $I_{OUT}FS$ be kept at 2mA constant, and this is done by the reference amplifier loop.

Current sources in the D to A itself cannot be checked directly, so a number of reference current sources are distributed across the chip to monitor conditions all along the array.

$$I_{REF} = 0.5mA \qquad R3 = \frac{V_{REF}}{0.5mA}$$

$$I_{OUT}FS \text{ is 4 times } I_{REF}$$

R3 can affect gain stability and thus must be highly stable; slight variations in the value of R3 can act as a gain control. R4 and R5 can affect offset stability and thus must be highly stable; slight variations in the value of R4 can act as an offset control. R1 and R2 supply the bias currents of the reference amplifier and comparator.

$$R1 = R3;\ R2 = R4//R5//R6$$

R6 should be selected such that the parallel combination of R4, R5 and R6 is about 1.25 K ohms, as this determines the D to A time constant and thus the conversion time.

DATA OUTPUTS

This device has 3-state output buffers on chip, eliminating the need for external buffers and latches.

The two inputs $\overline{BYTE\ 1}$ and $\overline{BYTE\ 2}$ control outputs DB9 through DB2, and outputs DB1 and DB0 respectively. The two inputs will normally be held high during a conversion to keep the 3-state buffers in their high impedance state. When data are ready (indicated by STATUS going high), they are read out by taking $\overline{BYTE\ 1}$ and $\overline{BYTE\ 2}$ low.

A test circuit and timing diagram for the output enable/disable delays are given below; the STATUS output shown uses a 5K ohm internal pullup resistor for CMOS/TTL compatibility.

DATA BUS CONNECTIONS

SSI 6070 can be connected directly to an 8-bit µP bus, where the two LSBs would normally be hardwired to the desired upper bits, usually the two MSBs. Hence, the data would be transferred in two words with control of them from $\overline{BYTE\ 1}$ and $\overline{BYTE\ 2}$.

For use with a 16-bit µP, $\overline{B1}$ and $\overline{B2}$ would be tied together and all 10 bits would be enabled simultaneously. The 10-bit word could then be placed at either the high or low end of the 16-bit bus.

UNIPOLAR ADJUSTMENT PROCEDURE. Apply continuous $\overline{START\ CONVERT}$ pulse at intervals of sufficient duration to allow a complete conversion and monitor the digital outputs.

OFFSET SETTING. Apply ½LSB to V_{IN} and adjust the offset circuit until DB0 (LSB) just flickers between ZERO and ONE with all other bits at ZERO.

GAIN SETTING. Apply full-scale minus 1.5LSB to V_{IN} and adjust gain until LSB just flickers between ZERO and ONE with all other bits at ONE. (Note: R3 gain adjustment)

BIPOLAR ADJUSTMENT PROCEDURE. Apply continuous $\overline{START\ CONVERT}$ pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

OFFSET SETTING. Apply - (FS-½LSB) to V_{IN} and adjust offset control until DBO (LSB) output just flickers between ZERO and ONE with all other bits at ZERO. (Note: R4 offset adjustment)

GAIN SETTING. Apply +(FS-1.5LSB) to V_{IN} and adjust gain until DBO (LSB) just flickers between ZERO and ONE with all other bits at ZERO. (Note: R3 gain adjustment)

BYTE								
1	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2
2	DB1	DB0	X	X	X	X	X	X
	D7	D6	D5	D4	D3	D2	D1	D0

DATA TRANSFERRED IN TWO WORDS

Figure 4 Data Bus Connections

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14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

Table 4
Unipolar Logic Coding

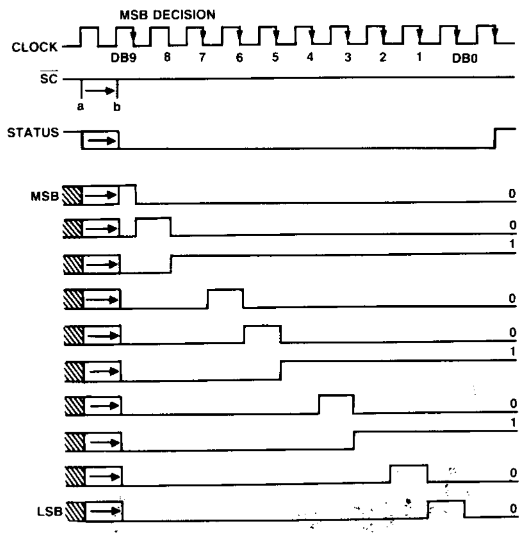
Analog Input (Nominal Code Center Value)	Digital Output Code MSB LSB
FS - 1LSB	1111111111
FS - 2LSB	1111111110
¾ FS	1100000000
½ + LSB	1000000001
½ FS	1000000000
½ FS - 1LSB	0111111111
¼ FS	0100000000
1LSB	0000000001
0	0000000000

$1\ LSB = \frac{FS}{1024}$

Bipolar Logic Coding

Analog Input (Nominal Code Center Value)	Digital Output Code MSB LSB
+(FS - 1LSB)	1111111111
+(FS - 2LSB)	1111111110
+(½ FS)	1100000000
+(1LSB)	1000000001
0	1000000000
-(1LSB)	0111111111
-(½ FS)	0100000000
-(FS - 1LSB)	0000000001
-FS	0000000000

$1\ LSB = \frac{2FS}{1024}$

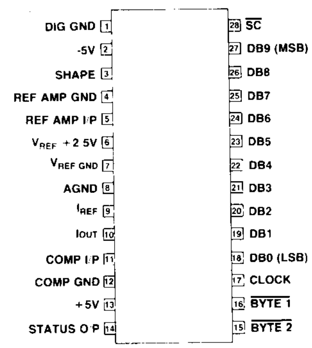


DON'T CARE MIN SC PULSE WIDTH 100nS NO MAX LIMIT

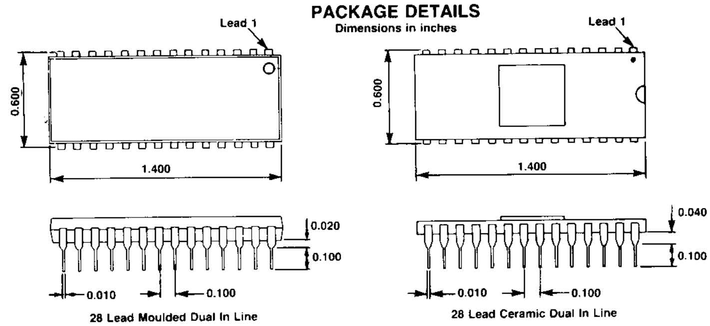
Note: Guaranteed period of ½ clock cycle min. 1½ clock cycles max. Allows MSB to settle before MSB decision

Figure 5 Timing Chart

PIN CONNECTIONS



PACKAGE DETAILS
Dimensions in inches



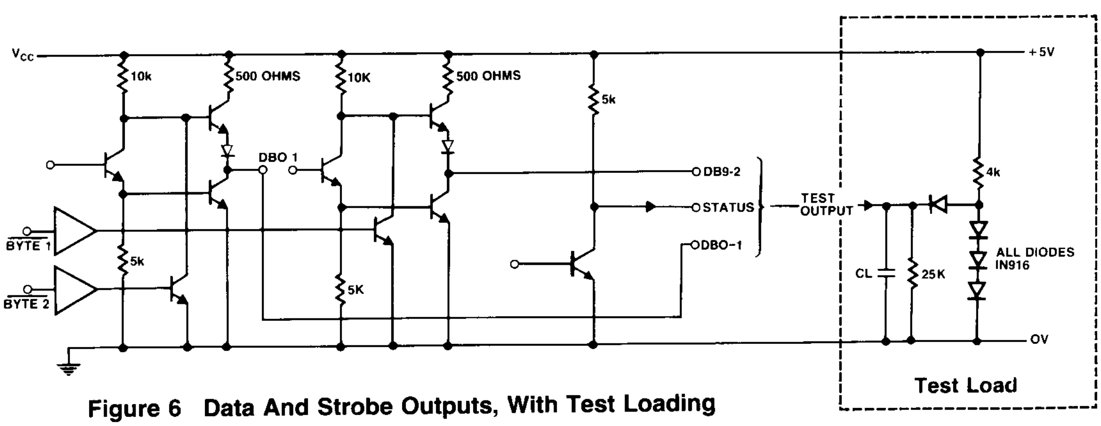


Figure 6 Data And Strobe Outputs, With Test Loading

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ELECTRICAL CHARACTERISTICS (continued)

Parameter	Version	$T_{amb} = +25°C$ Min.	Typ.	Max.	Over Spec Min.	Max.	Units	Conditions
LOGIC	All types							
$\overline{BYTE}$ 1 and 2								
High level input voltage V_{IH}		2.0	-	-	2.0	-	volts	
Low level input voltage V_{IL}		-	-	0.8	-	0.8	volts	
High level input current I_{IN}		-	18.0	-	-	-	μA	$V_{CC} = \pm 5.5V$ $V_{IN} = 5.5V$
High level input current I_{IH}		-	12.0	-	-	-	μA	$V_{CC} = \pm 5.5V$ $V_{IN} = 2.4V$
Low level input current I_{IL}		-	2.0	-	-	-	μA	$V_{CC} = \pm 5.5V$ $V_{IN} = 0.4V$
CLOCK	All types							
CLOCK high period		0.5	-	-	-	-	μS	
Max. clock frequency		550	730	1100	550	730	KHz	
High level input voltage V_{IH}		2.0	-	-	2.0	-	volts	
Low level input voltage V_{IL}		-	-	0.8	-	0.8	volts	
High level input current I_{IN}		-	15.0	-	-	-	μA	$V_{CC} = \pm 5.5V$ $V_{In} = 5.5V$
High level input current I_{IH}		-	5.0	-	-	-	μA	$V_{CC} = \pm 5.5V$ $V_{IN} = 2.4V$
Low level input current I_{IL}		-	1.5	-	-	-	μA	$V_{CC} = \pm 5.5V$ $V_{IN} = 0.4V$
High level output voltage V_{OH}	All types	2.4	-	-	2.4	-	volts	$V_{CC} = \pm 5V$
Low level output voltage V_{OL}		-	-	0.4	-	0.4	volts	
High level output current I_{OH}		-	-	-700	-	-	μA	
Low level output current I_{OL}		-	-	2.0	-	-	mA	
Three-state DISABLE output leakage		-	-	±2.0	-	-	μA	$V_{OUT} = 1.3V$
$\overline{BYTE}$ input to data output delays		-	200	260	-	-	ns	
ENABLE/DISABLE								
Delay time TE1		100	220	260	-	-	ns	Note 6
TE0		60	80	100	-	-	ns	Note 6
TD1		100	120	140	-	-	ns	Note 6
TD0		30	60	100	-	-	ns	Note 6
$\overline{SC}$ pulse width		100	-	-	-	-	ns	
$\overline{SC}$ input to STATUS		-	180	-	-	-	ns	

Note 1: No missing codes over full temperature range at appropriate accuracy.
Note 2: The maximum conversion time is 20 μS. This corresponds to a clock rate of 550KHz based on 11 clock periods per conversion cycle (see timing diagram). This provides an update rate of 45KHz.
Note 3: Single polarity and other input ranges may be provided by different input resistor values.
Note 4: Gain error is trimmable to zero with the aid of R3.
Note 5: The full scale D to A output current $I_{OUT} = 4$ times I_{REF}. For optimum performance $I_{REF} = 0.5mA$.
Note 6: Output loaded as shown in Figure 6.

Table 3

Unipolar Setting-Up Points

Input Range +FS	½ LSB	F S -1 ½LSB
+2.5V	1.22mV	2.4963V
+5.0V	2.441mV	4.9926V

Bipolar Setting-Up Points

Input Range ±FS	- FS-½ LSB	+ F S -1 ½ LSB
±2.5V	-2.4976V	+2.4927V
±5.0V	-4.9951V	+4.9854V

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Version	$T_{amb} = +25°C$ Min.	Typ.	Max.	Over Spec. Min.	Max.	Units	Conditions
TEMPERATURE COEFFICIENTS	6070 CPE							
(T_{min} to T_{max}) Unipolar offset		15 typ., 20 max.					ppm/°C	Ext. Ref.
		15 typ., 20 max.					ppm/°C	Int. Ref.
Bipolar offset		15 typ., 20 max.					ppm/°C	Ext. Ref.
		15 typ., 20 max.					ppm/°C	Int. Ref.
Gain		20 typ.					ppm/°C	Ext. Ref.*
		50 typ.					ppm/°C	Int. Ref.*
Resolution	All types	10	-	-	-	-	bits	
Conversion time (min.)		10	15	20	15	20	μS	Note 2
DAC reference I_{REF}		0.25	0.5	1.0	0.25	1.0	mA	Note 5
Nominal analog input range		-2.5	-	+2.5	-	-	volts	Note 3
Supply rejection		-	0.1	-	-	-	% per V	
Supply voltage $+V_{CC}$		+4.5	+5	+5.5	+4.5	+5.5	volts	
$-V_{CC}$		-4.5	-5	-5.5	-4.5	-5.5	volts	
Supply current $+I_{CC}$		-	30	40	-	-	mA	$+V_{CC}+5V$
$-I_{CC}$		-	21	28	-	-	mA	$-V_{CC}$-5V
Power consumption		-	300	360	-	-	mW	
INTERNAL VOLTAGE REFERENCE								
Output voltage	All types	-	2.480	-	-	-	volts	
Output voltage TOLERANCE	6070 MDE	-	-	±3.0	-	-	%	Ceramic
	6070 CPE	-	-	±5.0	-	-	%	Plastic
V_{REF} temp. coeff.	All types	-	-	-	26	50	ppm/°C	
Slope impedance		-	0.75	-	-	-	ohms	
Max. load current		-	±2.0	-	-	-	mA	
LOGIC **START CONVERT**	All types							
High level input voltage V_{IH}		2.0	-	-	2.0	-	volts	
Low level input voltage V_{IL}		-	-	0.8	-	0.8	volts	
High level input current I_{IH}		-	18.0	-	-	-	μA	V_{CC}±5.5V V_{IN}=5.5V
High level input current I_{IH}		-	8.0	-	-	-	μA	V_{CC}±5.5V V_{IN}=2.4V
Low level input current I_{IL}			4.0	-	-	-	μA	V_{CC}±5.5V V_{IN}+0.4V

(continued on page 5) *See Note 4

Table 2

Logic **Start Convert**	**All types**							
High level input voltage V_{IH}		2.0	-	-	2.0	-	volts	
Low level input voltage V_{IL}		-	-	0.8	-	0.8	volts	
High level input current I_{IH}		-	18.0	-	-	-	μA	V_{CC}= ±5.5V I_{IN}=5.5V
High level input current I_{IH}		-	8.0	-	-	-	μA	V_{CC}±5.5V V_{IN}=2.4V
Low level input current I_{IL}		-	4.0	-	-	-	μA	V_{CC}±5.5V V_{IN}+0.4V