DS3132-1 0

MS2002

DIGITAL SWITCH MODULE (DSM)

The MS2002 is an N-channel MOS LSI integrated circuit providing digital switching for 256 channels in PCM systems. The device is unidirectional in operation and is capable of switching data from any incoming channel to any outgoing channel. Input data can be either serial or parallel. The DSM is designed to be easily expandable to provide a greater switching capacity.

FEATURES

- Single 5V Supply
- TTL Compatible
- Interfaces Directly with European Standard CCITT 32 Channel Format
- 256 Input/256 Output Channels
- Serial or Parallel Inputs and Outputs
- Open Drain Outputs for Easy Expansion
- One System Clock and One Frame Synchronisation Pulse

APPLICATION

- Circuit Switched PCM or Data Systems

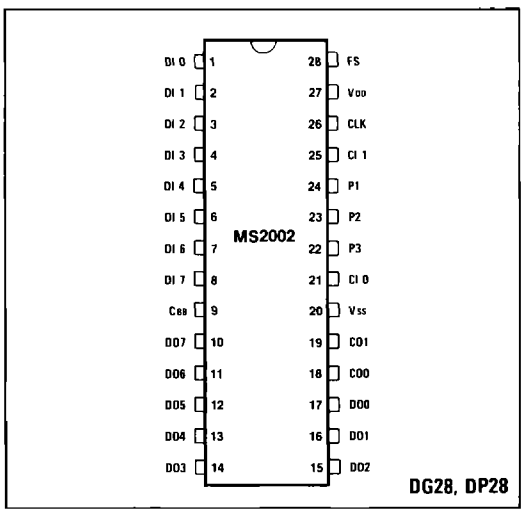


Fig.1 Pin connections - top view

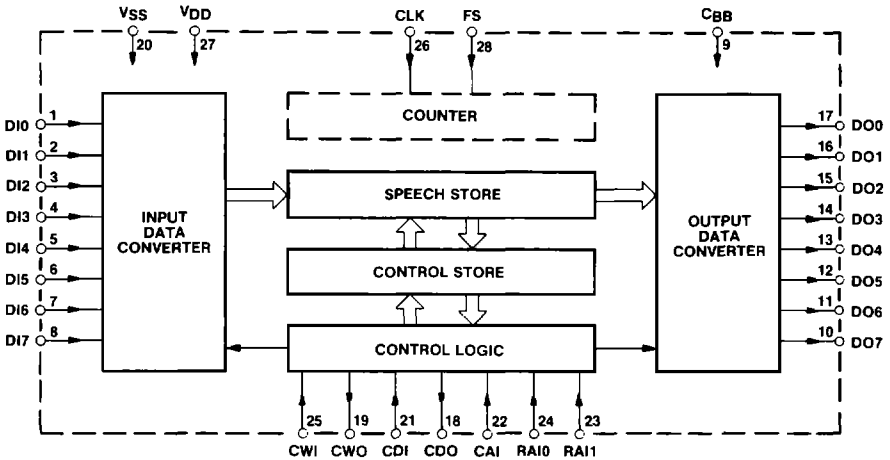


Fig.2 Functional block diagram

PIN DESCRIPTIONS

Symbol	Pin No.	Pin name and description
DI0-DI7	1-8	**Data In 0 to 7 (Digital Inputs).** These are the inputs for the 256 incoming channels. The data presented at these pins is latched on the alternate negative edges of the CLK clock to those used by DO0-7. Frame synchronisation for these pins is established by the FS pulse.
C_{BB}	9	**Bias Decoupling Capacitor (Decoupling Node).** A bias decoupling capacitor of 1000pF should be connected between this pin and V_{SS}.
DO7-DO0	10-17	**Data Out 0 to 7 (Digital Pull-down Outputs).** These are the output pins for the 256 outgoing channels. Data is output at these pins on the alternate negative edges of the CLK clock to those used by DI0-7. Frame synchronisation for these pins is established by the FS pulse.
CDO	18	**Control Data Out (Digital Pull-down Output).** This pin outputs control data bytes. Bit synchronisation and frame synchronisation are stablished by the CLK and FS signal in a similar way as on the DO0-7 pins. It is high impedance for time slots which are not in use for control instructions. It is also high impedance for time slots corresponding to the 'write all ones' instruction. During time slots corresponding to other control instructions this pin outputs either the inverse of the 8 least significant bits at a control store location or the data at the speech store location selected by these 8 bits
CWO	19	**Control Word Out (Digital Pull-down Output).** This pin outputs control word bytes. Bit synchronisation and frame synchronisation are established by the CLK and FS signals in a similar way as on the DO0-7 pins. It is high impedance for time slots which are not in use for control instructions and for time slots corresponding to the instruction 'write all ones'. During time slots corresponding to other instructions this pin outputs 4 bits which are the same as on CWI and 4 bits which indicate to the status of the chip.
V_{SS}	20	**Negative Supply Voltage (Power Input).** 0V
CDI	21	**Control Data In (Digital Input).** The control data bytes are latched into the chip at this pin. Bit synchronisation and frame synchronisation are established by the CLK and FS signals in a similar way as on the DI0-7 pins. The bits in the input control data byte are inverted and written into the control store by the instruction 'write CWM bit and CI bits'.
CAI	22	**Column Address In (Digital Input).** This pin defines the column position of a chip in the control array
RAI 1,0	23, 24	**Row Address In 1, 0 (Digital Inputs).** These pins defined the row position of a chip in the control array.
CWI	25	**Control Word In (Digital Input).** Control word bytes are latched into the chip at this pin. Bit synchronisation and frame synchronisation are established by the CLK and FS in a similar way as on the DI0-7 pins. The bits in the input control word byte control whether reads or writes occur, allow different chips in a control array to be addressed, and control whether connections are busy or free.
CLK	26	**Clock (Digital Input).** The system clock, nominally 4.096MHz, is input at this pin. It is used with the pulse on FS to establish bit synchronisation on the data and control inputs and outputs.
V_{DD}	27	**Positive Supply Voltage (Power Input).** 5V.
FS	28	**Frame Synchronisation (Digital Input).** The negative pulse input at this pin is used with the CLK clock to establish the frame synchronisation on the data and control inputs and outputs. The duration of the pulse determines the modes of the data input and output converters.

Duration (clock periods)	Data Inputs	Data Outputs
1	Serial	Serial
2	Serial	Parallel
3	Parallel	Serial
4	Parallel	Parallel

FUNCTIONAL DESCRIPTION

The MS2002 is a 256 channel non-blocking digital switch capable of connecting all 256 incoming channels to all 256 outgoing channels in any desired order. Alternatively, selected input channels may be broadcast to any number of output channels. Each output channel may, however, receive from only one input channel at a time

Speech data is input to the device via 8 lines (DI0-7) that can accept 8 bit data in either serial or parallel format at a 2.048Mb/s rate. Speech data is output is via a further 8 lines which may be set independently of the input lines to give serial or parallel format data.

Call routings are held in an on-chip control store in the form of a nine bit word for each outgoing speech channel, bit nine (CM) indicating the busy status of the channel (0 = busy). In the case of a busy outgoing channel the remaining eight bits denote the number of the input channel to be connected to that outgoing channel.

The contents of the control store can be modified, and the speech or control store interrogated, via control messages received over the control inputs (CWI, CDI). Data generated by interrogation of either the control or speech store appears on the two control outputs (CWO, CDO).

Frame Formats

Serial inputs and outputs on the DSM are numbered in the same way as the CCITT 2048kbit/s PCM link (see Fig.3). This applies to both data and control information.

If the DSM is configured for parallel data on the data inputs or outputs then the Parallel Channels are numbered from 0 to 255 (see Fig.4).

These are different frame alignments for inputs and outputs (see Fig.5) The outgoing alignment is delayed by 21 bit periods with respect to the incoming alignment.

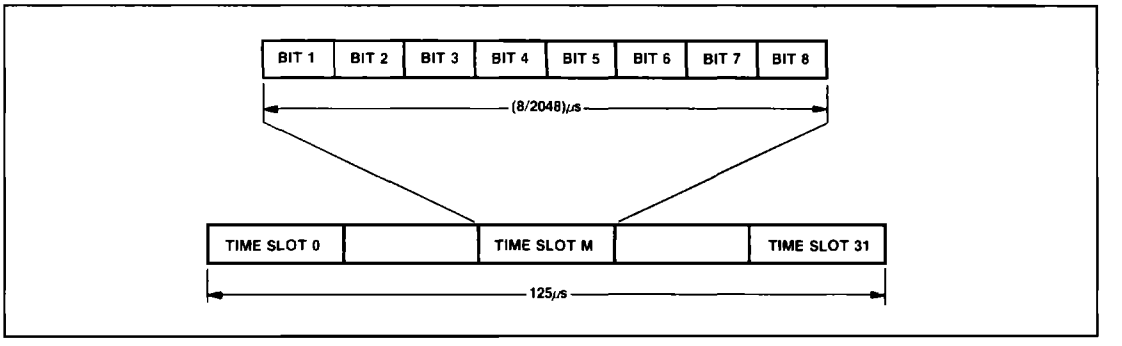


Fig 3 Serial format

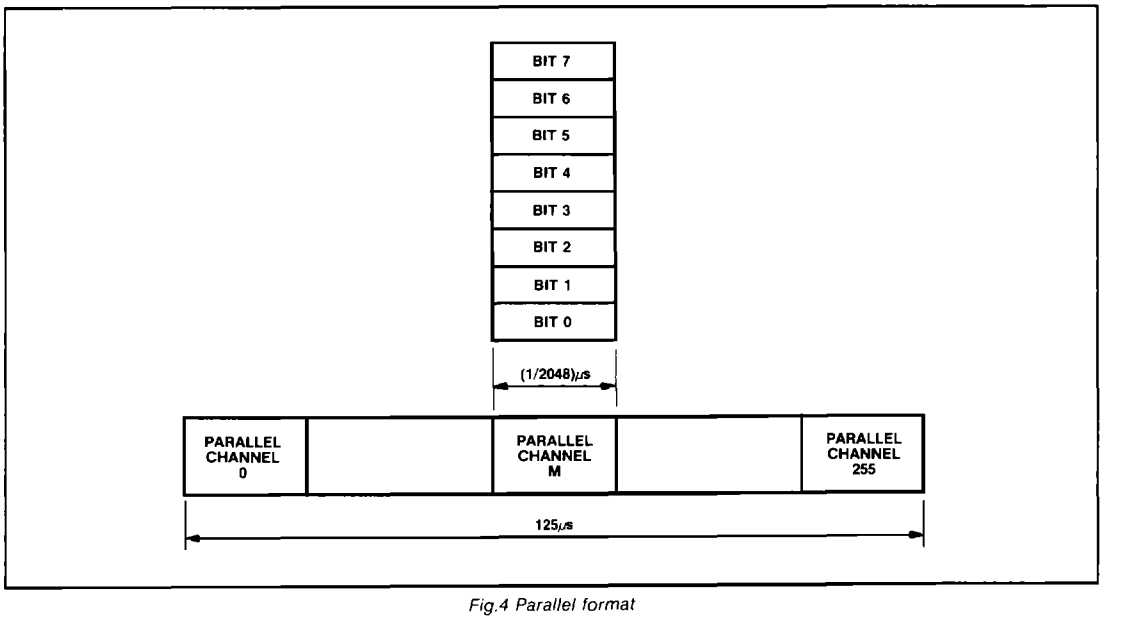


Fig.4 Parallel format

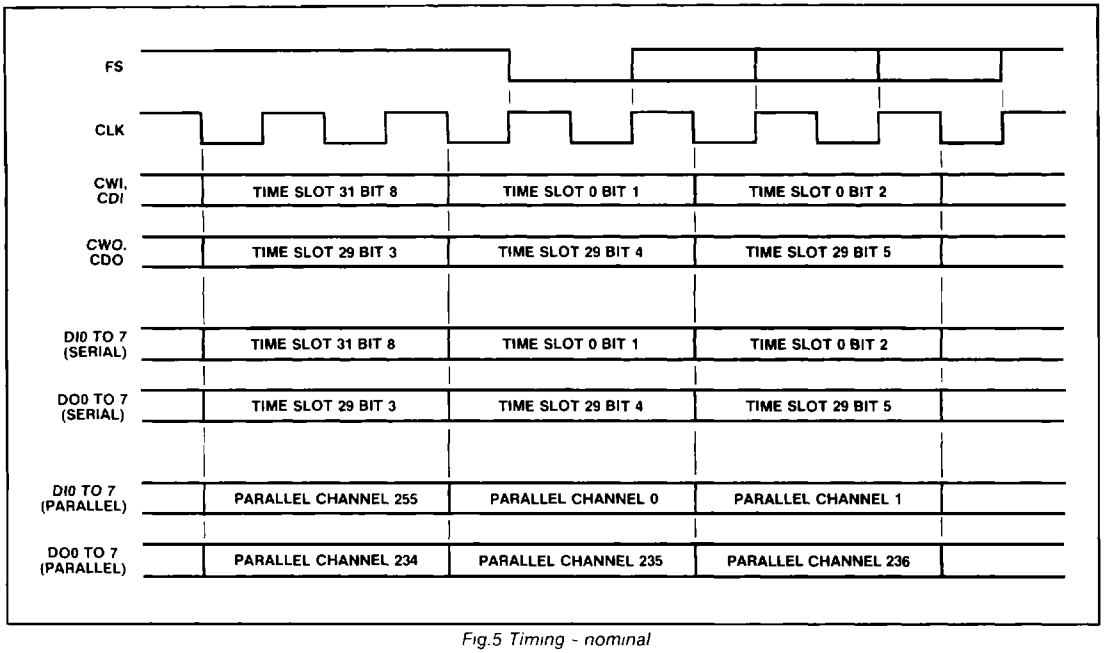


Fig.5 Timing - nominal

Speech Store

The Speech Store has 256 addresses each containing 8 bits. These addresses are associated with the Data In pins. If the DSM is configured for serial input then these addresses are organised by input pin and Time Slot (see Fig.6). If the MS2002 is configured for parallel input then these addresses correspond to the input Parallel Channels.

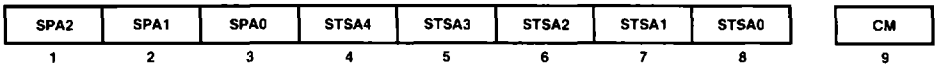
Control Store

The Control Store has 256 addresses each containing 9 bits. These addresses are associated with the Data Out pins in the same way that the Speech Store is associated with the Data In pins (see Fig.6).

Fig.7 shows how the 9 bits at each Control Store address are organised.

Store Address (Speech or Control)	Serial Time Slot Address (Input or Output)	Serial Pin Address (Input or Outut)	Parallel Channel (Input or Output)
0	0	0	0
1	0	1	1
2	0	2	2
3	0	3	3
4	0	4	4
5	0	5	5
6	0	6	6
7	0	7	7
8	1	0	8
9	1	1	9
	.	.	.
.	.	.	.
.		.	.
254	31	6	254
255	31	7	255

Fig.6 Relationship between inputs, outputs and stores



Bit	Name	Description
1-3	SPA2-0	**Speech Pin Address 2 to 0.** These bits are the Serial Pin Address in the Speech Store (see Fig.6) When used with the Speech Time Slot Address bits a unique Speech Store address is specified. This address corresponds to a Parallel Channel if parallel input is used.
4-8	STSA4-0	**Speech Time Slot Address 4 to 0.** These bits are the Serial Time Slot Address in the Speech Store (see Fig.6). When used with the Speech Pin Address bits a unique Speech Store address is specified. This address corresponds to a Parallel Channel if parallel input is used.
9	CM	**Connection Mode.** This bit determines whether the connection is busy or free and also helps to control reads from the DSM. If this bit is 0 then the connection is busy. If it is 1 then the connection is free. Fig.10 shows how this bit affects reads.

Fig.7 Bits at each control store address

Switching Delay

The switching function of the MS2002 is achieved by storing the incoming speech channels sequentially in the 256 x 8 speech store (after conversion to parallel format) and then sending them to the output channels in the order specified by the control store.

The delay encountered by each channel consists of a fixed delay, determined by the format conversion circuitry and the memory read/write cycle time, and a variable delay. The fixed delay is the 21 bits shown in Fig.5.

The variable delay is controlled by the sequence of writing to the speech store and reading from it under the direction of the control store. Input data is written to the speech store addresses in turn (see Fig.6). Output data is obtained by reading the control store addresses in turn and then reading the output data from the specified speech store address.

This means that when an input serial time slot is switched to the same output serial time slot then the delay is 21 bits if the Data In number is less than or equal to the Data Out number. The delay is 21 bits plus one frame if the Data In number is greater than the Data Out number.

The Control Array

The MS2002 is designed to be controlled in an array of two columns and four rows (see Fig.8). This control array need not be fully implemented. For example, a 512 channel switch can be constructed from two columns and two rows. If a large switch is required then control arrays can be arranged in a variety of architectures.

Each MS2002 in the Control Array uses the same control signals. These contain 32 Time Slots of 8 bits each.

The Time Slot used by an instruction is the Time Slot Address in the Control Store (see Fig.6). The format of the bits used for control, which is the same for both input and output, is shown in Figs. 9 and 10.

Instructions to the array are decoded according to the column in the array. The column whose Column Address pin matches the Column Address Bit on Control Word In responds to the instruction.

The write instruction can set up a connection from any one of the 1024 addresses in the Speech Stores of the 4 MS2002s in a row of the control array. The read instructions allow busy connections to be identified and monitored.

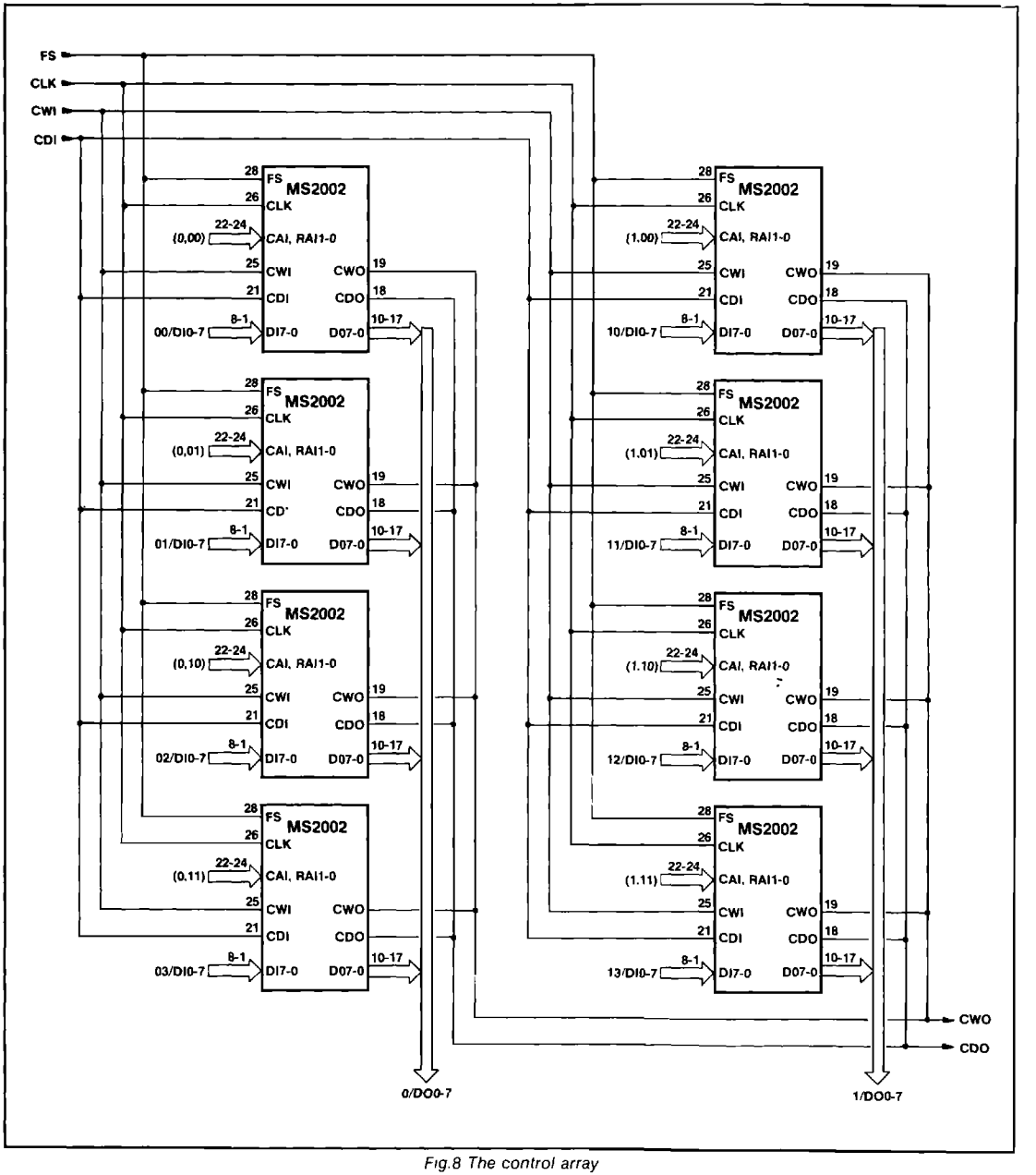
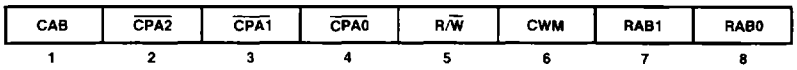


Fig.8 The control array



Bit	Name		Description
1	CAB		**Column Address Bit**
		In	If this bit matches the Column Address pin then the device will be written to or read from. If it does not match then Control Word Out and Control Data Out are high impedance during the output Time Slot.
		Out	This bit is set to the Column Address after a read from the Speech Store or after a write to the Control Store other than all 1's. It goes high impedance in all other cases.
2-4	$\overline{CPA2\text{-}0}$		**Control Pin Address 2 to 0**
		In	These bits are the Serial Pin Address at the Control Store (see Fig.6). The Time Slot Address is determined by the Time Slot on the Control Word In pin (see Fig.3). The Serial Pin and Time Slot Addresses define a unique address in the Control Store which corresponds to a Parallel channel if parallel output is used (Fig.6).
		Out	These bits are the same as those on the Time Slot on Control Word In if the Column Addresses match. They are high impedance otherwise.
5	R/$\overline{W}$		**Read or Write**
		In	This bit has no effect unless the Column Addresses match. If they do match then a read or write occurs depending whether it is 1 or 0 6 (see Fig.10).
		Out	This bit is the same as on the Time Slot on Control Word In if the Column Addresses match. It is high impedance otherwise.
6	CWM		**Control Word Mode**
		In	This bit has no effect unless the Column Addresses match. It can replace the Connection Mode bit at the Control Store address during writes or it can help to direct reads if the Column Addresses do match (see Fig.10).
		Out	This bit is the same as the Connection Mode bit at the Control Store address if the Column Addresses match. It is high impedance otherwise.
7-8	RAB1-0		**Row Address Bit 1 and 0**
		In	These bits have no effect unless the Column Addresses match. They help to control writes if the Column Addresses do match (see Fig.10). The Row Address Bits ensure that only one of the four MS2002s in a row of the Control Array can be active on the Data Out pins at any time.
		Out	These bits are set to the Row Address after certain operations and are high impedance otherwise. See Fig.11 for details.

Fig.9 Control word bits (both input and output) **NB** *The Control Word Out bits are open-drain pulldown outputs. This means that output high is the same as output high impedance*

Writing

The R/$\overline{W}$ bit of the instruction on Control Word In must be low for a write (see Fig.9). This causes a write to all MS2002s in the selected column. This write is to the same address in the Control Store of each MS2002. The Time Slot part of the address is the same as the Time Slot used by the instruction on Control Word In and Control Data In. The Pin part of the address is selected by the Control Pin Address bits in the Control Word (see Figs. 6 and 9).

The MS2002s in the selected column whose Row Address pins do not match the Row Address Bits in the Control Word have 1s written to the 9 bits at the address in the Control Store. This ensures that none of these MS2002s are in conflict with the remaining MS2002 on the Data Out pins. They also go high impedance during the control Time Slot on Control Word Out and Control Data Out (except for the $\overline{CPA2\text{-}0}$ and R/$\overline{W}$ bits which are the same for all MS2002s - see Fig.11).

The MS2002 whose Row Address matches responds differently to the instruction. The Control Word Mode bit and the Control Data bits are written into the address in the Control Store. This allows a connection to be established onto the Data Out pins. This MS2002 also responds differently on the control outputs unless the 9 bits written to the Control Store are all 1s. Fig.11 shows how the MS2002 acknowledges the instruction.

Reading

A read is performed automatically to acknowledge a write as mentioned in the previous section. It is also possible to read from the array independently of writing. The column selected by the Column Address Bit of the instruction will be read when the R/$\overline{W}$ bit is high. Reads are associated with an address in the Control Store. Either the bits at that address or the bits in the Speech Store selected by them will be read. This provides information about calls in progress or about the status of a connection.

The Row Address Bits in the instruction are ignored during reads. Each MS2002 which has one or more 0s at the selected address in its Control Store will respond to a read instruction. To avoid possible confusion about which MS2002 in a row is being read the array should be initialised by writing to it.

Two types of read are possible, depending on the input Control Word Mode bit. If this bit is 0 then a Type-0 Read occurs. Type-0 Reads are always from the Control Store. If the Control Word Mode bit is 1 then a Type-1 Read occurs. Type-1 Reads are from the Control Store or from the Speech Store depending on whether the Connection Mode bit at the Control Store address is 1 or 0 (free or busy). Fig.11 shows how the reads affect the control outputs.

Type-0 Reads indicate whether or not the connection through the array to the Data Out pins is busy or free. If it is busy then it identifies the MS2002 and Speech Store Address in it which sources the connection.

Type-1 Reads tap a connection to the Data Out pins if it is busy. They also indicate the MS2002 which sources the connection but cannot specify the origin within the MS2002 If there is no busy connection assocaited with the Control Store address the a Type-1 Read indicates the presence of 0s at the Control Store address.

$\overline{SPA2}$	$\overline{SPA1}$	$\overline{SPA0}$	$\overline{STSA4}$	$\overline{STSA3}$	$\overline{STSA2}$	$\overline{STSA1}$	$\overline{STSA0}$
1	2	3	4	5	6	7	8

Bit	Name	Description	
1-3	$\overline{SPA2-0}$	**Speech Pin Address 2 to 0**	
		In	These bits replace the Speech Pin Address bits at the Control Store address during a write if the Row Addresses match (see Fig.10). **NB** These bits are inverted with respect to those at the Control Store address. i.e. if these are all 0 then they refer to Speech Pin Address 7 (see Fig.6).
		Out	These bits are high impedance unless a read or write occurs. During a read these bits can contain the Speech Pin Address bits at the Control Store address or bits 1 to 3 of the Speech Store location addressed by the bits at the Control Store address (see Fig.11). **NB** These bits are inverted with respect to the contents of the Control Store but not with respect to the contents of the Speech Store.
4-8	$\overline{STSA4-0}$	**Speech Time Slot Address 4 to 0**	
		In	These bits replace the Speech Time Slot Address bits at the Control Store address during a write if the Row Addresses match (see Fig.11). **NB** These bits are inverted with respect to those at the Control Store address, i.e. if these are all 0 then they refer to Speech Time Slot Address 31 (see Fig.6).
		Out	These bits are high impedance unless a read or write occurs During a read these bits can contain the Speech Time Slot Address bits at the Control Store address or bits 4 to 8 of the Speech Store location addressed by the bits at the Control Store address (see Fig.11) **NB** These bits are inverted with respect to the contents of the Control Store but not with respect to the contents of the Speech Store.

Fig.10 Control data bits (both input and output) **NB** *The Control Data Out bits are open-drain pulldown outputs This means that output high is the same as output high impedance.*

Control Word In			CM Bit at Control Store Address	Instruction	Control Word Out			Control Data Out
R/W Bit	CWM Bit	Row Address			CAB Bit	CWM Bit	RAB1-0 Bits	
0	X	Matches	X	Write CWM bit + CDI bits	CAP Pin *†	Control Store Bit 9 (CM)†	RAP1-0 Pins *†	Control Store Bits 1-8†
0	X	Does Not Match	X	Write all 1s	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	X	Read Type 0	CAP Pin *†	Control Store Bit 9 (CM)	RAP1-0 Pins *	Control Store Bits 1-8
1	1	X	1	Read Type 1	High Impedance	Control Store Bit 9 (CM) = 1	High Impedance	Control Store Bits 1-8
1	1	X	0		CAP Pin†	Control Store Bit 9 (CM) = 0	RAP1-0 Pins	Speech Store Bits 1-8

Fig.11 The control operations

NB It is assumed that the Column Address matches in which case $\overline{CPA2\text{-}0}$ and R $\overline{W}$ are the same as on the control Time Slot on Control Word In The control outputs are high impedance during the control Time Slot if the Column Address does not match
* High Impedance if data at Control Store Address is all 1 s
† Should be identical to the data on the control inputs

ELECTRICAL CHARACTERISTICS

Test Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Characteristic	Symbol	Value			Units
		Min.	Typ.(1)	Max.	
Positive supply voltage	V_{DD}	4.75	5.0	5.25	V
Ambient temperature	T_{amb}	0		70	°C
Input low voltage	V_{IL}	0	0.4	0.8	V
Input high voltage	V_{IH}	2.0	2.4	V_{CC}	V
Output pullup resistor	R_{OP}	1000			Ω
Output load capacitor	C_{OP}	50			pF
Bias decoupling capacitor	C_{BB}	900	1000	1100	pF

Digital Static Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Supply current	I_{DD}		40	60	mA	Unloaded
Input leakage current	I_{LI}			50	μA	$0 < V < V_{CC}$
Output low voltage	V_{OL}	0		0.4	V	I_{OL} (Sink) = 2mA
Output low voltage	V_{OL}	0		2.0	V	I_{OL} (Sink) = 8mA
Output leakage current	I_{LO}			50	μA	$0 < V < V_{CC}$

Analog Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Pin capacitance	C_P		8	10	nF	Unloaded

Digital Switching Characteristics - Clock (see Fig.12)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Clock period	t_{CP}	225	244	275	ns	
Clock rise time	t_{CR}		50		ns	
Clock high period	t_{CH}	82			ns	
Clock fall time	t_{CF}		50		ns	
Clock low period	t_{CL}	82			ns	

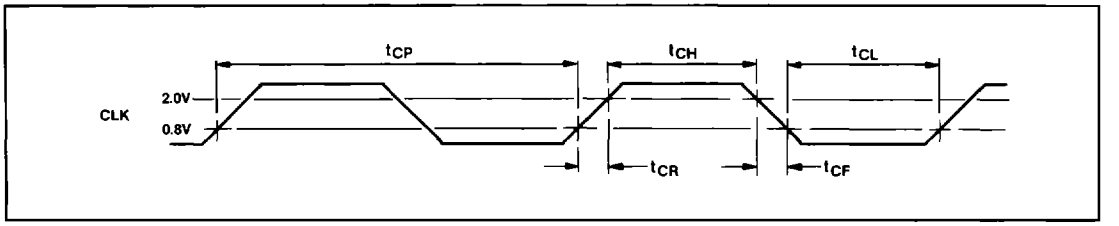


Fig.12 Timing - clock

Digital Switching Characteristics - Frame Synchronisation (see Figs.5 and 13)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Frame Synchronisation falling hold time	t_{FFH}	90	122		ns	
Frame synchronisation falling setup time	t_{FFS}	60	122		ns	
Frame synchronsiation rising hold time	t_{FRH}	90	122		ns	
Frame synchronisation rising setup time	t_{FFS}	60	122		ns	

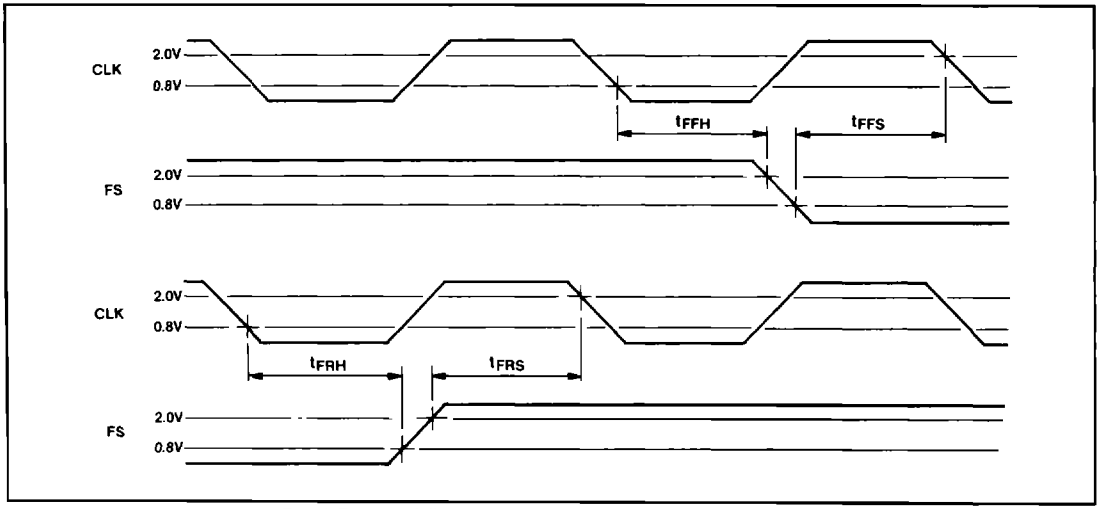


Fig.13 Timing - falling and rising edges of frame synchronisation

Digital Switching Characteristics - Data and Control Inputs and Outputs (see Figs.5 and 14)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Input setup time	t_{IS}	60	244		ns	
Input hold time	t_{IH}	90	244		ns	
Output hold time	t_{OH}	5			ns	
Output delay	t_{OD}			150	ns	

NOTE
1 Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

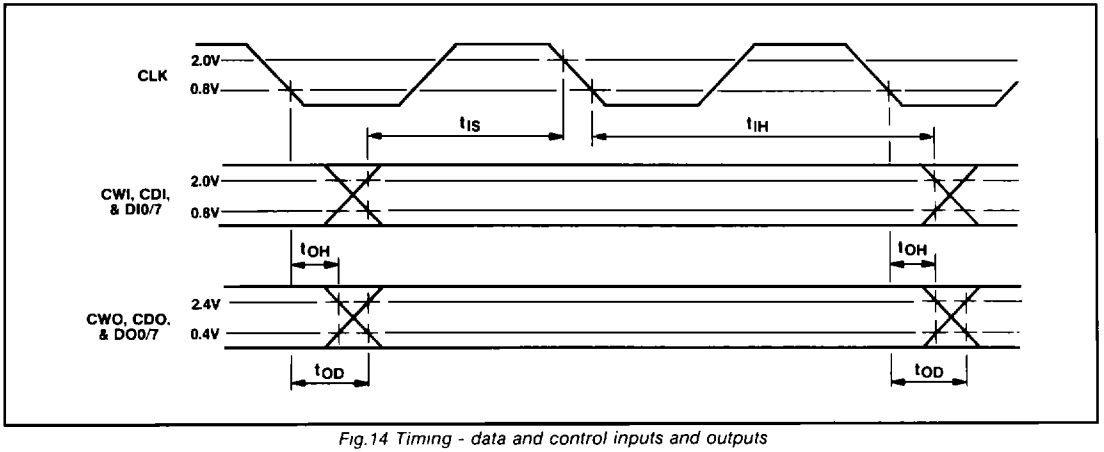


Fig.14 Timing - data and control inputs and outputs

ABSOLUTE MAXIMUM RATINGS

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Positive supply voltage, V_{DD}	-0.5V to +7V
Storage tempertaure, T_{ST}	-65°C to +150°C
Digital input voltage, V_{ID}	-0.3V to V_{DD} +0.3V
Clamp current (Sink or Source), I_C	50mA
Package power dissipation, P_P	800mW