CW10 (HFA3841IV)
WLAN MAC controller

CHOICE MICROSYSTEMS

The CW10 is a single chip controller that provides all processing and functionality needed for the MAC protocol of the IEEE 802.11 standard for wireless LANs. The CW10 supports a glueless interface to a host computer conforming to PC Card 95, and can control a variety of radio frequency (RF) modems. A minimum implementation consists of the CW10, at least 64K bytes of static RAM, and a clock source.

Medium Access Control (MAC) functionality is required any time a medium, such as network wiring or the frequency band used by a radio, accessible by more than one device. The CW10 implements protocols that manage the sharing according to standard rules recognized by all devices. Just as the IEEE 802.3 standards define the MAC rules for Ethernet networks, the IEEE 802.11 standard defines the MAC rules for wireless LANs.

The CW10 supports direct-sequence or frequency-hopping spread spectrum radios in the 915MHz, 2.4GHz, and 5.2GHz bands, at data rates up to 12Mb/s.

CW10 Family Members:

- The CW10 provides the functionality of an 802.11 Station device.
- The CW10AP provides the additional functions needed in an 802.11 Access Point (power save buffering, PS-poll response, intra-BSS frame forwarding, priority access to transmit queues from the host interface,. and optional point coordination).

The CW10 provides a glueless interface to most 802.11-compatible RF Modems (PHYs):

- Direct sequence (DS) spread spectrum PHYs and high speed PHYs for 802.11a and 802.11b are supported through a pair of highly configurable serial interfaces for Modem Data and Modem Management.
- Frequency hopping (FH) spread spectrum PHYs that provide a serial digital bitstream interface to the MAC can be connected directly. FH PHY designs that provide an analog interface will require an additional interface chip.
- A memory mapped parallel interface is also available for PHYs that are designed for connection to a processor bus.
- Custom PHY support is available for a nominal NRE charge.

Features:

- Supports 802.11 PHYs and enhanced data rates up to12Mb/s.
- 128-pin thin quad flat pack (TQFP) to fit PCMCIA type 2 form factor.
- 3.3V operation with 5V tolerant I/O signals.
- Low Power consumption: 25mA active, 8mA doze, <1mA sleep. Supports all 802.11 power management modes, with dynamically variable clock speed for further power saving.
- Implements the full IEEE 802.11 wireless LAN MAC protocol, including the optional Point Coordination Function (PCF), Wired Equivalent Privacy (WEP) and shared key authentication.
- Real-time WEP encryption and decryption are implemented using special hardware to accelerate keystream generation. This allows a unique Initialization Vector (IV) to be used for each frame with no loss of throughput.
- The CW10 can generate and decode PHY Layer Convergence Protocol (PLCP) for direct attachment to RF modems with a serial bitstream interface.
- The CW10 handles low level protocol functions without host intervention, including acknowledgment, RTS/CTS, fragmentation and de-fragmentation, and automatic beacon monitoring.

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- Active or passive scanning performed autonomously by CW10 once initiated by host command.
- The CW10 includes 2Kx16 on-chip control store RAM to hold time critical firmware, and 512x16 on-chip data store RAM. (On-chip RAM not available in gate array version.)
- Can address up to 4MB of address space, including up to 3.5MB of buffer RAM.
- Host interface attaches without glue to 16-bit PC Card 95 connector. Supports 8 and 16 bit transfers to and from host memory. Also supports direct connection to ISA or embedded CPU bus.
- Host interface pins assigned to allow simple routing of PC board traces to PC Card 95 Connector, memory, and PHY.
- Host interface command and status handshakes allow concurrent operations from multi-threaded I/O drivers.
- PCMCIA host interface includes address decode for system boot ROM, with zero glue interface to enable a ROM chip attached to the PC Card 95 bus. A special "genesis" mode allows programming of local flash memory through the host interface for production and firmware upgrades.
- On-chip UART for remote I/O and other serial wired interface configurations.
- Configuration from serial EEPROM, parallel flash EPROM, or wait for download through host interface.
- On-chip oscillator can drive PHY, or PHY can provide clock to MAC. A clock prescaler allows clocks from 6MHz to 50MHz to be used.

CW10 Block Diagram