FUJITSU

8-CHANNEL 8-BIT A/D CONVERTER

MB 4066

June 1987
Edition 1.0

8-CHANNEL 8-BIT A/D CONVERTER

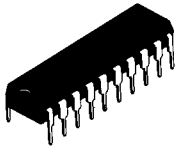
The Fujitsu MB 4066 is an analog-to-digital converter (ADC) for general purpose which features eight channels of analog inputs and 8-bit data length of digital output.

Analog input signal is converted to serial 8-bit digital data by the successive-approximation technique which provides high-speed conversion, i.e. many analog data can be converted within a short time.

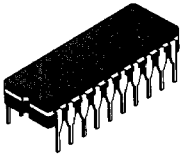
Additionally, the MB 4066 has dual range conversion capability, which provides sequentially one data of both range, standard and contracted modes, to chose better data between them and to delete the range change time.

All digital I/O signals including control inputs are TTL level compatible so as to provide wide application such as in microprocessor-controlled system and so on.

- Single Power Supply: +7.6 V to +18 V
- Multiplex 8-Channel Analog Inputs:
- Resolution: 8 bits
- Linearity: ±0.19% Max.
- Analog Input Voltage Ranges:
- Automatic Range Change/Dual Range Conversion: 0 to V_{REF} Standard mode; 0 to 1/4V_{REF} Contracted mode
- Successive-Approximation Conversion: 100 μs/ch Max. at f_{CLK} = 100 kHz
- Ratio-metric Conversion by Reference Voltage V_{REF}
- Serial Data Output (Open Collector)
- TTL/CMOS Compatible Digital I/O
- Power Consumption: 160 mW Typ. at V_{CC} = 8V
- Standard 20-pin Dual In-line Package

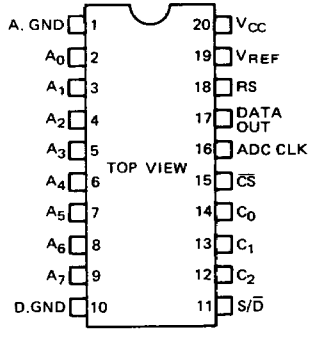


PLASTIC PACKAGE
DIP-20P-M01



CERAMIC PACKAGE
DIP-20C-C03

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	+20	V
Digital Input Voltage		V_{ID}	+20	V
Digital Output Voltage (Off-State)		V_{OH}	+20	V
Analog Input Voltage		V_{IA}	+20	V
Reference Voltage		V_{REF}	+5.5	V
Storage Temperature	Ceramic	T_{STG}	−55 to +150	V
	Plastic	T_{STG}	−40 to +125	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Fig. 1 – MB 4066 BLOCK DIAGRAM

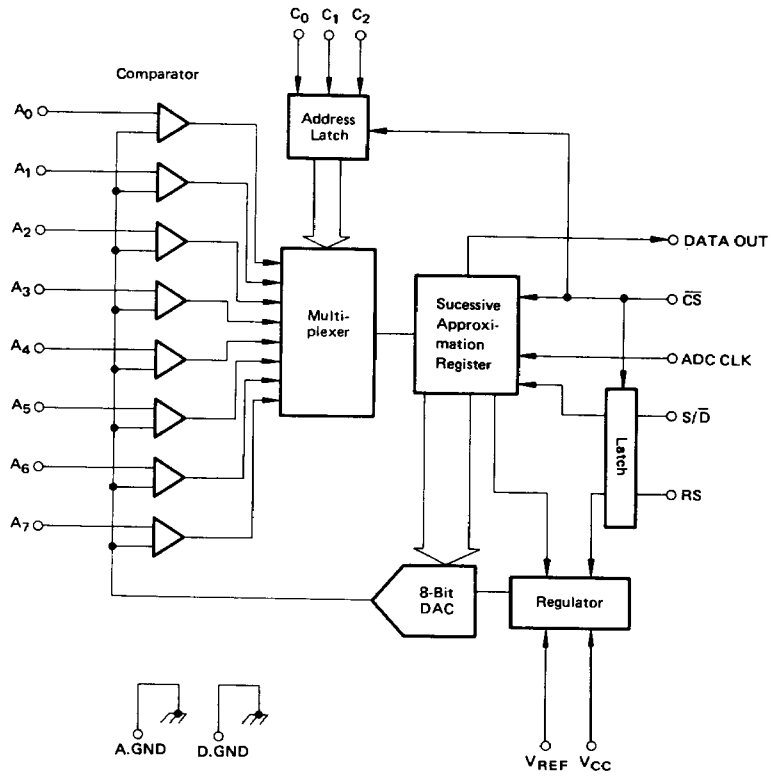

TABLE 1: CONVERSION MODES

S/D	RS	1st Conversion	2nd Conversion
L	L	Contracted Range	Standard Range
L	H	Standard Range	Contracted Range
H	L	Contracted Range	–
H	H	Standard Range	–

TABLE 2: CHANNEL SELECTIONS

C_2	C_1	C_0	Channel
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

PIN DESCRIPTIONS

Pin Name	Pin No.	Descriptions
A_0 to A_7	2 to 9	**Analog Inputs** These inputs are provided to receive eight channels of analog inputs. One of them is selected by a combination of C_0 to C_2.
S/$\overline{D}$	11	**Conversion Mode Select Input** This control input is provided to select a conversion sequence with RS input as shown in Table 1. When low, analog input voltage is converted in both ranges, and when high, in one range only. This input is latched at the falling edge of $\overline{CS}$.
C_2 to C_0	12 to 14	**Channel Select Inputs** These inputs are used to select one of eight analog input as shown in Table 2. This inputs are latched at the falling edge of $\overline{CS}$.
$\overline{CS}$	15	**Chip Select Input** This control input is used to start analog to digital conversion and to terminate it. When $\overline{CS}$ goes low, the A/D conversion starts and the DATA OUTPUT is enabled. When the A/D conversion is completed or termination of the conversion is required, $\overline{CS}$ is made high.
ADC CLK	16	**A/D Conversion Clock** This clock signal is used for A/D conversion. The conversion speed is determined by this clock rate. But precise stability of the clock rate is no required.
DATA OUT	17	This output is provided to output the A/D conversion results as digital signals. The converted digital data are serially output in the order of start-bit, MSB (Most Significant Bit), 2SB (Second Significant Bit), . . . , 7SB, LSB (Least Significant Bit) and stop-bit in synchronous with the ADC CLK.
RS	18	**Range Select Input** This control input is provided to select an analog input voltage as shown in Table 1. This input is latched at the falling edge of $\overline{CS}$.
V_{REF}	19	**Reference Voltage Input** This input provides the conversion reference for the analog to digital conversion circuit.
A. GND D. GND	1 10	Analog Ground Digital Ground
V_{CC}	20	Power Supply Voltage, 7.6 V to 18 V.

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.6	12	18	V
Reference Voltage	V_{REF}	4.75	5.00	5.25	V
Digital Output Low Current	I_{OL}			8	mA
Ambient Operating Temperature	T_A	-40		+85	℃

ANALOG CIRCUIT CHARACTERISTICS

(Recommended Operating Condiions unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Resolution					8	bit
Linearity Error					±0.5	LSB
Differential Linearity Error					±0.9	LSB
Zero Transition Voltage	V_{ZS}	Standard Conversion Mode V_{REF} = 5.000V		20		mV
Full Scale Transistion Voltage	V_{FS}			4980		mV
Zero Transition Voltage	V_{ZC}	Contracted Conversion Mode V_{REF} = 5.000V		5		mV
Full Scale Transition Voltage	V_{FC}			1245		mV
V_{REF} Input Current	I_{REF}	V_{REF} = 5.000V	0.5	1.0	2.0	mA
Comparator Input Current	I_{COP}				-250	nA
Conversion Time	t_{CYC1}	f_{CLK} = 100kHz, S/D = "1"			100	μs/CH
	t_{CYC0}	f_{CLK} = 100kHz, S/D = "0"			200	μs/CH

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DIGITAL CIRCUIT DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Input High Voltage	V_{IH}			2.0			V
Input Low Voltage	V_{IL}					0.8	V
Input Clamp Voltage	V_{IC}	I_{IL} = −18mA				−1.5	V
Output High Current	I_{OH}	V_{IH} = 2V, V_{IL} = 0.8V V_{OH} = 20V				100	μA
Output Low Voltage	V_{OL}	V_{IH} = 2V V_{IL} = 0.8V	I_{OL} = 4mA			0.4	V
			I_{OL} = 8mA			0.5	V
Input High Current	I_{IH}	V_{IH} = 2.7V				20	μA
		V_{IH} = 20V				100	μA
Input Low Current	I_{IL}	V_{IL} = 0.4V			−20	−100	μA
Power Supply Current	I_{CC}	V_{CC} = 20V			20	38	mA

DIGITAL CIRCUIT AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
ADC CLK Cycle Time	t_{CY}	10			μs
ADC CLK H level Pulse Width	$t_{WAC}{}^{+}$	2.5			μs
ADC CLK L level Pulse Width	$t_{WAC}{}^{-}$	2.5			μs
$\overline{CS}$ H level Pulse Width	$t_{WCS}{}^{+}$	1.5			μs
$\overline{CS}$ Set-up Time	t_{SCS}	1			μs
$\overline{CS}$ Hold Time	t_{HCS}	1			μs
Channel Set-up Time	t_{SCH}	0			μs
Channel Hold Time	t_{HCH}	1.5			μs
Propagation Delay Time	t_{PLH}		0.8	2	μs
	t_{PHL}				

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Fig. 2 – AC MEASUREMENT CIRCUIT

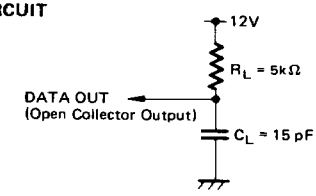

Fig. 3 – AC TIMING DIAGRAM

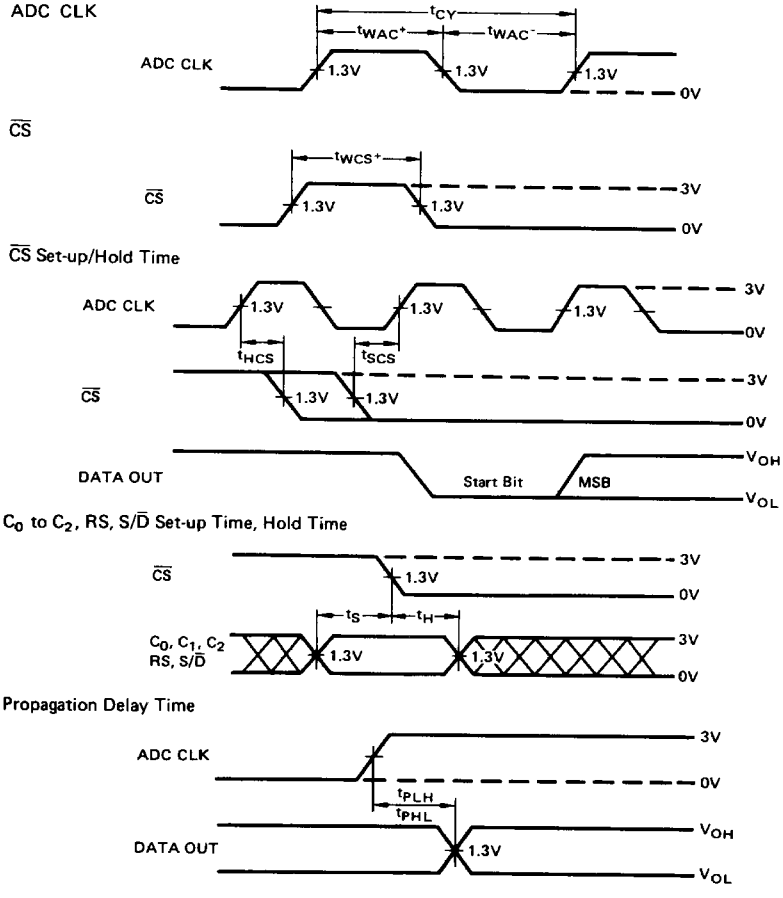

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Fig. 4 – TIMING DIAGRAM ($S/\overline{D}$ = "0")

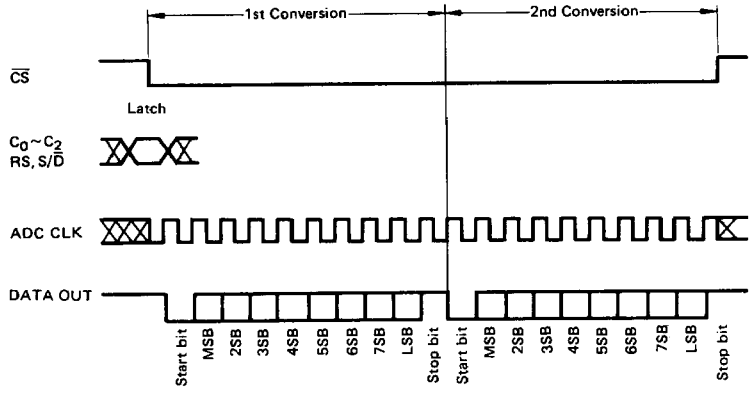
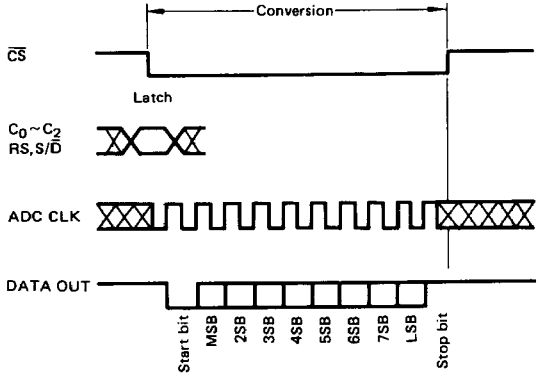


Fig. 5 – TIMING DIAGRAM ($S/\overline{D}$ = "1")



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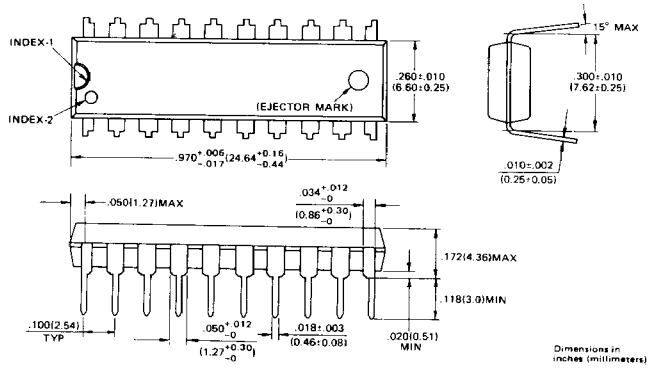
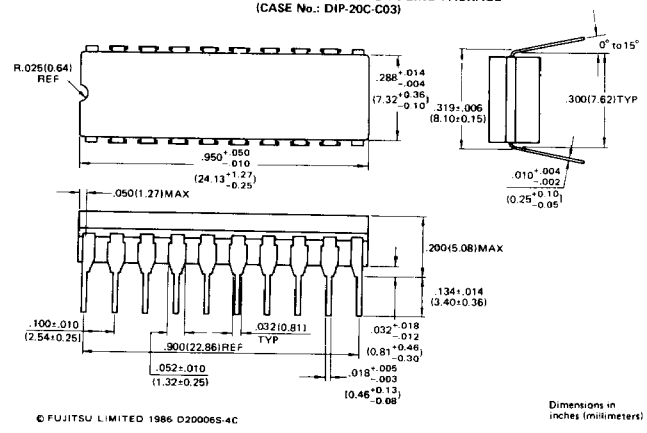
PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M01)



20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)



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