20420

Integrated Analog Device for GSM Applications

Conexant's 20420 Integrated Analog (IA) device is a highly integrated, mixed signal device designed for use in GSM 900/1800/1900 cellular handsets. With its companion devices, the M46 Baseband Processor (BP), see Conexant document 100779C, and the 20436 Power Management Integrated Circuit (PMIC), see Conexant document 100772B, the IA forms Conexant's Baseband Device Set for GSM single-band or multi-band handsets.

The IA performs all the mixed signal functions required in a GSM handset. The IA also provides interfaces to the BP and RF subsystem. Three serial ports are available to allow configuration of the IA by the BP, and transfer of data between the IA and BP. A programmable state machine is included to control the operation of the RF subsystem with discrete transmit power and receiver gain control signals.

The IA generates Gaussian Minimum-Shift Keying (GMSK) modulated In-Phase and Quadrature (I/Q) signals for upconversion and transmission by the RF subsystem, and digitizes the received Intermediate Frequency (IF) output from the RF subsystem. A voiceband Codec provides interfaces for the microphone and speaker, and an Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC) for signal conversion.

The IA is designed to operate over a voltage range of 2.7–3.6 V for optimum low-power system performance.

The IA is available in a 100-pin Chip Array Ball Grid Array (CABGA) package. IA package and pin configuration are shown in Figure 1. A block diagram of the 20420 IA is shown in Figure 2. The signal pin assignments and functional pin descriptions are specified in Table 1.

Features

- Bandpass Σ-Δ A/D conversion of the received IF signal
- Programmable control of receive path gain
- Burst store RAM for storage of transmit data
- GMSK modulation of burst store contents
- D/A conversion of I/Q output from the GMSK modulator
- Programmable control of RF transmit signal ramping profile and power level
- Low noise voiceband ADC for interface to handset microphone
- Low noise voiceband DAC for interface to handset speaker
- Intra-Frame Sequencer (IFS) state machine for programmable control of system timing signals and RF control signals
- Synthesizer state machine and serial interface for control of the RF subsystem synthesizer device
- Generation of system timing reference signals for baseband circuitry and the RF synthesizer device
- Auxiliary ADC to monitor systems signals such as battery voltage
- Serial ports for interface to Conexant's M46 Baseband Processor

Applications

- GSM 900/1800/1900 handsets or modules

	1	2	3	4	5	6	7	8	9	10
A	MIC_BIAS	LINEIN_P	TX_PWR_P	TX_EN_2	AVSS	AVDD	TX_Q_M	AVSS	AVSS	TX_RX
B	MIC_P	LINEIN_M	TX_EN_0	TX_I_M	AVSS	VREF	RX_IF_P	RX_IF_M	AUXADC2P	AUXADC2M
C	MIC_M	CDCVREFC	TX_PWR_M	TX_EN_1	VREFC	TX_Q_P	AVDD	NC	AUXADC1	SYNREF19
D	AVDD	CDCVREF	LINE0_M	TX_I_P	AVDD	AVDD	XTAL_IN	AVDD	XTAL_OUT	VOSC
E	SPKR_P	AVSS	AVDD	LINE0_P	RBIAS	V_SUB	NC	DVSS	AVSS	AVSS
F	DVDD	DVSS	AVSS	SPKR_M	V_SUB	DVDD	SYN_DAT	SYNFRM_0	DVDD	SYNE
G	RX_GAIN0	RXGAIN1	RXEN2	RXGAIN2	CNTRLDAT	DVSS	RX_DATA	SYN_LOCK	STATUS1	SYN_CLK
H	RXEN0	RXEN1	NC	CNTRLRT	CNTRLCLK	DVDD	SYS_CLK	DVSS	SYNFRM_1	STATUS2
J	NC	HIGHBAND	CDCCLK	ENCDRDAT	V_SUB	RX_RATE	RX_CLOCK	DVDD	CLK_REQ	PWRONRST
K	NC	CDCRATE	DCDRDAT	RSPNSDAT	DVSS	NU	FRAME_RT	DVDD	DVSS	RESET

C881

Figure 1. IA Device Pinout - Top View

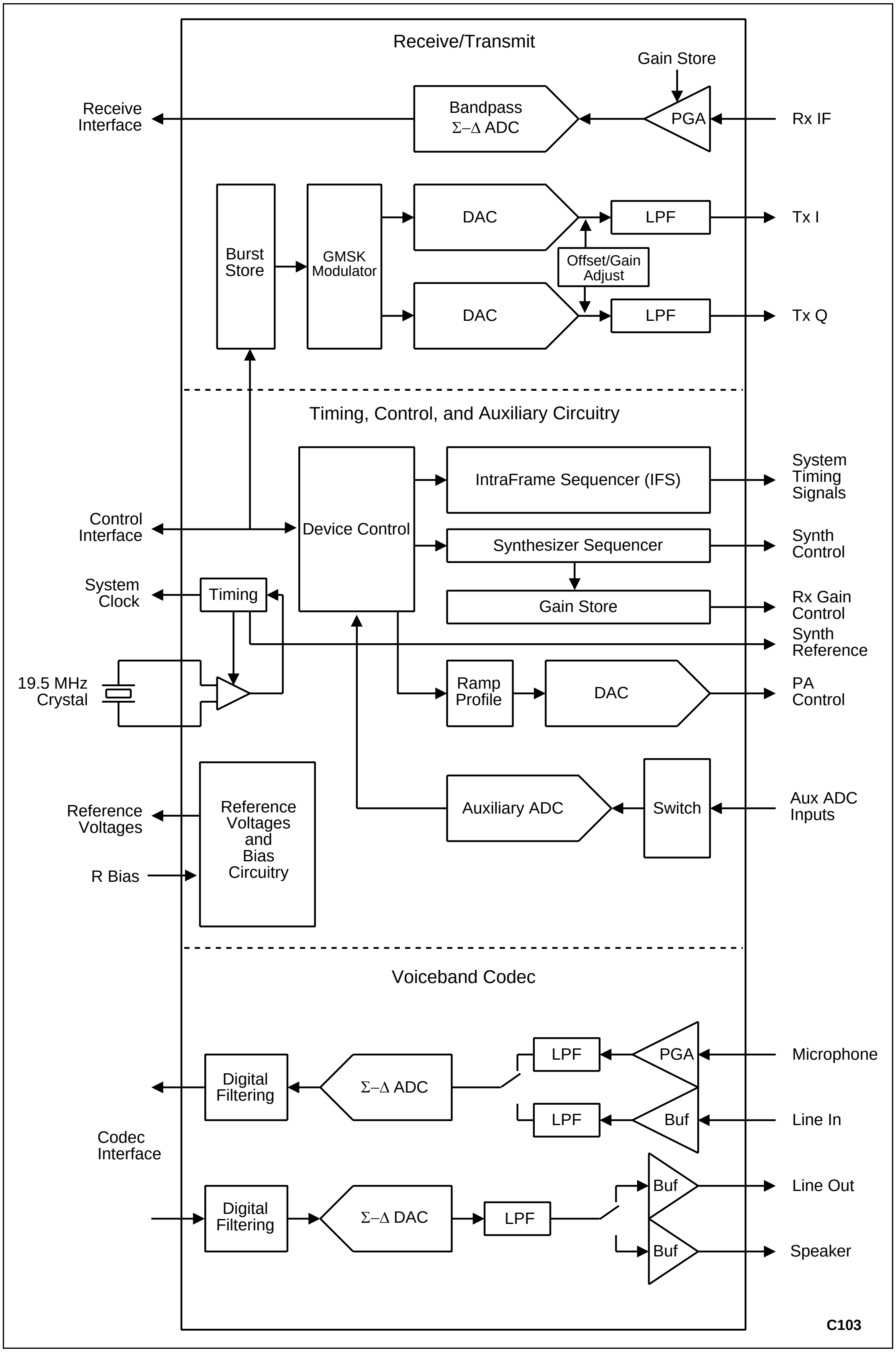

Figure 2. IA Device Block Diagram

Table 1. IA Device Pinout Assignments (1 of 2)

Pin #	Pin Name	Description
Power		
F1, F6, F9, H6,, J8, K8	DVDD	Digital supply
E8, F2, G6, H8, K5, K9	DVSS	Digital ground
A6, C7, D1, D5, D6, D8, E3	AVDD	Analog supply
A5, A8, A9, B5, E2, E9, E10, F3	AVSS	Analog ground
D10	VOSC	Crystal oscillator supply
E6, F5, J5	V_SUB	Substrate ground
Reference Voltages		
B6	VREF	Reference voltage output (2.35 V)
C5	VREFC	Bias reference voltage output (1.35 V)
D2	CDCVREF	Codec reference voltage output (2.35 V)
C2	CDCVREFC	Codec bias reference voltage output (1.35 V)
E5	RBIAS	Resistor bias for internal references. Connect 121 kΩ ± 1% resistor from RBIAS to AVSS ground.
System Signals		
J9	CLK_REQ	Clock request input
K10	RESET	System reset signal
J10	PWRONRST	Power on reset signal
K7	FRAME_RT	GSM frame rate output
Clock Generation / Timing		
H7	SYS_CLK	System clock output (3.9 MHz)
D7	XTAL_IN	19.5 MHz crystal oscillator input signal
D9	XTAL_OUT	19.5 MHz crystal oscillator input signal
C10	SYNREF19	19.5 MHz reference signal for RF frequency synthesizer
Receiver Input		
B7	RX_IF_P	Receiver IF positive input
B8	RX_IF_M	Receiver IF negative input
Transmitter Output		
D4	TX_I_P	Transmitter I channel positive output
B4	TX_I_M	Transmitter I channel negative output
C6	TX_Q_P	Transmitter Q channel positive output
A7	TX_Q_M	Transmitter Q channel negative output
RF Subsystem Control		
G3	RXEN2	RF receiver enable control 2
H2	RXEN1	RF receiver enable control 1
H1	RXEN0	RF receiver enable control 0
G4	RXGAIN2	RF receiver gain control 2
G2	RXGAIN1	RF receiver gain control 1
G1	RXGAIN0	RF receiver gain control 0
J2	HIGHBAND	GSM/DCS band select
A10	TX_RX	Transmit/receive select

Table 1. IA Device Pinout Assignments (2 of 2)

Pin #	Pin Name	Description
RF Subsystem Control (continued)		
A4	TX_EN_2	RF transmitter enable control 2
C4	TX_EN_1	RF transmitter enable control 1
B3	TX_EN_0	RF transmitter enable control 0
G8	SYN_LOCK	Synthesizer lock input
F10	SYNEN	Synthesizer enable
A3	TX_PWR_P	Transmit power control positive output
C3	TX_PWR_M	Transmit power control negative output
Audio		
B1	MIC_P	Microphone positive input
C1	MIC_M	Microphone negative input
A1	MIC_BIAS	Regulated output voltage to bias the handset microphone
E1	SPKR_P	Speaker positive output
F4	SPKR_M	Speaker negative output
A2	LINEIN_P	Line positive input
B2	LINEIN_M	Line negative input
E4	LINEO_P	Line positive output
D3	LINEO_M	Line negative output
Serial Ports		
H4	CNTRLRT	Control port rate signal
G5	CNTRLDAT	Control port data in signal
K4	RSPNSDAT	Control port data out signal
H5	CNTRLCLK	Control port clock
J6	RX_RATE	Receive port rate signal
G7	RX_DATA	Receive port data signal
J7	RX_CLOCK	Receive port clock signal
K2	CDCRATE	Codec port rate signal
K3	DCDRDAT	Codec port decoder data
J4	ENCDRDAT	Codec port encoder data
J3	CDCCLK	Codec port clock
H9	SYNFRM_1	Synthesizer port enable signal 1
F7	SYN_DATA	Synthesizer port output data
G10	SYN_CLK	Synthesizer port output clock
F8	SYNFRM_0	Synthesizer port enable signal 0
Auxiliary ADC		
C9	AUXADC1	Auxiliary ADC 1 input, single-ended
B9 B10	AUXADC2P AUXADC2M	Auxiliary ADC 2 positive input Auxiliary ADC 2 negative input
Miscellaneous		
G9	STATUS1	Logic level of this pin is stored in an IA register
H10	STATUS2	Logic level of this pin is stored in an IA register
C8, E7, H3, J1, K1	NC	No connect. Do not connect to this pin.
K6	NU	Not used. Connect to ground.

Technical Description

Clock Generation

The IA provides an oscillator circuit that generates a 19.5 MHz reference signal when used with an external 19.5 MHz crystal. This reference is used to generate a reference clock for the RF subsystem frequency synthesizer, a 3.9 MHz system clock for the baseband digital device, and all the timing signals required by the internal circuitry of the IA.

To minimize power dissipation, the oscillator circuit and the clock generation circuits can be turned off when the handset enters low power mode.

The clock generation circuit consists of the following blocks:

- Crystal oscillator circuit
- Synthesizer reference signal circuit
- System clock circuit

Crystal Oscillator Circuit. The crystal oscillator circuit features an internal oscillator function, which is used with an external crystal. The contents of an internal register, the Oscillator Control Register, are used to tune the crystal oscillator frequency. The external components required are a 19.5 MHz crystal, a bias resistor, and a load capacitor. The output of the oscillator circuit is a 19.5 MHz reference signal. A block diagram for the internal and external parts of the circuit is shown in Figure 3.

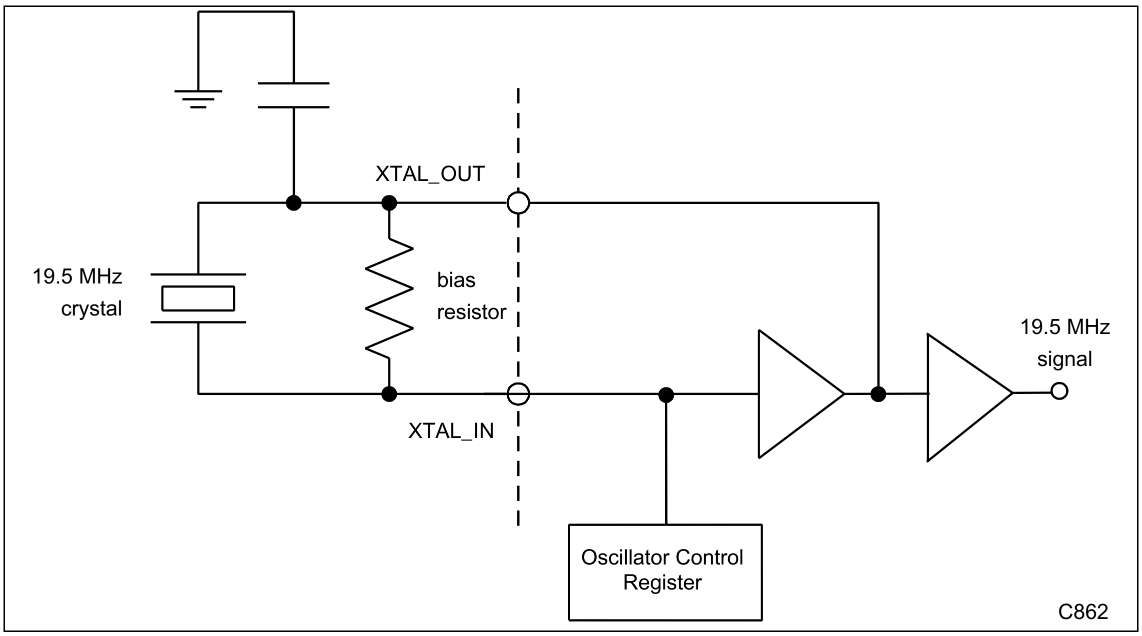

Figure 3. Crystal Oscillator Circuit Block Diagram

Synthesizer Reference Signal Circuit. The IA produces a reference signal for use by the synthesizer device in the RF subsystem. A 19.5 MHz reference output is provided on SYNREF19 (pin C10). Figure 4 shows the load circuit for the SYNREF19 pin.

System Clock Circuit. The IA generates a 3.9 MHz system clock from the 19.5 MHz reference signal. The 3.9 MHz clock is available for use by the BP.

Control Interface

The control interface is a four-wire serial interface, which allows the BP to control and configure the IA. The interface is a high speed, synchronous, full duplex, serial communications link.

The control interface consists of the following signals:

- CntrlClk: 3.9 MHz clock signal input to the IA.
- CntrlrT: Control input signal used to indicate the start and end of a data transfer session between the BP and IA.
- CntrlDat: Serial input data to the IA.
- RspnsDat: Serial output data from the IA.

The BP is the bus master for the control interface and initiates all communications over the interface. The BP uses the control interface to perform the following functions:

- Send control information to configure IA operation.
- Send bursts of transmit data for modulation by the IA.
- Read contents of the IA registers.

Figure 5 shows the Control Interface timing diagram for write and read operations.

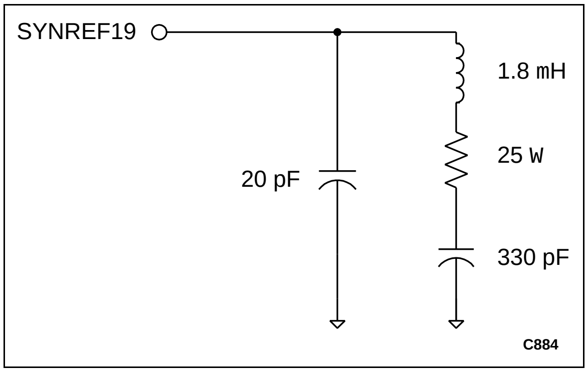

Figure 4. SYNREF19 Load Circuit

Table 2. 20420 IA Register Addresses

Address (hex)	Name	Function
00–3F	Intra-Frame Sequencer	RAM for Intra-Frame Sequencer state machine
40–5F	Ramp Store	RAM for transmitter power ramping profile
60–6F	Synthesizer Sequencer	RAM for Synthesizer Sequencer state machine
70–7B	Burst Store RAM	RAM for storing one burst of data bits to be modulated
7C	Tx Offset	Adjusts I/Q transmit channel DC offset voltage
7D	TX I/Q Control	Adjusts I/Q transmit channel gain imbalance
7E	Reserved	—
7F	Crystal Oscillator Control	Tune the oscillator frequency of the crystal oscillator circuit
80	Reserved	—
81	Encoder Control	Controls the voiceband encoder operation
82	Decoder Control	Controls the voiceband decoder operation
83	Auxiliary ADC Input Select	Selects the input to the Auxiliary ADC
84	Reserved	—
85	Reserved	—
86	Master Control	Control register for enabling / disabling various IA functions
87	Auxiliary ADC	Contains the 8-bit, two's-complement output from the Auxiliary ADC
88–FF	Reserved	—

Intra-Frame Sequencer

The Intra-Frame Sequencer (IFS) is a programmable state machine that generates timing and control signals for the RF subsystem and internal IA circuits. The IFS consists of a 64-word RAM (each word is 16 bits wide) that is written to over the control interface. The IFS RAM is located at IA register addresses 0x00 to 0x3F (Table 2). There are 32 states in the IFS, with each state controlled by two words:

- Duration Word: defines the duration of the state.
- Assertions Word: defines the logic level of each of the control signals in the state.

The duration word for each state specifies the length of the state, as a number of 2.166 MHz clock cycles (1 cycle = 0.4625 µs). This frequency is 8 times the system bit rate (270.833 kbps). Bits 14–0 of the duration word specify the number of clock cycles in the state. The length of the state is calculated as follows:

$$(\text{Duration Word}[14:0] + 1) \times 0.4625\ \mu s$$

Bit 15 is a reset bit. If this bit is set to 1, the state machine will reset to its starting state on the next 2.166 MHz clock cycle after the specified duration of the current state has expired.

The assertions word for each state specifies the logic level of each of the control signals. There are a total of 16 control signals, some of which are output from the IA, while others are only used internally. Table 3 specifies the function of each of the control signals and the IA output pin for each signal, if applicable.

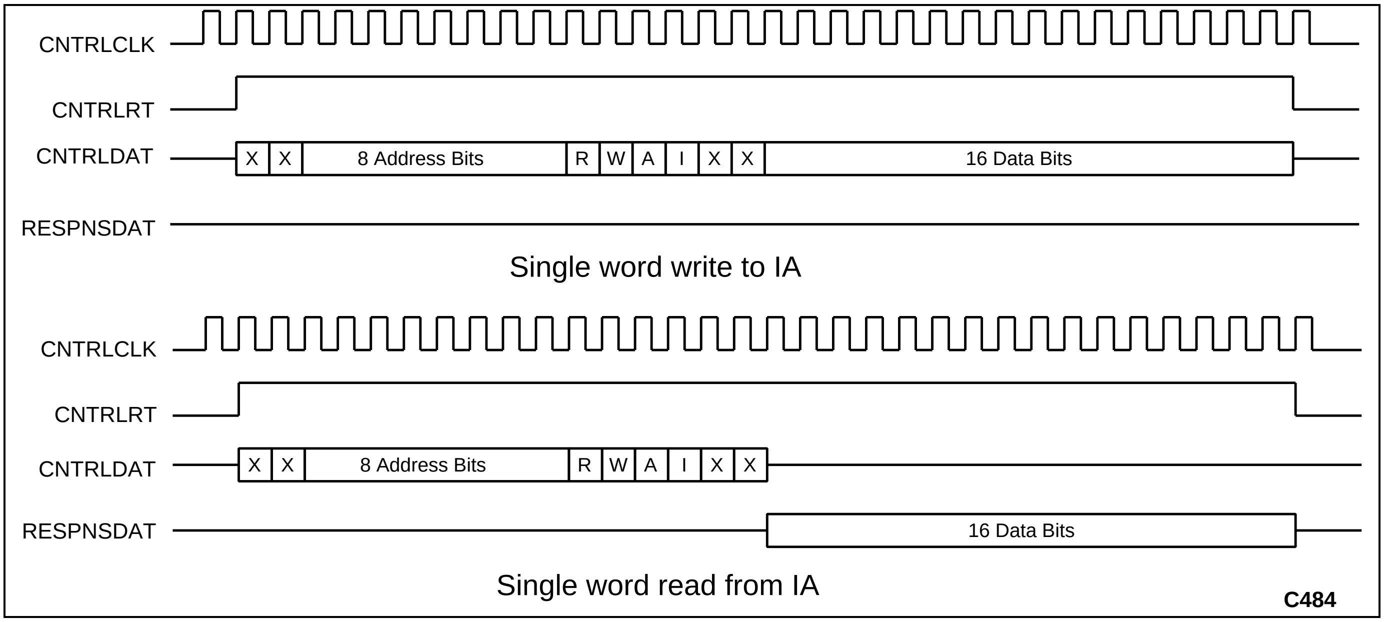

Figure 5. Control Interface Read And Write Timing Diagram

Table 3. Intra-Frame Sequencer Control Signal Functions

Bit	Pin Name	Function
15	Internal only	Initiates auxiliary ADC conversion
14	Internal only	Enables internal Tx path
13	TX_EN_1	Control signal 1 which may be used by the RF subsystem to enable a section of the transmitter
12	TX_EN_2	Control signal 2 which may be used by the RF subsystem to enable a section of the transmitter
11	Internal only	Together with bit 2, enables the ramp profile stored in the ramp store on the TX_PWR_P and TX_PWR_M pins
10	TX_EN_0 / RXEN0	The value of this bit is routed to TX_EN_0 or RXEN0 depending on bit [1] in the Master Enables register
9	Internal only	Selects between Rx and Monitor slots
8	TX_RX	Selects between Transmit and Receive slots
7	Internal only	Enables internal Rx path
6	RXEN1	Control signal 1 which may be used by the RF subsystem to enable a section of the receiver
5	RXEN2	Control signal 2 which may be used by the RF subsystem to enable a section of the receiver
4	SYNEN	Enables RF frequency synthesizer
3	Internal only	Together with bit 2, enables contents of synthesizer sequencer to be output on the synthesizer control serial interface
2	Internal only	Together with bit 11, enables the ramp profile stored in the ramp store on the TX_PWR_P and TX_PWR_M pins Together with bit 3, enables contents of synthesizer sequencer to be output on the synthesizer control serial interface Enables output from gain store to be output on Rx gain control pins Enables PGA gain setting in the IA Rx chain Sets HIGHBAND output at the correct level to select GSM or DCS1800 band
1	SYN_FAST	Control signal for RF frequency synthesizer
0	FRAME_RT	Frame rate signal for use by Conexant BP

Synthesizer Sequencer

The synthesizer sequencer is a programmable state machine that can be configured using the control interface. Each state in the sequencer consists of two 16-bit words. The data can be used to program the frequency synthesizer device in the RF subsystem or to configure the operation of an RF transceiver device. The sequencer RAM is comprised of 16×16-bit words. The sequencer RAM is located at IA register addresses 0x60 to 0x6F, Table 2.

The operation of the synthesizer sequencer is controlled by signals from the IFS. When bit 2 from the IFS is set to 0, the synthesizer sequencer is reset to its starting state. The sequencer remains in this state as long as bit 2 is set to 0.

If bit 2 is set to 1 (reset released) and bit 3 is set to 1, the synthesizer sequencer starts to send the first state of the sequencer over the synthesizer interface. Of the 32 bits stored in the first state, 24 are sent over the interface. After the 24 bits have been sent, the sequencer counts 8 serial interface bit periods.

When the count expires, the state of IFS bit 3 is checked. If it is still set to 1, an additional 24 bits from the next state of the synthesizer sequencer are sent through the synthesizer interface. If bit 3 is set to 0, the sequencer waits until bit 3 is set to 1 again before proceeding to the next sequencer state.

For each synthesizer state, a 24-bit data sequence (bits 31–8) is sent out on the synthesizer interface. This data may be a command for an RF frequency synthesizer device to set up the required frequency for a transmit, receive, or monitor slot. The data may also be a command to configure the operation of one of the RF subsystem devices.

The 32-bit data for each state also controls other IA circuits and outputs. If bit 31 is set to 1, SYNFRM_1 on the synthesizer interface is asserted (set low) while the 24-bit data is being sent out on the synthesizer interface. Conversely, if bit 31 is set to 0, SYNFRM_0 on the synthesizer interface is asserted (set low) while the 24-bit data is being sent out on the synthesizer interface.

If bit 2 is set to 1, bits 30–22 update the receiver gain settings in the IA. Bits 30–28 are output as RXGAIN2, RXGAIN1, and RXGAIN0, respectively. Bits 27–22 are used to set the gain of the Programmable Gain Amplifier (PGA) in the IA receiver path.

Bits 1–0 determine the state of the HIGHBAND output from the IA. The HIGHBAND signal can be used by the RF subsystem to select either the GSM or DCS frequency band. If bits 1–0 = 10b, the HIGHBAND output signal is set high. If bits 1–0 = 01b, the HIGHBAND output signal is set low. If bits 1–0 = 00b, the HIGHBAND signal stays at its previous value.

Synthesizer Interface

The synthesizer interface is a four-wire serial interface for communication between the IA and RF subsystem. The interface is a high speed, synchronous, simplex serial communications link. The synthesizer sequencer provides the data that is sent out on the synthesizer interface.

The four synthesizer interface signals are:

- SYN_CLK: 4.3 MHz output clock signal.
- SYNFRM_0: 135.4 kHz output framing signal. This signal remains low for 24 SYN_CLK periods if the MSB of the data word is set to 0.
- SYNFRM_1: 135.4 kHz output framing signal. This signal remains low for 24 SYN_CLK periods if the MSB of the data word is set to 1.
- SYN_DATA: Serial output data. The bit rate is 4.3 MHz. Each data word sent over the interface is 24 bits long. Eight padding bits are appended to the data word to give a frame rate of 135.4 kHz.

Typically, the synthesizer interface is used to send tuning data from the IA to the RF subsystem frequency synthesizer. Each time the RF subsystem has to tune to a new frequency (for transmit, receive, or monitor slots), a command is sent over the synthesizer interface to configure the RF subsystem synthesizer.

Figure 6 shows the timing diagram for the synthesizer interface.

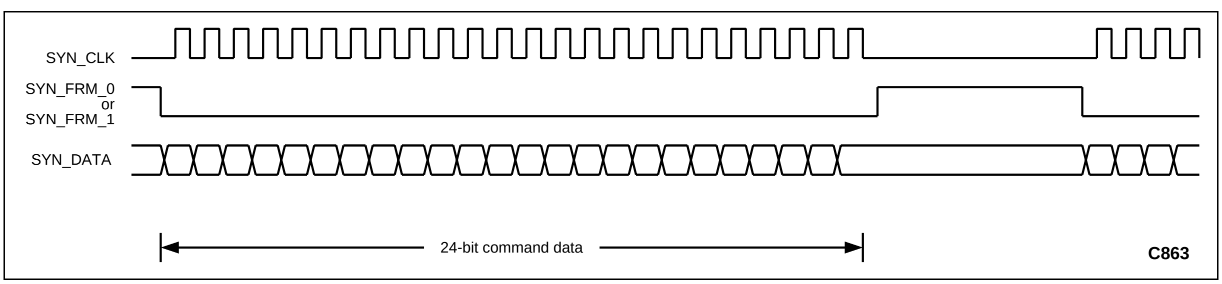

Figure 6. Synthesizer Interface Timing Diagram

Receiver

The IA receiver amplifies the received differential IF signal and converts the analog signal into digital samples for processing by the BP. The received signal is AC-coupled on the IA.

The IA receiver path consists of the following blocks:

- Programmable Gain Amplifier
- Bandpass ADC
- Receive Interface

Programmable Gain Amplifier (PGA). The PGA amplifies the IF input signal on the RX_IF pins. The received IF signal frequency is 14.6 MHz. The gain of the PGA is programmable in

6 dB steps from 0 dB to 36 dB, as specified in Table 4. The gain is controlled by bits 11–6 in the Synthesizer Sequencer.

Table 4. Receiver Programmable Gain Amplifier Settings

Synthesizer Sequencer Bits 11–6	PGA Gain Setting (dB)
000000	0
000100	6
010100	12
100100	18
101000	24
101001	30
101010	36
all other bit settings	undefined

Bandpass ADC. The Bandpass Sigma-Delta (Σ–Δ) ADC samples the amplified IF signal from the PGA at a rate of 19.5 Msps. The digital samples produced by the ADC are a quadrature baseband representation of the IF input signal. The ADC uses Σ–Δ technology to generate high resolution 12-bit samples. The 12-bit samples are left-justified in 16-bit words.

The In-Phase/Quadrature (I/Q) samples produced are output from the ADC at a rate of 1.083 Msps. This corresponds to an I/Q pair sample rate of 540 ksps, which is twice the GSM bit rate of 270 kbps.

Receive Interface. I/Q samples generated by the ADC are sent out from the IA on the Receive Interface. The Receive Interface is a three-wire serial interface that is designed to interface between the IA and BP. The interface is a high speed, synchronous, simplex, serial communications link. The interface signals are:

- RX_CLOCK: 19.5 MHz output clock.
- RX_RATE: 1.083 MHz output clock that indicates the start of a word on the RX_DATA output. The pulse width of the RX_RATE clock is one bit period.
- RX_DATA: Serial output data. The data rate is 19.5 Mbps.

Figure 7 shows the Receive Interface timing diagram.

The receive interface serial output data rate is 19.5 Mbps. The data changes state on the rising edge of the clock signal. Each I or Q sample is 16 bits wide with two stuff bits between samples. The RX_RATE signal indicates when a new I or Q sample is starting.

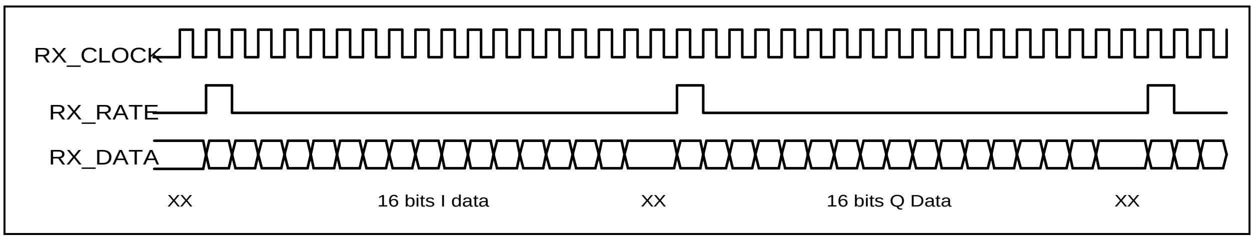

Figure 7. Receive Interface Timing Diagram

Transmitter

The IA transmitter buffers the baseband transmit data, performs GMSK modulation of the data and generates analog I/Q output signals for the RF subsystem.

The IA Transmitter path contains the following blocks:

- Burst Store RAM
- GMSK Modulator
- I/Q DACs
- I/Q Reconstruction Filters

Burst Store RAM. The Burst Store RAM is used to store the transmit data. The Burst Store RAM consists of a bank of 12×16-bit registers, which is written to using the IA Control Interface. The starting address of the Burst Store RAM is specified in Table 2. When the IFS bit 14 = 1, the contents of the Burst Store RAM are shifted out serially to the GMSK modulator. As long as bit 14 remains set to 1, data continues to be shifted out to the GMSK modulator. The data is shifted out starting with the word in the lowest address of the Burst Store RAM, most significant bit first. The serial output rate is 270.83 kbps.

GMSK Modulator. The GMSK modulator performs the modulation of the serial data stream from the Burst Store RAM and generates I and Q data samples. During the transmit slot of the TDMA frame, the I and Q data are generated at a rate of 4.33 Msps (16 times the input data rate). Each sample is a 10-bit word. The I and Q samples are the complex representation of the GMSK waveform.

I/Q DACs. The I/Q DACs convert the I and Q samples, from the GMSK modulator, from digital samples to analog signals. The conversion rate is 4.33 Msps, the same as the data rate of the GMSK Modulator output.

Reconstruction Filters. The Reconstruction Filters provide lowpass filtering of the analog I and Q signals from the I/Q

DACs. The output of the reconstruction filters are continuous time I and Q signals. The differential I and Q outputs are available at the TX_I_P/TX_I_M and TX_Q_P/TX_Q_M pins of the IA.

I/Q DC Offset and Gain Imbalance Adjust. The IA provides adjustments to minimize the DC offset and gain imbalance between the I and Q transmit channels. This adjustment may be used to compensate for offsets and imbalances introduced in the RF subsystem.

I/Q DC Offset Adjust. The Tx Offset Register is used to store the I/Q DC offset adjustment value. For both I and Q channels the contents of this 8-bit register are added to the 10-bit samples from the modulator to generate the DC compensated samples. If no DC compensation is required, the registers are loaded with 0s. Bits 15–8 contain the I channel DC offset adjustment value, and bits 7–0 contain the Q channel DC offset adjustment value. The Tx Offset Register is located at address 0x7C (Table 2).

Gain Imbalance Adjust. Gain mismatch between the I and Q transmit channels in the RF Subsystem can be compensated for in the IA using the Tx I/Q Control Register. Bits 5–1 contain the I/Q channel relative gain adjustment value. The Tx I/Q Control Register is located at address 0x7D (Table 2).

Tx Power Control

The IA generates a differential signal to control the output power level of the handset Power Amplifier (PA). The Tx Power Control circuitry in the IA consists of the following blocks:

- Ramp Store
- Power Control DAC

Ramp Store Memory. The Ramp Store Memory is a bank of RAM consisting of 32×16-bit words. The Control Port is used to write to the Ramp Store Memory, located at addresses 0x40 to 0x5F. At the start of a transmit slot, the PA output power must be ramped up to the required transmit power level. At the end of the transmit slot, the PA output power must be ramped back down. The ramping profile is stored in the Ramp Store Memory.

Bit 2 and bit 11 of the IFS register enable the output from the Ramp Store Memory. When bit 2 and bit 11 are set to 1 for the first time, words 0–m in the Ramp Store Memory are sequentially sent out to generate the rising edge of the ramp profile. When bit 2 and bit 11 are set to 1 for the second time, words (m + 1) through n in the Ramp Store Memory are sequentially sent out to generate the falling edge of the ramp profile. The number of words, that is, the values of m and n, used to create the rising and falling edges depend on the duration of each state in the IFS.

Bits 15–6 of each word specify the power level for that state. Bits 5–0 specify the duration of the state, as a number of 2.167 MHz clock cycles. 2.167 MHz is 8 times the system bit rate (270.833 kbps).

Power Control DAC. The Ramp Store outputs 10-bit data samples to the Power Control DAC. The Power Control DAC is a 10-bit DAC that converts the samples it receives from the Ramp Store into a differential analog signal that is output from the IA device. The differential signal is used to control the PA output power.

Voiceband Codec

The Voiceband Codec consists of the following:

- Encoder
- Decoder
- Codec Interface

Encoder. The Encoder converts analog speech signals from the handset microphone into digital samples for processing. The digitized samples are sent to the BP over the Codec Interface.

The Encoder block is comprised of:

- Input Buffer/PGA
- Low Pass Filters
- Σ–Δ ADC
- Digital Filter

Input Buffer and Programmable Gain Amplifier. A fixed gain amplifier is used to buffer the LINEIN signal. A PGA is used to buffer the MIC input signal. The buffered LINEIN and MIC input signals are multiplexed to the input of the encoder. The LINEIN input is selected by writing a logic 1 to bit 13 of the Encoder Control Register. The MIC input is selected by writing to bit 12 of the Encoder Control Register.

The LINEIN signal is a differential input. The input buffer has a fixed gain of 6 dB. The maximum LINEIN signal level is 0.53 V_{rms}.

The MIC input is a differential input. The PGA provides gain from 6 dB to 41 dB. The maximum input signal level depends on the gain setting. At each gain setting, the maximum input signal level results in an input to the Encoder ADC whose root mean square (rms) value is 6.02 dB below that of the full-scale input of the ADC. PGA gain is configured by writing to bits 11–9 of the Encoder Control Register. The Encoder Control Register address is specified in Table 2. Table 5 specifies the maximum input level for each of the gain settings and the value of bits 11–9 for each gain setting.

Table 5. PGA Gain Settings

PGA Gain Setting	Encoder Control Register Bits 11–9	Input Level V_{rms}
6	000	0.500
23	001	0.071
26	010	0.050
29	011	0.035
32	100	0.025
35	101	0.018
38	110	0.013
41	111	0.009

The IA provides a clean bias voltage for the handset microphone. The MIC_BIAS signal level is 2.2 V ± 10 mV and can provide up to 1.5 mA of current.

Low Pass Filters. Each of the input paths (LINEIN and MIC) has an anti-aliasing lowpass filter, which removes unwanted frequency components from the input signal. The 3 dB cutoff frequency of each filter is typically 100 kHz.

Σ–Δ ADC. The outputs of the LINEIN and MIC anti-aliasing filters are multiplexed at the ADC input. The value of Encoder Control Register bits 13–12 selects the ADC input signal. The Σ–Δ ADC converts the input analog signal to digital samples. The ADC samples the input signal at a rate of 2 Msps, and generates a 1-bit serial data stream.

Encoder Digital Filter. A digital filter in the encoder filters the serial data stream from the ADC and generates a 13-bit sample word, in two's complement form, at a rate of 8 ksps. These output samples are sent from the IA to the BP using the Codec Interface.

Encoder Control Register. Encoder Control Register contents control Encoder operation. Table 6 describes Encoder Control Register bit functions. The Encoder Control Register address is specified in Table 2.

Decoder. The IA Decoder receives digital samples over the Codec Interface, and converts the samples to an analog signal. This signal is output from the IA on one of the two analog outputs. The output signal is used to drive an audio transducer such as the handset speaker.

Table 6. Encoder Control Register

Bit	Function
15–14	Enable Encoder 00: Encoder disabled 01: Reserved 10: Reserved 11: Encoder enabled
13	Enable LINEIN input 0: disabled 1: enabled
12	Enable MIC input 0: disabled 1: enabled
11–9	Select gain of MIC input PGA 000: 6 dB 001: 23 dB 010: 26 dB 011: 29 dB 100: 32 dB 101: 35 dB 110: 38 dB 111: 41 dB
8–0	Reserved

The Decoder consists of the following devices:

- Digital Filter
- Σ–Δ DAC
- Low Pass Filter
- Output Buffers

Decoder Digital Filter. A digital filter in the decoder filters the digitized samples and generates a 1-bit serial data stream. The digital filter receives samples from the BP over the Codec Interface. The input samples to the filter are 16-bit, two's-complement words. The input sample rate is 8 ksps. The output of the lowpass filter is a 1-bit serial data stream that is used as the input to the Σ–Δ DAC. The digital filter incorporates an optional gain stage. The gain is set by writing to bits 13–12 of the Decoder Control register. The address of the Decoder Control register is specified in Table 2. The gain settings of the Decoder Digital filter are specified in Table 7.

Σ–Δ DAC. A Σ–Δ Decoder DAC is used to generate an analog output signal from the 1-bit serial data stream from the decoder digital filter. The DAC incorporates an optional 6 dB gain stage. The gain stage is enabled by writing a logic 1 to bit 9 of the Decoder Control register. The address of the Decoder Control register is specified in Table 2.

Table 7. Decoder Control Register

Bit	Function
15–14	Enable Decoder 00: Decoder disabled 01: Reserved 10: Reserved 11: Decoder enabled
13–12	Digital Filter gain 00: 0 dB 01: +6 dB 10: –6 dB 11: Reserved
11	Reserved
10	Enable SPKR output 0: disabled 1: enabled
9	D/A Gain 0: 0 dB 1: 6 dB
8	Enable LINEO output 0: disabled 1: enabled
7–0	Reserved

Lowpass Filter. The Decoder Lowpass Filter is a reconstruction filter that smoothes the output signal from the decoder DAC.

Output Buffers. The decoder output buffers are used to drive the output signals from the lowpass filter out to the LINEO_P/LINEO_M and SPKR_P/SPKR_M pins. The LINEO output is enabled by writing a logic 1 to bit 8 of the Decoder Control register. The SPKR output is selected by writing a logic 1 to bit 10 of the Decoder Control register. The Decoder Control Register address is specified in Table 2.

The LINEO output is a differential output. The maximum output signal level is 4 Vp-p into a differential resistive load of 2 kΩ.

The SPKR output is a differential output, which is designed to drive a handset speaker. The maximum output signal level is 4 Vp-p into a differential resistive load of 600 Ω or 2 Vp-p into a differential resistive load of 150 Ω.

Decoder Control Register. The Decoder Control Register is used to control the operation of the Decoder. Table 7 describes the function of each bit in the Decoder Control Register. The address of the Decoder Control Register is specified in Table 2.

Codec Interface

The Codec Interface is a four-wire serial interface that is designed to interface between the IA and Conexant's Baseband Processor (BP). The interface is a high speed, synchronous, full duplex, serial communications link. The interface is connected to the Voiceband Codec on the IA.

The interface signals are:

- CDCCLK: 4 MHz interface clock output.
- CDCRATE: 8 kHz framing signal output.
- ENCDRDAT: Serial data output. The bit rate is the same as the CDCCLK rate (4 Mbps). The word rate is the same as the CDCRATE signal (8 kwps). Words are 16 bits wide.
- DCDRDAT: Serial data input. The bit rate is the same as the CDCCLK rate (4 Mbps). The word rate is the same as the CDCRATE signal (8 kwps). Words are 16 bits wide.

The operation of the Codec Interface during a voice call is as follows:

1. Digitized audio samples are received from the BP over the Codec Interface. The Decoder converts digitized samples to an analog signal, which is used to drive the handset speaker or the Line Out signal.
4. The Codec converts the analog signal from the handset MIC or LINEIN input into digital samples. These samples are sent from the IA to the BP over the Codec Interface.

Figure 8 shows the timing diagram for the IA Codec Interface.

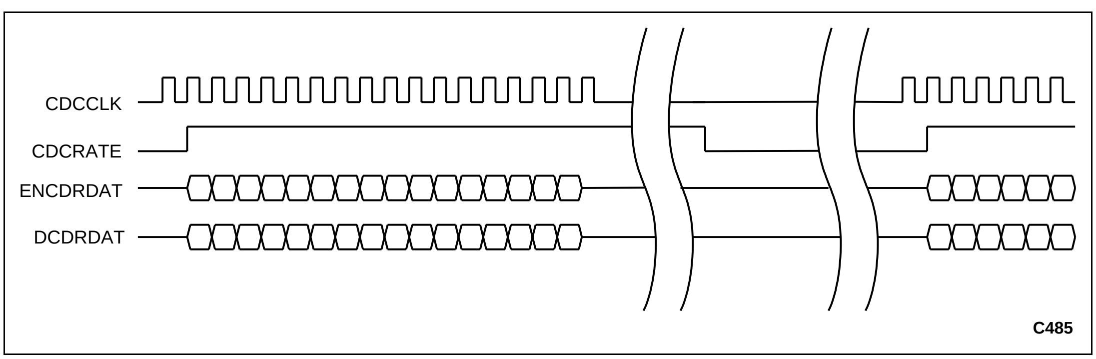

Figure 8. IA Codec Interface Timing Diagram

Auxiliary ADC

The Auxiliary ADC is a general purpose 8-bit ADC with the following two external inputs that are used for monitoring system signals such as handset temperature or handset battery voltage.

- AUXADC1. A single-ended input
- AUXADC2P/AUXADC2M. Differential inputs

Each time the Auxiliary ADC is enabled, a single conversion is performed and the 8-bit, two's-complement result is placed in bits 15–8 of the Auxiliary ADC register. The ADC is enabled whenever bit 15 output from the IFS transitions from 0 to 1. The address of the Auxiliary ADC register is specified in Table 2.

Auxiliary ADC Registers. The Auxiliary ADC register stores the ADC 8-bit output. The function of each bit in the register is described in Figure 8. The addresses of the Auxiliary ADC Registers are specified in Table 2.

The Auxiliary ADC register also stores the logic levels of the STATUS1 and STATUS2 pins. The register can be read to determine the logic level of the pins.

Table 8. Auxiliary ADC Register

Bit	Function
15–8	Two's-complement output from Auxiliary ADC
7–3	Reserved
2	Level of STATUS2 pin
1	Level of STATUS1 pin
0	Reserved

The Auxiliary ADC Input Select Register selects either the AUXADC1 or AUXADC2 as the input to the Auxiliary ADC. The function of each bit in the register is described in Table 9.

Table 9. Auxiliary ADC Input Select Register

Bit	Function
15–13	ADC Input Select 000: AUXADC2 001: AUXADC1 010–111: Reserved
12–0	Reserved

Electrical and Mechanical Specifications

The absolute maximum ratings of the 20420 IA device are provided in Table 10, the recommended operating conditions are specified in

Table 11, and the electrical characteristics are specified in Table 12. Table 13 provides the electrical specifications for the 19.5 MHz crystal. Figure 9 shows a block diagram for a typical application. Figure 10 provides the package dimensions for the 100-pin CABGA. Figure 11 shows the shipping tray dimensions.

ESD Sensitivity

Caution. The 20420 is an Electrostatic Discharge (ESD) static-sensitive electronic device. The human body and test equipment can build electrostatic charges that can discharge without detection.

Do not operate or store 20420 devices near strong electrostatic fields. Permanent damage may occur. Take proper ESD precautions.

Table 10. IA Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply voltage	V_{dd}	−0.5 to +6.0	V
Input voltage	V_{in}	(V_{SS} – 0.3) to (V_{DD} + 0.3)	V
Analog inputs	V_{in}	(V_{SS} – 0.3) to (V_{DD} + 0.3)	V
DC input clamp current	I_{ik}	±10	mA
DC output clamp current	I_{ok}	±50	mA
Static discharge voltage (25 °C)	V_{esd}	Human Body Model: ±2500 Charged Device Model: ±200	V
Latch-up current (25 °C)	I_{trig}	±150	mA
Storage temperature range	T_{stg}	−55 to +150	°C
Note: Voltages referenced to ground (V_{SS}).			

Table 11. IA Recommended Operating Conditions

Parameter	Symbol	Limits	Units
Supply voltage	V_{DD}	+2.7 to +3.6	V
Operating ambient temperature range	T_A	−40 to +85	°C

Table 12. IA Electrical Characteristics (1 of 2)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Analog Inputs						
Receive IF Inputs (RX_IF_P / RX_IF_M)						
Differential Input Signal Level					2.5	Vp-p
Input Frequency				14.6		MHz
Differential Input Resistance				20	25	kΩ
Differential Input Capacitance			10		15	pF
Microphone Input (MIC_P / MIC_M)						
Differential Input Signal Level		PGA gain = 6 dB		0.500		V_{RMS}
		PGA gain = 23 dB		0.071		V_{RMS}
		PGA gain = 26 dB		0.050		V_{RMS}
		PGA gain = 29 dB		0.035		V_{RMS}
		PGA gain = 32 dB		0.025		V_{RMS}
		PGA gain = 35 dB		0.018		V_{RMS}
		PGA gain = 38 dB		0.013		V_{RMS}
		PGA gain = 41 dB		0.009		V_{RMS}
Input Impedance		PGA gain = 6 dB (note 2)	43	250		kΩ
		PGA gain = 41 dB (note 2)		38		kΩ
Line Input (LINEIN_P / LINEIN_M)						
Differential Input Signal Level				0.53		V_{RMS}
Single-ended Input Impedance				150		kΩ
Current Bias Resistor (RBIAS)		Resistor connected to ground	119.8	121	122.2	kΩ
Auxiliary ADC 1 Input (AUXADC1)						
Input Voltage			0		V_{DD}	V
Auxiliary ADC 2 Input (AUXADC2P / AUXADC2M)						
Input Signal Level			0		V_{DD}	V
Differential Input Signal Level					4.0	Vp-p
Input Common Mode Voltage			0		2.0	V
Differential Input Impedance			2			MΩ
Transmit I/Q Outputs (TX_I_P / TX_I_M and TX_Q_P / TX_Q_M)						
Differential Output Signal Level		No load connected	0.98	1.0	1.02	V
Common Mode Voltage			1.34	1.35	1.36	V
Differential Load Resistance			20			kΩ
Differential Load Capacitance					20	pF
Output Impedance			1.6	2	2.4	kΩ
Transmit Power Control (TX_PWR_P / TX_PWR_M)						
Differential Output Signal Level					4.0	V
Common Mode Voltage				1.35		V
Differential Load Resistance			20			kΩ
Differential Load Capacitance					10	pF
Output Impedance			1.6	2	2.4	kΩ
Speaker Output (SPKR_P / SPKR_M)						
Differential Output Signal Level		R_L = 600 Ω			4	Vp-p
		R_L = 150 Ω			2	Vp-p
Line Output (LINEO_P / LINEO_M)						
Differential Output Signal Level		R_L = 2 kΩ			4	Vp-p

Table 12. IA Electrical Characteristics (2 of 2)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Analog Outputs (continued)						
Microphone Bias Voltage (MIC_BIAS) Bias Voltage Source Current			 2.150	 2.2	 2.250 1.5	 V mA
Synthesizer Reference Clock (SYNREF19) Frequency Signal Level Load			 0.7	 19.5 1.0 see Figure 4	 1.3	 MHz V
Internal Voltage Reference (VREF)		0.1 µF cap. to ground required	2.34	2.35	2.36	V
Internal Bias Reference Voltage (VREFC)		0.1 µF cap. to ground required	1.34	1.35	1.36	V
Internal Codec Reference Voltage (CDCVREF)		0.1 µF cap. to ground required	2.34	2.35	2.36	V
Internal Codec Bias Reference Voltage (CDCVREFC)		0.1 µF cap. to ground required	1.34	1.35	1.36	V
Digital Signals						
Input high voltage	V_{IH}	V_{DD} = 3.0 V	$0.8 \times V_{DD}$			V
Input low voltage	V_{IL}	V_{DD} = 3.0 V			0.4	V
Output high voltage	V_{OH}	V_{DD} = 3.0 V, sourcing 100 µA	$0.8 \times V_{DD}$			V
Output low voltage	V_{OH}	V_{DD} = 3.0 V, sinking 1.6 mA			0.4	V
Input capacitance (inputs)	C_{IN}	V_{DD} = 3.0 V			5	pF
Capacitive load (outputs)	C_L	V_{DD} = 3.0 V			20	pF
System Clock						
3.9 MHz Clock Output High voltage Output Low voltage	 V_{OH} V_{OL}	 I_{OH} = 100 µA I_{OL} = 1.6 mA	 2.4		 0.4	 V V

Notes:
1. All voltages referenced to ground (V_{SS}). Currents are positive when flowing into the device.
2. Single-ended measurement.

Table 13. Specifications for 19.5 MHz Crystal

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drive Level				75		µW
Load Capacitance	C_{LD}	Load capacitance is variable and is used for frequency tuning	7.0	10.2	15.0	pF
Nominal Resonant Frequency		C_{LD} = 10.2 pF Temperature = 25 °C		19.5		MHz
Frequency Stability Initial Tolerance Temperature Drift Aging Drift		 C_{LD} = 10.2 pF Temperature = 25 °C –30°C to +70 °C Over 5 years	 –10 –12 –5		 +10 +12 +5	 ppm ppm ppm
Crystal Parameters Motional Inductance Motional Capacitance Series Resistance Shunt Capacitance		 C_{LD} = 10.2 pF		 3.3 20 15 4.3		 mH ff Ω pF

Notes:
The fundamental oscillation mode of the crystal is used, and the crystal is a parallel type.
The crystal is expected to be pulled back to its nominal operating frequency given its specified frequency stability and specified extremes in load capacitance range.

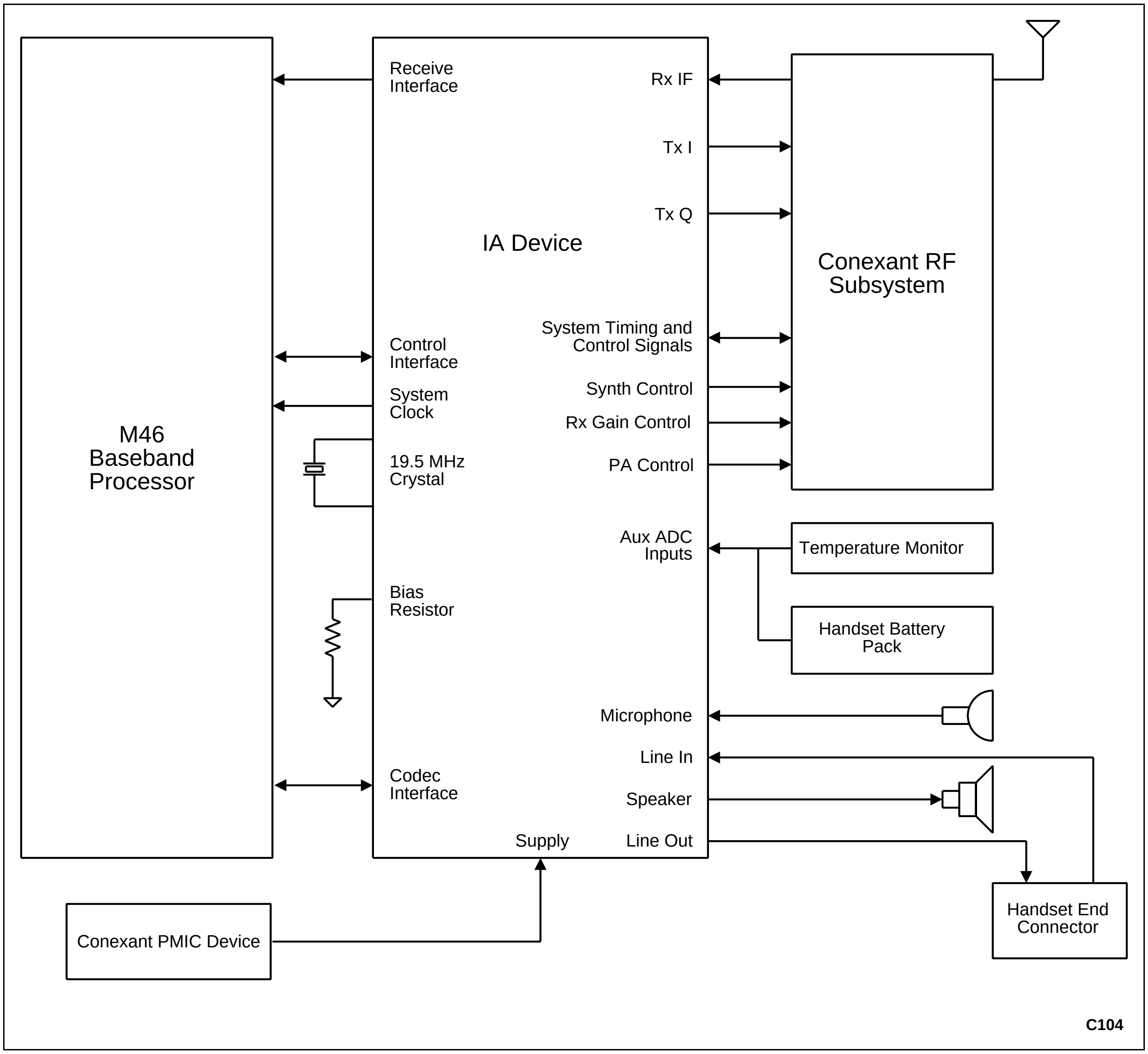

Figure 9. Typical IA Device Application Block Diagram

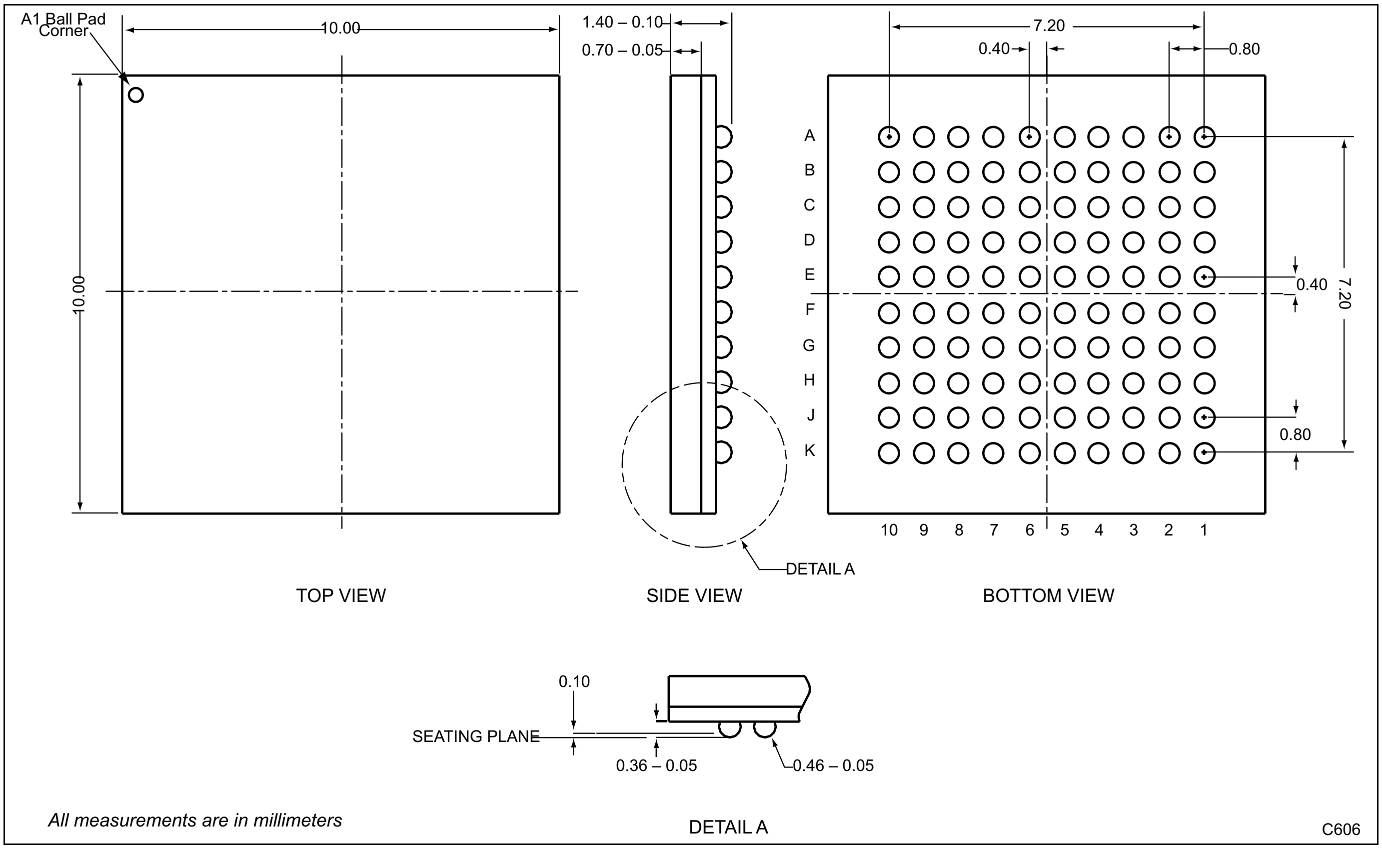

Figure 10. IA Device 100-Pin CABGA Package Dimension Drawing

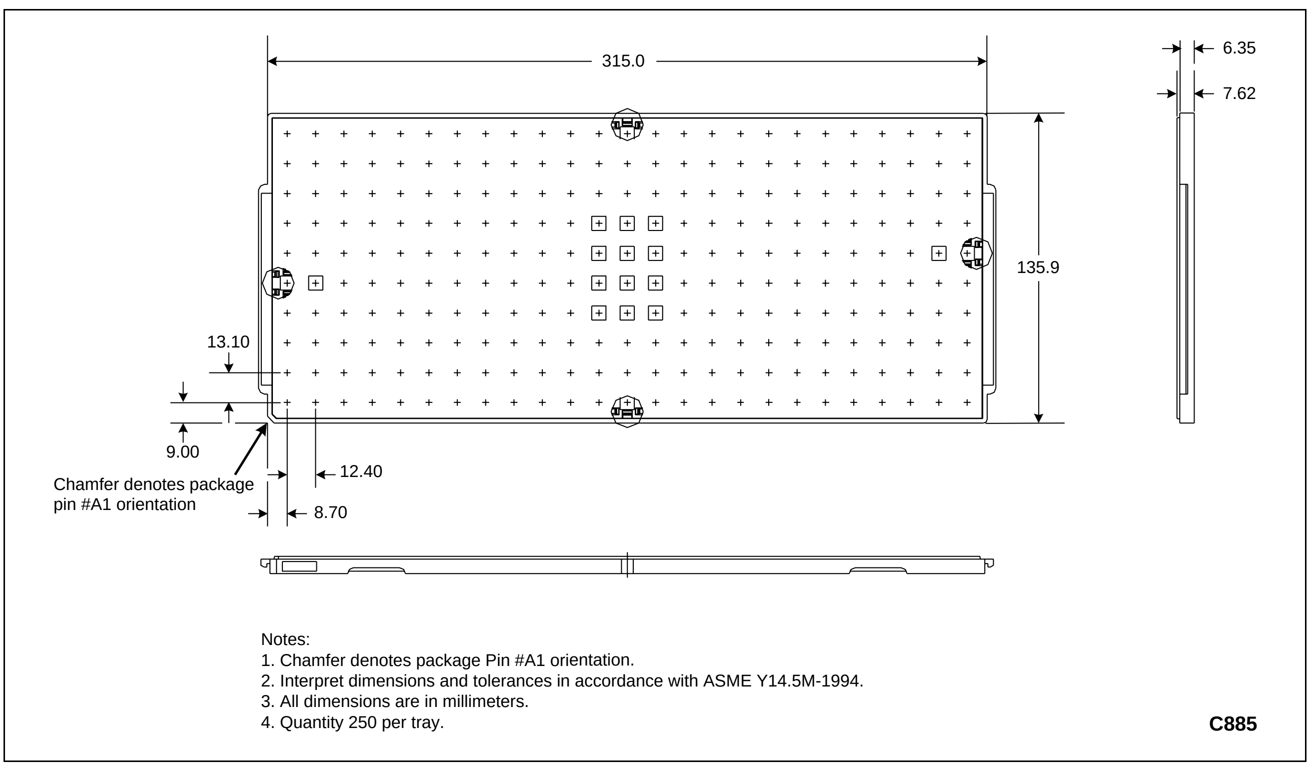

Figure 11. 20420 Shipping Tray Dimensions

Ordering Information

Model Name	Manufacturing Part Number
20420 Integrated Analog 100-pin CABGA	20420

Further Information
literature@conexant.com
(800) 854-8099 (North America)
(949) 483-6996 (International)
Printed in USA

World Headquarters
Conexant Systems, Inc.
4311 Jamboree Road
Newport Beach, CA
92660-3007
Phone: (949) 483-4600
Fax 1: (949) 483-4078
Fax 2: (949) 483-4391

Americas

U.S. Northwest/
Pacific Northwest – Santa Clara
Phone: (408) 249-9696
Fax: (408) 249-7113

U.S. Southwest – Los Angeles
Phone: (805) 376-0559
Fax: (805) 376-8180

U.S. Southwest – Orange County
Phone: (949) 483-9119
Fax: (949) 483-9090

U.S. Southwest – San Diego
Phone: (858) 713-3374
Fax: (858) 713-4001

U.S. North Central – Illinois
Phone: (630) 773-3454
Fax: (630) 773-3907

U.S. South Central – Texas
Phone: (972) 733-0723
Fax: (972) 407-0639

U.S. Northeast – Massachusetts
Phone: (978) 367-3200
Fax: (978) 256-6868

U.S. Southeast – North Carolina
Phone: (919) 858-9110
Fax: (919) 858-8669

U.S. Southeast – Florida/ South America
Phone: (727) 799-8406
Fax: (727) 799-8306

U.S. Mid-Atlantic – Pennsylvania
Phone: (215) 244-6784
Fax: (215) 244-9292

Canada – Ontario
Phone: (613) 271-2358
Fax: (613) 271-2359

Europe

Europe Central – Germany
Phone: +49 89 829-1320
Fax: +49 89 834-2734

Europe North – England
Phone: +44 1344 486444
Fax: +44 1344 486555

Europe – Israel/Greece
Phone: +972 9 9524000
Fax: +972 9 9573732

Europe South – France
Phone: +33 1 41 44 36 51
Fax: +33 1 41 44 36 90

Europe Mediterranean – Italy
Phone: +39 02 93179911
Fax: +39 02 93179913

Europe – Sweden
Phone: +46 (0) 8 5091 4319
Fax: +46 (0) 8 590 041 10

Europe – Finland
Phone: +358 (0) 9 85 666 435
Fax: +358 (0) 9 85 666 220

Asia – Pacific

Taiwan
Phone: (886-2) 2-720-0282
Fax: (886-2) 2-757-6760

Australia
Phone: (61-2) 9869 4088
Fax: (61-2) 9869 4077

China – Central
Phone: 86-21-6361-2515
Fax: 86-21-6361-2516

China – South
Phone: (852) 2 827-0181
Fax: (852) 2 827-6488

China – South (Satellite)
Phone: (86) 755-518-2495

China – North
Phone: (86-10) 8529-9777
Fax: (86-10) 8529-9778

India
Phone: (91-11) 692-4789
Fax: (91-11) 692-4712

Korea
Phone: (82-2) 565-2880
Fax: (82-2) 565-1440

Korea (Satellite)
Phone: (82-53) 745-2880
Fax: (82-53) 745-1440

Singapore
Phone: (65) 737 7355
Fax: (65) 737 9077

Japan
Phone: (81-3) 5371 1520
Fax: (81-3) 5371 1501

CONEXANT™
What's next in communications technologies™