Microprocessor With Clock and RAM

GOULD Electronics

S6802/A/B/S6808/A/B

Features

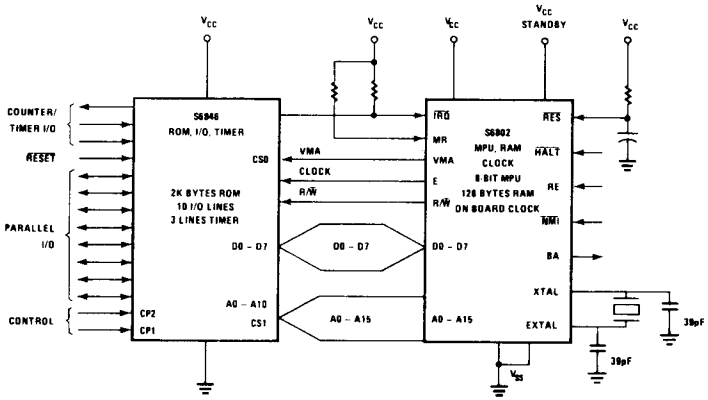
- ☐ On-Chip Clock Circuit
- ☐ 128x8-Bit On-Chip RAM (S6802)
- ☐ 32 Bytes of RAM Are Retainable (S6802)
- ☐ Software-Compatible With the S6800
- ☐ Expandable to 64K Words
- ☐ Standard TTL-Compatible Inputs and Outputs
- ☐ 8-Bit Word Size
- ☐ 16-Bit Memory Addressing
- ☐ Interrupt Capability
- ☐ Clock Rates:
  S6802/S6808—1.0MHz
  S68A02/S68A08—1.5MHz
  S68B02/S68B08—2.0MHz

General Description

The S6802/S6808 are monolithic 8-bit microprocessors that contain all the registers and accumulators of the present S6800 plus an internal clock oscillator and driver on the same chip. In addition, the S6802 has 128 bytes of RAM on board located at hex addresses 0000 to 007E. The first 32 bytes of RAM, at addresses 0000 to 001F, may be retained in a low power mode by utilizing V_{CC} standby, thus facilitating memory retention during a power-down situation. The S6808 is functionally identical to the S6802 except for the 128 bytes of RAM. The S6808 does not have any RAM.

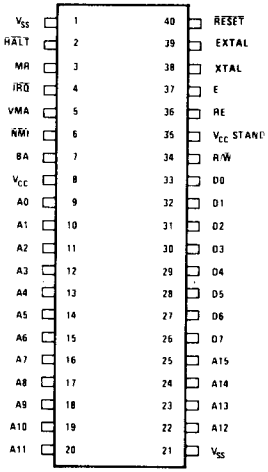
The S6802/S6808 are completely software compatible with the S6800 as well as the entire S6800 family of parts. Hence, the S6802/S6808 are expandable to 64K words. When the S6802 is interfaced with the S6846 ROM-I/O-Timer chip, as shown in the Block Diagram below, a basic 2-chip microcomputer system is realized.

Typical Microcomputer Block Diagram



BLOCK DIAGRAM OF A TYPICAL COST EFFECTIVE MICROCOMPUTER. THE MPU IS THE CENTER OF THE MICROCOMPUTER SYSTEM AND IS SHOWN IN A MINIMUM SYSTEM INTERFACING WITH A ROM COMBINATION CHIP. IT IS NOT INTENDED THAT THIS SYSTEM BE LIMITED TO THIS FUNCTION BUT THAT IT BE EXPANDABLE WITH OTHER PARTS IN THE S6800 MICROCOMPUTER FAMILY.

Pin Configuration



S6800 FAMILY

S6802/A/B/S6808/A/B

Absolute Maximum Ratings

Supply Voltage, V_{CC} ..... −0.3V to +7.0V
Input Voltage, V_{IN} ..... −0.3V to +7.0V
Operating Temperature Range, T_A ..... 0° to +70°C
Storage Temperature Range, T_{stg} ..... −55°C to +150°C
Thermal Resistance, θ_{JA}
Plastic ..... 100°C/W
Ceramic ..... 50°C/W

This device contains circuitry to protect the inputs against damage due to high static voltage or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

D.C. Characteristics:

(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter		Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	Logic, EXtal RESET	$V_{SS}+2.0$ $V_{SS}+4.0$	— —	V_{CC} V_{CC}	V
V_{IL}	Input Low Voltage	Logic, EXtal, RESET	$V_{SS}-0.3$	—	$V_{SS}+0.8$	V
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = Max)	Logic*	—	1.0	2.5	μA
V_{OH}	Output High Voltage (I_{LOAD} = −205μA, V_{CC} = Min) (I_{LOAD} = −145μA, V_{CC} = Min) (I_{LOAD} = −100μA, V_{CC} = Min)	 D0–D7 A0–A15, R/W, VMA, E BA	 $V_{SS}+2.4$ $V_{SS}+2.4$ $V_{SS}+2.4$	 — — —	 — — —	V V V V
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mA, V_{CC} = Min)		—	—	$V_{SS}+0.4$	V
P_D	Power Dissipation	(Measured at T_A = 0°C)	—	0.600	1.2	W
C_{IN} C_{OUT}	Capacitance # (V_{IN} = 0, T_A = 25°C, f = 1.0MHz	 D0–D7 Logic Inputs, EXtal A0–A15, R/W, VMA	 — — —	 10 6.5 —	 12.5 10 12	pF pF
V_{CC} Standby	V_{CC}		4.0	—	5.25	V
I_{DD} Standby	I_{DD} Standby		—	—	8.0	mA

Clock Timing (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter	S6802/S6808			S68A02/S68A08			S68B02/S68B08			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f	Frequency of Operation Input Clock ÷ 4	0.1	—	1.0	0.1	—	1.5	.1	—	2	MHz
f_{xtal}	Crystal Frequency	1.0	—	4.0	1.0	—	6.0	1.0	—	8	
t_{CYC}	Cycle Time	1.0	—	10	6.7	—	10	.50	—	10	μs
t_ϕ	Fall Time Measured between $V_{SS}+0.4V$ and $V_{SS}-2.4V$	—	—	25	—	—	25	—	—	25	ns

*Except IRQ and NMI, which require 3KΩ pull-up load resistors for wire-OR capability at optimum operation. Does not include Extal and Xtal, which are crystal inputs.
#Capacitance are periodically sampled rather than 100% tested.

S6802/A/B/S6808/A/B

Read/Write Timing (Figures 1 through 5; Load Circuit of Figure 3.)
(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to + 70°C unless otherwise noted)

Symbol	Parameter	S6802/S6808			S68A02/S68A08			S68B02/S68B08			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{AD}	Address Delay C = 90pF C = 30pF		100	270			180 165			150 135	ns
t_{ACC}	Peripheral Read Access Time	575			360			250			ns
t_{DSR}	Data Setup Time Read	100			70			60			ns
t_{DHR}	Data Hold Time Read	10	30		10			10			ns
t_{AH}	Address Hold Time (Address, R/W, VMA)	20			20			20			ns
t_{DDW}	Data Delay Time Write Processor Controls			225			170			160	ns
t_{DHW}	Data Hold Time Write	30			20			20			ns
t_{PCS}	Processor Control Setup Time	200			140			110			ns
t_{PCr}, t_{PCf}	Processor Control Rise and Fall Time			100			100			100	ns

Figure 1. Read Data from Memory or Peripherals

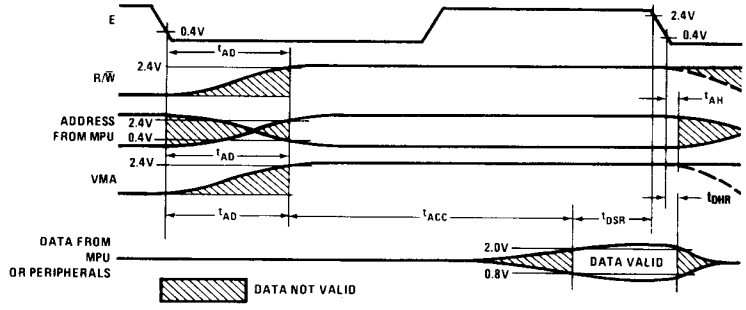


Figure 2. Write Data in Memory or Peripherals

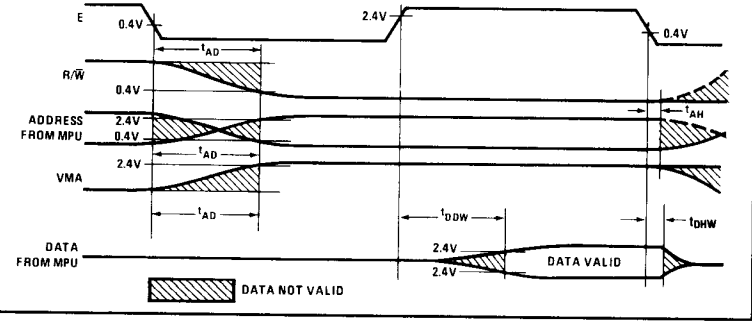
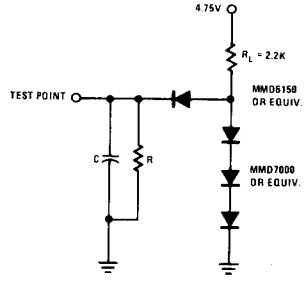


Figure 3. Bus Timing Test Load



C = 130pF FOR D0 – D7, E
= 90pF FOR A0 – A15, R/W, AND VMA
= 30pF FOR BA
R = 11.7 KΩ FOR D0 – D7, E
= 16.5KΩ FOR A0 – A15, R/W, AND VMA
= 24KΩ FOR BA

S6800 FAMILY