HARRIS
SEMICONDUCTOR

# HCTS299MS

## Radiation Hardened 8-Bit Universal Shift Register; Tri-State

December 1992

## Features

- **3 Micron Radiation Hardened CMOS SOS**
- **Total Dose 200K or 1 Mega-RAD (Si)**
- **Dose Rate Upset >$10^{10}$ RAD(Si)/s 20ns Pulse**
- **Cosmic Ray Upset Rate 2 x $10^{-9}$ Errors/Bit Day**
- **Latch-Up Free Under Any Conditions**
- **Fanout (Over Temperature Range)**
  - **Bus Driver Outputs . . . . . . . . . . . . . 15 LSTTL Loads**
- **Military Temperature Range . . . . . . . . -55°C to +125°C**
- **Significant Power Reduction Compared to LSTTL ICs**
- **DC Operating Voltage Range . . . . . . . . . . .4.5V to 5.5V**
- **LSTTL Input Compatibility**
  - **VIL = 0.8V Max**
  - **VIH = VCC/2 Min**
- **Input Current Levels II ≤ 5µA at VOL, VOH**

## Description

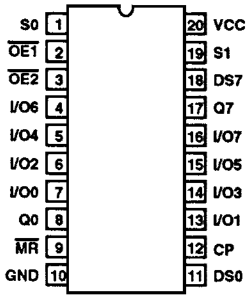
The Harris HCTS299MS is a Radiation Hardened 8-bit shift/storage register with tri-state bus interface capability. The register has four synchronous operating modes controlled by the two select inputs (S0, S1). The mode select, the serial data (DS0, DS7) and the parallel data (IO0 - IO7) respond only to the low to high transition of the clock (CP) pulse. S0, S1 and the data inputs must be one set up time period prior to the clocks positive transition. The master reset ($\overline{\text{MR}}$) is an asynchronous active low input.

The HCTS299MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family with TTL input compatibility.

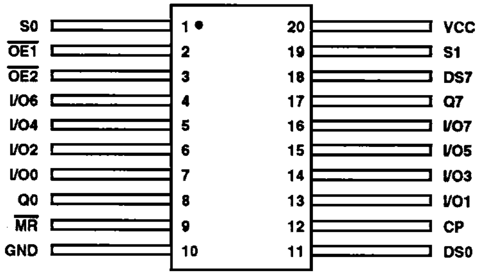
The HCTS299MS is supplied in a 20 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

## Pinouts

**20 PIN CERAMIC DUAL-IN-LINE**
**MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C**
TOP VIEW



**20 PIN CERAMIC FLAT PACK**
**MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C**
TOP VIEW



## Truth Tables

### Register Operating Modes

| FUNCTION | INPUTS | | | | | | | REGISTER OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{MR}$ | CP | S0 | S1 | DS0 | DS7 | I/On | Q0 | Q1 ... Q6 | Q7 |
| Reset (Clear) | L | X | X | X | X | X | X | L | L ... L | L |
| Shift Right | H | ↑ | h | l | l | X | X | L | q0 ... q5 | q6 |
| | H | ↑ | h | l | h | X | X | H | q0 ... q5 | Q6 |
| Shift Left | H | ↑ | l | h | X | l | X | q1 | q2 ... q7 | L |
| | H | ↑ | l | h | X | h | X | q1 | q2 ... q7 | H |
| Hold (Do Nothing) | H | ↑ | l | l | X | X | X | q0 | q1 ... q6 | q7 |
| Parallel Load | H | ↑ | h | h | X | X | l | L | L ... L | L |
| | H | ↑ | h | h | X | X | h | H | H ... H | H |

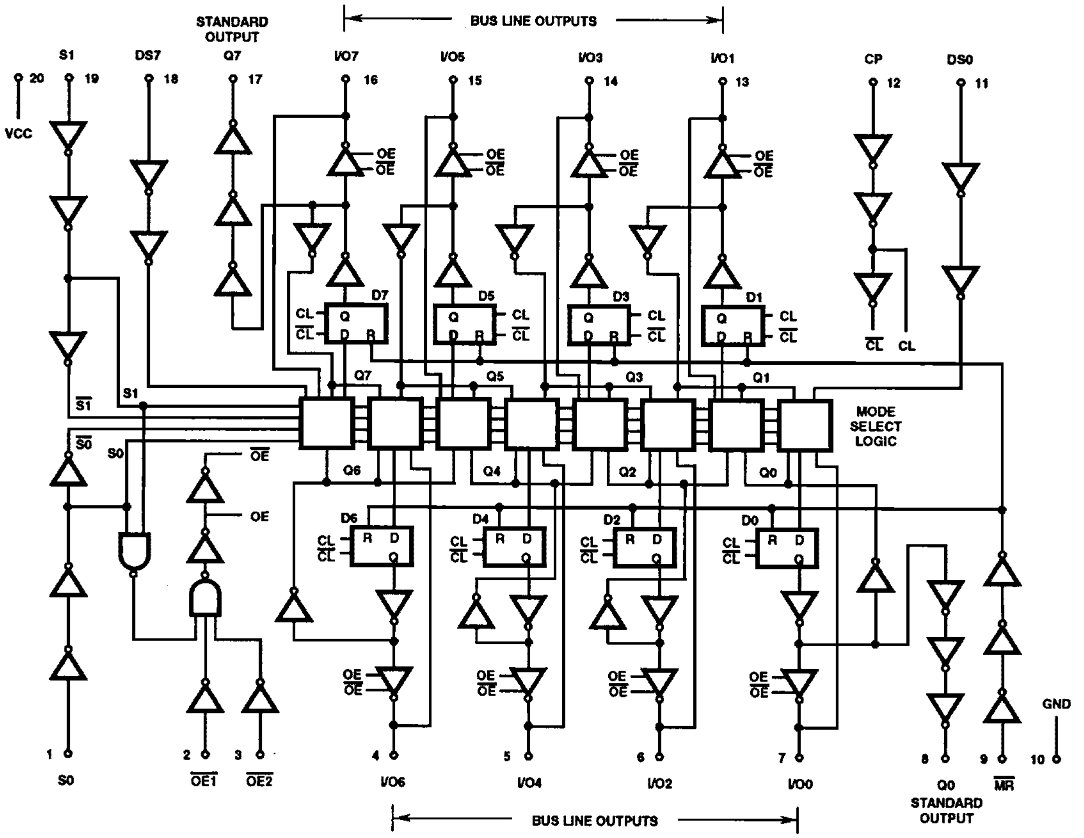
### Tri-State I/O Port Operating Mode

| FUNCTION | INPUTS | | | | | INPUTS/OUTPUTS |
|---|---|---|---|---|---|---|
| | $\overline{OE1}$ | $\overline{OE2}$ | S0 | S1 | Qn (REGISTER) | I/O0 ... I/O7 |
| Read Register | L | L | L | X | L | L |
| | L | L | L | X | H | H |
| | L | L | X | L | L | L |
| | L | L | X | L | H | H |
| Load Register | X | X | H | H | Qn = I/On | I/On = Inputs |
| Disable I/O | H | X | X | X | X | Z |
| | X | H | X | X | X | Z |

H = HighVoltage Level
L = Low Voltage Level
X = Immaterial
Z = Output in High Impedance State
h = Input Voltage High One Setup Time Prior Clock Transition
l = Input voltage Low One Setup Time Prior Clock Transition
↑ = Low-to-High Clock Transition

qn = Lower Case Letter Indicates the State of the Referenced Output One Setup Time Prior Clock Transition

## Functional Block Diagram



## Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . . . . . . . . . . . . . . . . . . . . . -0.5 to +7.0V
Input Voltage Range, All Inputs . . . . . . . . . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . . . . . . . . . . . . . . . . . . . ±10mA
DC Drain Current, Any One Output . . . . . . . . . . . . . . . . . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . . . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . . . . . . . . . . . . . . +265°C
Junction Temperature (TJ) . . . . . . . . . . . . . . . . . . . . . . . . . . +175°C
ESD Classification . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . Class 1

## Reliability Information

| Thermal Impedance | $\theta_{ja}$ | $\theta_{jc}$ |
|---|---|---|
| Weld Seal DIC | 75°C/W | 16°C/W |
| Weld Seal Flat Pack | 64°C/W | 12°C/W |

Power Dissipation per Package (PD)
For $T_A$ = -55°C to +100°C . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1W
For $T_A$ = +100°C to +125°C . . . . . . . Derate Linearly at 13mW/°C

*CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.*

## Operating Conditions

Supply Voltage (VCC) . . . . . . . . . . . . . . . . . . . . . . . . +4.5V to +5.5V
Operating Temperature Range ($T_A$) . . . . . . . . . . . . -55°C to +125°C
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . . . 500ns Max
Input Low Voltage (VIL) . . . . . . . . . . . . . . . . . . . . . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . . . . . . . . . . . . . . . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETERS | SYMBOL | (NOTE 1) CONDITIONS | GROUP A SUB-GROUPS | TEMPERATURE | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Quiescent Current | ICC | VCC = 5.5V, VIN = VCC or GND | 1 | +25°C | - | 40 | µA |
| | | | 2, 3 | +125°C, -55°C | - | 750 | µA |
| Output Current (Sink) | IOL | VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V | 1 | +25°C | 7.2 | - | mA |
| | | | 2, 3 | +125°C, -55°C | 6.0 | - | mA |
| Output Current (Source) | IOH | VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V | 1 | +25°C | -7.2 | - | mA |
| | | | 2, 3 | +125°C, -55°C | -6.0 | - | mA |
| Output Voltage Low | VOL | VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V | 1, 2, 3 | +25°C, +125°C, -55°C | - | 0.1 | V |
| | | VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V | 1, 2, 3 | +25°C, +125°C, -55°C | - | 0.1 | V |
| Output Voltage High | VOH | VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V | 1, 2, 3 | +25°C, +125°C, -55°C | VCC -0.1 | - | V |
| | | VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V | 1, 2, 3 | +25°C, +125°C, -55°C | VCC -0.1 | - | V |
| Input Leakage Current | IIN | VCC = 5.5V, VIN = VCC or GND | 1 | +25°C | -0.5 | +0.5 | µA |
| | | | 2, 3 | +125°C, -55°C | -5.0 | +5.0 | µA |
| Tri-State Output Leakage Current | IOZ | Applied Voltage = 0V or VCC | 1 | +25°C | -1 | +1 | µA |
| | | | 2, 3 | +125°C, -55°C | -50 | +50 | µA |
| Noise Immunity Functional Test | FN | VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2) | 7, 8A, 8B | +25°C, +125°C, -55°C | - | - | - |

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

**TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS**

| PARAMETER | SYMBOL | (NOTES 1, 2) CONDITIONS | GROUP A SUB-GROUPS | TEMPERATURE | LIMITS | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | | | MIN | MAX | |
| CLK to I/On | TPHL, TPLH | VCC = 4.5V | 9 | +25°C | 2 | 28 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 32 | ns |
| CLK to Q0, Q7 | TPHL, TPLH | VCC = 4.5V | 9 | +25°C | 2 | 30 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 34 | ns |
| $\overline{\text{MR}}$ to Output | TPHL | VCC = 4.5V | 9 | +25°C | 2 | 32 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 36 | ns |
| $\overline{\text{OEn}}$ to Output | TPZH | VCC = 4.5V | 9 | +25°C | 2 | 23 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 25 | ns |
| | TPHZ | | 9 | +25°C | 2 | 25 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 27 | ns |
| | TPZL | | 9 | +25°C | 2 | 27 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 30 | ns |
| | TPLZ | | 9 | +25°C | 2 | 30 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 34 | ns |

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS**

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | | | MIN | MAX | |
| Capacitance Power Dissipation | CPD | VCC = 5.0V, f = 1MHz | 1 | +25°C | Typical 98 | | pF |
| | | | 1 | +125°C | Typical 114 | | pF |
| Input Capacitance | CIN | VCC = Open, f = 1MHz | 1 | +25°C | - | 10 | pF |
| | | | 1 | +125°C | - | 10 | pF |
| Output Transition Time | TTHL, TTLH | VCC = 4.5V | 1 | +25°C | - | 15 | ns |
| | | | 1 | +125°C, -55°C | - | 22 | ns |
| Max Operating Frequency | FMAX | VCC = 4.5V | 1 | +25°C | - | 25 | MHz |
| | | | 1 | +125°C, -55°C | - | 16 | MHz |
| Setup Time DS0, DS7, I/On to CLK | TSU | VCC = 4.5V | 1 | +25°C | 20 | - | ns |
| | | | 1 | +125°C, -55°C | 30 | - | ns |
| Setup Time S1, S0 to CLK | TSU | VCC = 4.5V | 1 | +25°C | 27 | - | ns |
| | | | 1 | +125°C, -55°C | 41 | - | ns |
| Hold Time DS0, DS7, I/On, S0, S1 to CLK | TH | VCC = 4.5V | 1 | +25°C | 0 | - | ns |
| | | | 1 | +125°C, -55°C | 0 | - | ns |
| Recovery Time $\overline{\text{MR}}$ to CLK | TREC | VCC = 4.5V | 1 | +25°C | 5 | - | ns |
| | | | 1 | +125°C, -55°C | 5 | - | ns |

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)**

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Pulse Width $\overline{MR}$ | TW ($\overline{MR}$) | VCC = 4.5V | 1 | +25°C | 15 | - | ns |
| | | | 1 | +125°C, -55°C | 22 | - | ns |
| Pulse Width CLK | TW (CLK) | VCC = 4.5V | 1 | +25°C | 20 | - | ns |
| | | | 1 | +125°C, -55°C | 30 | - | ns |

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

**TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS**

| PARAMETERS | SYMBOL | (NOTES 1, 2) CONDITIONS | TEMPERATURE | 200K RAD LIMITS MIN | 200K RAD LIMITS MAX | 1M RAD LIMITS MIN | 1M RAD LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Quiescent Current | ICC | VCC = 5.5V, VIN = VCC or GND | +25°C | - | 0.75 | - | 2.0 | mA |
| Output Current (Sink) | IOL | VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V | +25°C | 6.0 | - | 5.0 | - | mA |
| Output Current (Source) | IOH | VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V | +25°C | -6.0 | - | -5.0 | - | mA |
| Output Voltage Low | VOL | VCC = 4.5V or 5.5V, VIH = VCC/2,<br>VIL = 0.8V at 200K RAD,<br>VIL = 0.3V at 1M RAD,<br>IOL = 50µA | +25°C | - | 0.1 | - | 0.1 | V |
| Output Voltage High | VOH | VCC = 4.5V or 5.5V, VIH = VCC/2,<br>VIL = 0.8V at 200K RAD,<br>VIL = 0.3V at 1M RAD,<br>IOH = -50µA | +25°C | VCC -0.1 | - | VCC -0.1 | - | V |
| Input Leakage Current | IIN | VCC = 5.5V, VIN = VCC or GND | +25°C | -5 | +5 | -5 | +5 | µA |
| Tri-State Output Leakage Current | IOZ | Applied Voltage = 0V or VCC | +25°C | - | ±50 | - | ±100 | µA |
| Noise Immunity Functional Test | FN | VCC = 4.5V, VIH = 2.25V,<br>VIL = 0.8V at 200K RAD,<br>VIL = 0.3V at 1M RAD (Note 3) | +25°C | - | - | - | - | - |
| CLK to I/On | TPHL, TPLH | VCC = 4.5V | +25°C | 2 | 32 | 2 | 40 | ns |
| CLK to Q0, Q7 | TPHL, TPLH | VCC = 4.5V | +25°C | 2 | 34 | 2 | 43 | ns |
| $\overline{MR}$ to Output | TPHL | VCC = 4.5V | +25°C | 2 | 36 | 2 | 45 | ns |
| $\overline{OEn}$ to Output | TPZH | VCC = 4.5V | +25°C | 2 | 25 | 2 | 32 | ns |
| | TPHZ | | | 2 | 27 | 2 | 33 | ns |
| | TPZL | VCC = 4.5V | +25°C | 2 | 30 | 2 | 43 | ns |
| | TPLZ | | | 2 | 34 | 2 | 43 | ns |

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

| PARAMETER | GROUP B SUBGROUP | DELTA LIMIT |
|---|---|---|
| ICC | 5 | 12μA |
| IOL/IOH | 5 | -15% of 0 Hour |
| IOZL/IOZH | 5 | ±200nA |

TABLE 6. APPLICABLE SUBGROUPS

| CONFORMANCE GROUPS | | METHOD | GROUP A SUBGROUPS | READ AND RECORD |
|---|---|---|---|---|
| Initial Test (Preburn-In) | | 100%/5004 | 1, 7, 9 | ICC, IOL/H, IOZL/H |
| Interim Test I (Postburn-In) | | 100%/5004 | 1, 7, 9 | ICC, IOL/H, IOZL/H |
| Interim Test II (Postburn-In) | | 100%/5004 | 1, 7, 9 | ICC, IOL/H, IOZL/H |
| PDA | | 100%/5004 | 1, 7, 9, Deltas | |
| Interim Test III (Postburn-In) | | 100%/5004 | 1, 7, 9 | |
| PDA | | 100%/5004 | 1, 7, 9, Deltas | |
| Final Test | | 100%/5004 | 2, 3, 8A, 8B, 10, 11 | |
| Group A (Note 1) | | Sample/5005 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 | |
| Group B | Subgroup B-5 | Sample/5005 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas | Subgroups 1, 2, 3, 9, 10, 11 |
| | Subgroup B-6 | Sample/5005 | 1, 7, 9 | |
| Group D | | Sample/5005 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 | |

NOTE: 1. Alternate Group A Inspection in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

| CONFORMANCE GROUPS | METHOD | TEST | | READ AND RECORD | |
|---|---|---|---|---|---|
| | | PRE RAD | POST RAD | PRE RAD | POST RAD |
| Group E Subgroup 2 | 5005 | 1, 7, 9 | Table 4 | 1, 9 | Table 4 (Note 1) |

NOTE: 1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC BURN-IN AND DYNAMIC

| OPEN | GROUND | 1/2 VCC = 3V ± 0.5V | VCC = 6V ± 0.5V | OSCILLATOR | |
|---|---|---|---|---|---|
| | | | | 50kHz | 25kHz |
| STATIC BURN-IN I TEST CONNECTIONS (Note 1) | | | | | |
| 8, 17 | 1 - 7, 9 - 16, 18, 19 | - | 20 | - | - |
| STATIC BURN-IN II TEST CONNECTIONS (Note 1) | | | | | |
| 8, 17 | 10 | - | 1 - 7, 9, 11 - 16, 18 - 20 | - | - |
| DYNAMIC BURN-IN TEST CONNECTIONS (Note 2) | | | | | |
| - | 2, 3, 10, 18, 19 | 4 - 8, 13 - 17 | 1, 9, 20 | 12 | 11 |

NOTES:

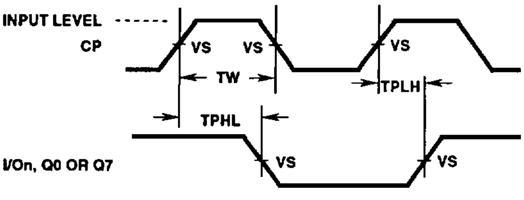
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

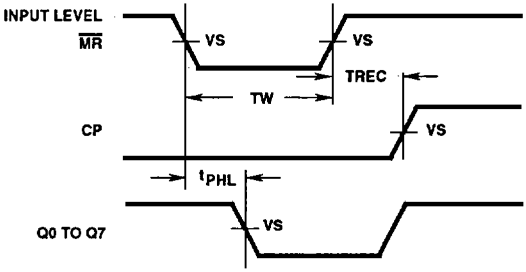
| OPEN | GROUND | VCC = 5V ± 0.5V |
|---|---|---|
| 8, 17 | 10 | 1 - 7, 9, 11 - 16, 18 - 20 |

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

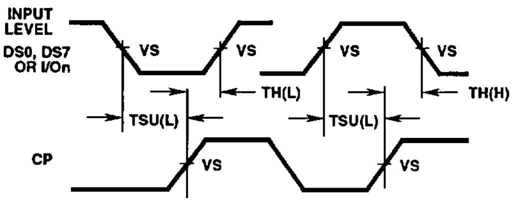
## AC Timing Diagrams and Load Circuit



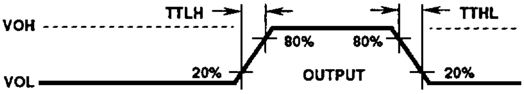
CLOCK PRE-REQUISITE AND PROPAGATION DELAYS



MASTER RESET PRE-REQUISITE AND PROPAGATION DELAYS



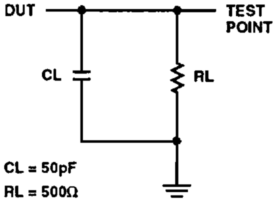
DATA PRE-REQUISITE TIMES



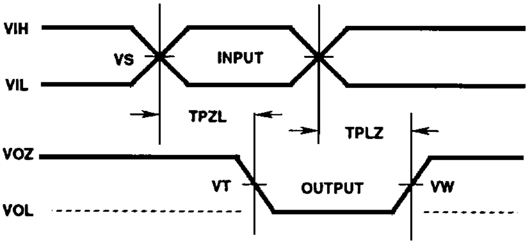
OUTPUT TRANSITION TIME

AC VOLTAGE LEVELS

| PARAMETER | HCTS | UNITS |
|---|---|---|
| VCC | 4.50 | V |
| VIH | 3.00 | V |
| VS | 1.30 | V |
| VIL | 0 | V |
| GND | 0 | V |



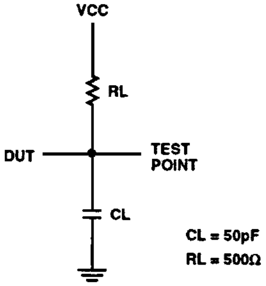
## Tri-State Low Timing Diagrams



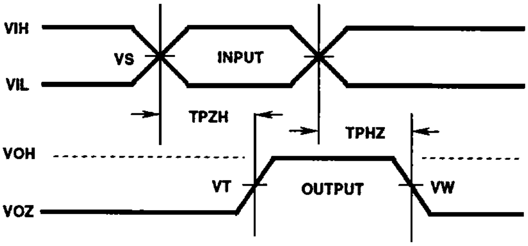
**TRI-STATE LOW VOLTAGE LEVELS**

| PARAMETER | HCTS | UNITS |
|---|---|---|
| VCC | 4.50 | V |
| VIH | 3.00 | V |
| VS | 1.30 | V |
| VT | 1.30 | V |
| VW | 0.90 | V |
| VIL | 0 | V |
| GND | 0 | V |

## Tri-State Low Load Circuit



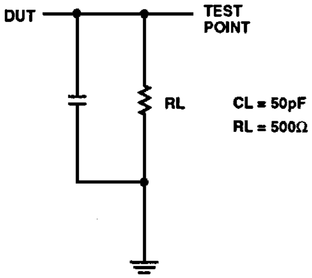
## Tri-State High Timing Diagrams



**TRI-STATE HIGH VOLTAGE LEVELS**

| PARAMETER | HCTS | UNITS |
|---|---|---|
| VCC | 4.50 | V |
| VIH | 3.00 | V |
| VS | 1.30 | V |
| VT | 1.30 | V |
| VW | 3.60 | V |
| VIL | 0 | V |
| GND | 0 | V |

## Tri-State High Load Circuit



## *Die Characteristics*

**DIE DIMENSIONS:**
123 x 94 mils

**METALLIZATION:**
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

**GLASSIVATION:**
Type: $SiO_2$
Thickness: 13kÅ ± 2.6kÅ

**DIE ATTACH:**
Material: Silver Epoxy

**WORST CASE CURRENT DENSITY:**
$<2.0 \times 10^5 A/cm^2$

**BOND PAD SIZE:**
100μm x 100μm
4 mils x 4 mils

## *Metallization Mask Layout*

HCTS299MS