PRODUCT BRIEF

AHA3370/3371

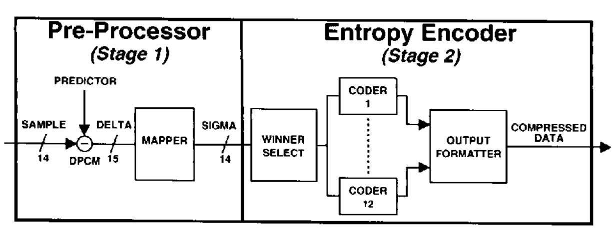
A HIGH SPEED LOSSLESS IMAGE COMPRESSION/DECOMPRESSION CHIP SET

AHA3370/3371 is a high speed, two chip VLSI implementation of the Rice lossless image compression algorithm. The compressor, AHA3370, employs a prediction coder using either the default previous symbol or the user specified external values and a Rice coding set with 12 different entropy coders. This combination helps achieve high compression depending on the entropy of the data being compressed. The chip set handles quantization of 4 to 14-bits per sample, also referred to as a symbol.

The algorithm adapts rapidly to changing entropy conditions and efficiently compresses data over a wide entropy range. (Entropy is the amount of randomness in a sample of data.) The AHA3370 usually achieves a compression ratio of 2.5:1 over several blocks, 6:1 and higher is possible depending on the data. A block contains 16 samples.

The AHA3370, an external Packetizer/Concatenator and the AHA3371 constitute a high speed, cost effective solution for lossless compression and decompression of broadcast quality, full motion, image data comprised of multiple bits per pixel. At maximum quantization of 14-bits per sample, the AHA3370 is capable of rates up to 35 MBytes/sec and the AHA3371 up to 21.5 MBytes/sec.

The architecture of the AHA3370 is a pipeline with data being input every clock cycle and compressed data being output when it is available. This enables the chip to maintain a fixed latency of 64 clock cycles.



Block Diagram of Rice Paradigm

FEATURES

PERFORMANCE:

- Rice adaptive lossless image compression algorithm
- Capable of rates up to 35 MBytes/sec compression and 21.5 MBytes/sec decompression
- 2.5 to 1 average compression ratio

FLEXIBILITY:

- Selectable quantization of 4 to 14-bits/sample
- The AHA3370 can input data continuously or in blocks of 16 samples each
- The AHA3370 supports a fill mode for blocks with less than 16 samples
- Automatic programmable insertion of reference symbols
- Uses either previous symbol prediction or user specified external prediction values
- The AHA3371 allows truncated packets
- The AHA3371 can input data in a continuous stream or in packets containing between 1 and 1024 compressed blocks of data

SYSTEM INTERFACE:

- No internal registers to program — hardware pins provided for user selectable parameters

OTHERS:

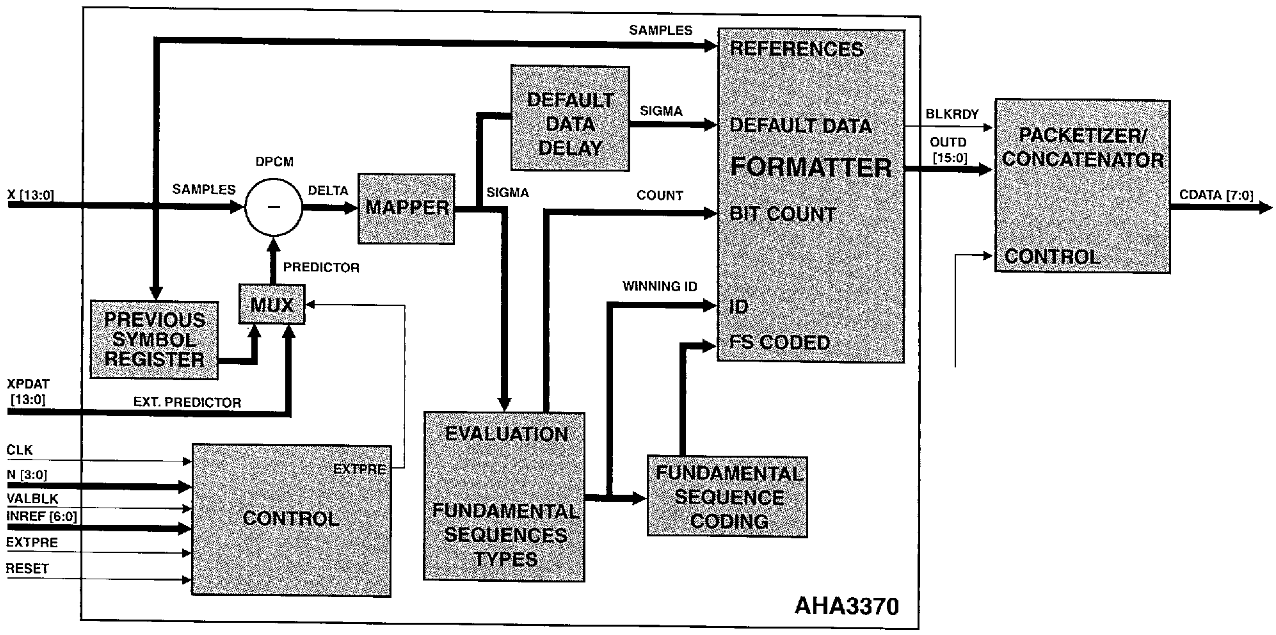
- Packetizer design and netlist available for an Actel FPGA implementation
- ISA Bus Demo Board available
- Software emulation of the algorithm available
- Low power static CMOS technology
- 25 mil lead pitch 100 pin QFP

APPLICATIONS

- Broadcast video
- Medical Imaging
- Satellite Imaging

Advanced Hardware Architectures

Request the *AHA3370/3371* Product Specification for complete details



AHA3370 Compressor Block Diagram

THE RICE ALGORITHM

The Rice algorithm was developed in the 1970's at the Jet Propulsion Laboratory (JPL), Pasadena, California, by Robert Rice for use in deep space missions. This lossless compression method is rapidly adaptive and efficient over a wide range of entropy conditions.

The algorithm uses previous symbol as a default, which calculates the differences between the previous sample and the current sample. Those differences are then mapped into positive integers. Because the algorithm uses differences, the original reference value must be sent out by the AHA3370 so the AHA3371 can determine the original sample values.

The AHA3370 relies on four principles:

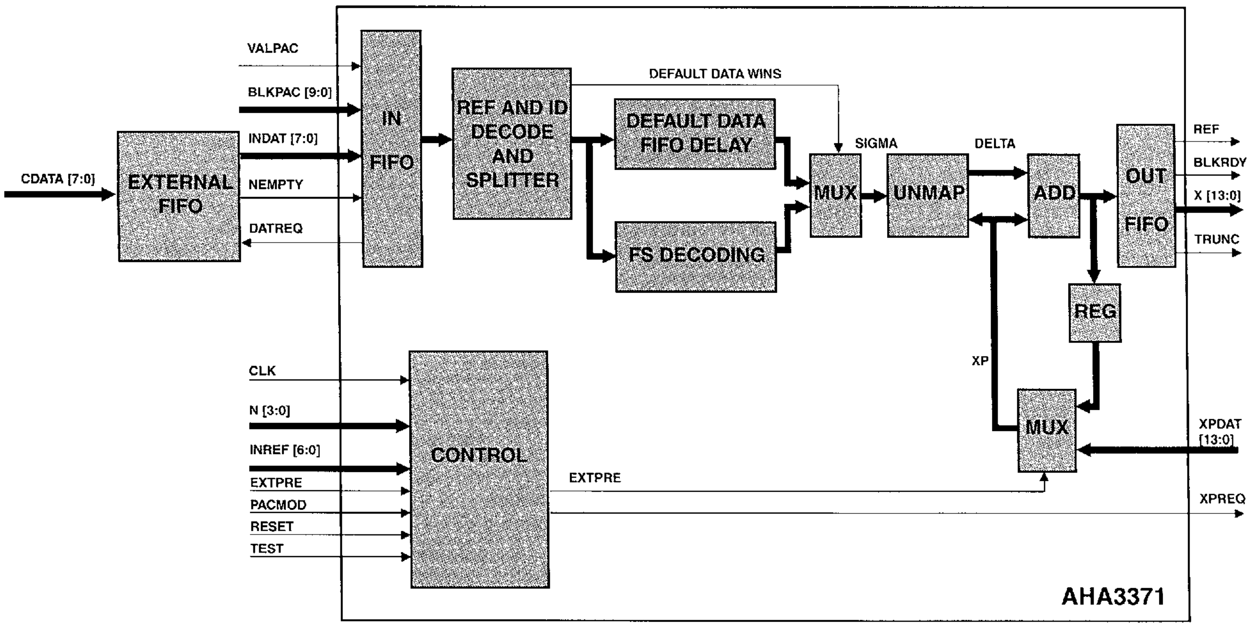
1. Using multiple encoders, each of which target a particular entropy range.

2. Processing an entire block of data by all the encoders, and picking the encoder that achieves the best compression ratio. This is a different philosophy than trying to predict the winning compressor for the next block based on what is known of the present block.

3. Maintaining small sized blocks for adaptability. This assumes the few bits required for an ID tag are insignificant compared to the ability to adapt to data with widely varying, unknown statistics.

4. Sample splitting, which makes the assumption that some of the least significant bits are random; and, therefore, cannot be compressed. The more significant bits are compressed and sent followed by the raw data of the least significant bits that are split off and saved.

Combined with the sample splitting is a simple code called the Fundamental Sequence. It works well for entropy ranges of approximately 2.5 bits/sample. The sample splitting is used 10 times with the Fundamental Sequence to cover entropy conditions that range from approximately 3 to 13-bits. A high entropy default encoding option limits the possible expansion to the number of bits in the input data block plus 4 ID bits. This makes the worst case maximum expansion six percent for 4-bit symbols and two percent for 14-bit symbols.



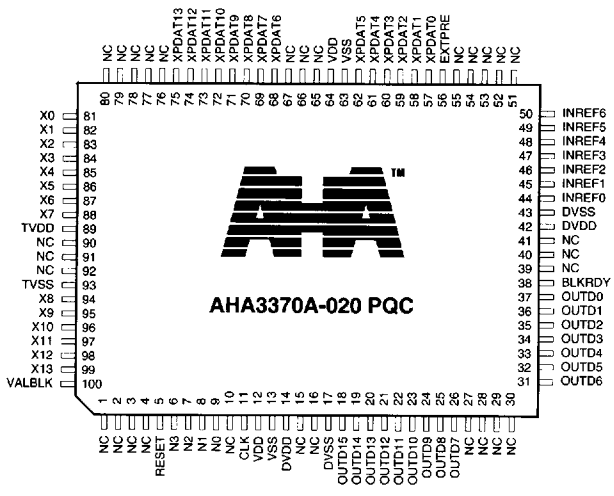
AHA3371 Decompressor Block Diagram

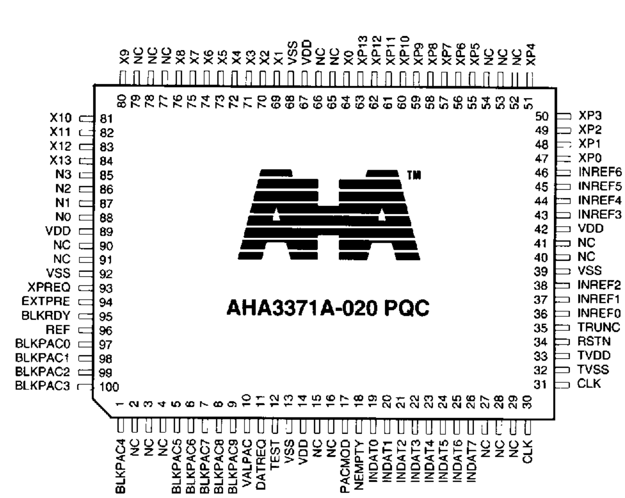
AHA3370 FUNCTIONAL DESCRIPTION

The AHA3370, Universal Symbol Compressor (USC), accepts input data symbols of 4 to 14-bits. These are first processed by a Differential Pulse Code Modulator (DPCM). This generates a sequence of differences, delta values, between each symbol and the immediately preceding symbol. These differences are then mapped into positive integers, called sigma values, such that the smaller differences, which are more likely to occur in image and audio type data, are given the smallest values. When a block of 16 differential samples are accumulated, the device identifies which of the second stage's 12 entropy coders will give the maximum compression for that block (see the block diagram on the first page). The unit then outputs a 16-bit header, a reference symbol when called for, the compressed block of data and fill bits as needed. The output is formatted onto a 16-bit bus. An external circuit called the Packetizer/Concatenator receives this output data and either packetizes it or converts it to a continuous stream compatible with the AHA3371 decompressor. The Packetizer/Concatenator removes the 16-bit header and fill bits from each block of 16 samples. If the data is to be packetized, then fill bits are inserted where necessary at the end of a packet. A packet can contain between 1 and 1024 compressed blocks of data. The maximum compression ratio for a block is 11.2:1 for 14-bit symbols, 6.4:1 for 8-bit symbols and 3.2:1 for 4-bit symbols.

AHA3371 FUNCTIONAL DESCRIPTION

The AHA3371, Universal Symbol Decompressor (USD), can be used in conjunction with an AHA3370 being clocked at 10 MHz or in a stand alone configuration. When used in conjunction, the decompression rate is equal to or greater than the compression rate of the AHA3370. This rate does not exceed the maximum decompression rate of the AHA3371, which is 12.3 MSamples/sec. The AHA3371 is a self-timed synchronous circuit, receiving data only when it asks for it. An external FIFO, therefore, is needed on the input side of the USD that holds the compressed data and supplies data nearly continuously. Whenever the Decompressor needs more data, it reads from the FIFO. The AHA3371 reads the coder ID generated by the AHA3370 and then decompresses the data in the manner specified by the ID.





ORDERING INFORMATION

PART NUMBER	DESCRIPTION
AHA3370A-020 PQC	Universal Symbol Compressor
AHA3371A-020 PQC	Universal Symbol Decompressor

AHA supplies other lossless compression devices using DCLZ, a derivative of the Lempel-Ziv Welch algorithm; error correction and storage controllers.

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PB337x-0694

RELATED TECHNICAL PUBLICATIONS

DOCUMENT #	DESCRIPTION
PS337x	AHA337x Product Specification (20 MSamples/sec)
PS3210	AHA3210 Product Specification (10 MBytes/sec, DCLZ)
PS3101	AHA3101 Product Specification (2.5 MBytes/sec, DCLZ)
GLGEN1	General Glossary of Terms
DCAHA	AHA3370/3371 Demonstration Disk (PC Compatible)
ANRA01	AHA Rice Demo Kit – User's Manual
ANRA02	AHA3370/3371 Packetizer Design for an Actel FPGA
RNASA1	On the Optimality of Code Options for a Universal Noiseless Coder
RNASA2	Algorithms for a Very High Speed Universal Noiseless Coding Module
RNASA3	Some Practical Universal Noiseless Coding Techniques, Part III, Module PSI14,K+
IEEE Article	A VLSI Chip Set for High-Speed Lossless Data Compression