NAND Flash Module

29F32G08

* NOTE: product does not ship with tie bars attached.

FEATURES:

High density
- Based on 32Gb x8 NAND flash die
- Supports higher speed designs with less capacitance/fewer I/O's to drive

NAND Flash Interface
- Single Level Cell (SLC) Technology
- ONFI 2.2 Compliant

Operating Voltage
- VCC 3.0 to 3.6V
- VCCQ 1.7 to 1.95V or 3.0 to 3.6V

Page Size
- 8640 bytes (8192 + 448 spare bytes)
- Supports external BCH correction algorithms (16 bit correction per 540 bytes)

Features
- High reliability data storage for demanding space applications
- Ceramic hermetic package with built-in TID shielding
- Class E, I, A, B or S

Speed
- Up to asynchronous timing mode 5 (50MT/sec)

Temperature Range
- -55°C to 125°C

Endurance
- 60,000 cycles typical

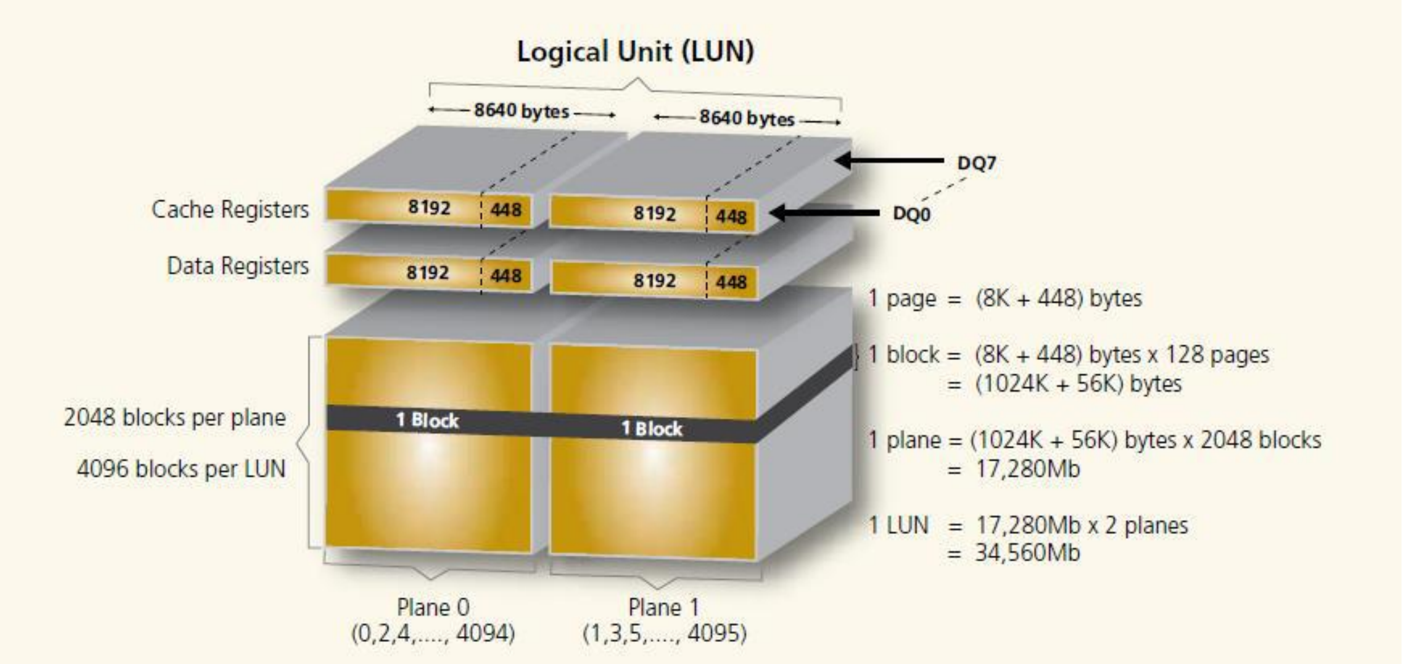
DESCRIPTION:

DDC's 32 Gb high density NAND flash features a x8 wide bus.

This NAND flash uses Single-Level Cell (SLC) NAND technology. Storing 1 bit of data per memory cell, SLC NAND offers fast read and write capabilities and boot times, excellent endurance and reliability.

DDC's patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding, while providing the required radiation shielding for a lifetime in orbit or space mission. RAD-PAK® provides a greater than 100 krads(Si) total dose tolerance, depending on space mission. This product is available with screening up to DDC Microelectronics self-defined Class S.

Supported Features:
ONFI 1.0, 2.0, 2.1, 2.2
Interleaved (multi-plane) operations
Multiple LUN operations
Small Data Move
Interleaved Address restrictions for cache operations
No interleaved block address restrictions
Overlapped/concurrent interleaving supported
Supports timing modes: 0 thru 5
Supports driver strength settings: underdrive, overdrive 1 and 2
Odd to Even Page Copyback
Supported Commands:
Reset
Reset LUN
Get Features
Set Features
Read Status
Read Status Enhanced
Change Read Column
Change Read Column Enhanced
Change Write Column
Change Row Address
Read Mode
Read Page
Read Page Multi-plane
Read Page Cache Sequential
Read Page Cache Random
Read Page Cache Last
Program Page
Program Page Multi-Plane
Program Page Cache
Erase Block
Erase Block Multi-Plane
Copyback Read
Copyback Program
Copyback Program Multi-Plane
Read Unique ID
Read Parameter Page
Read ID
Not Supported:
Non-sequential page programming
16 bit data bus width per Target/LUN
Synchronous Mode

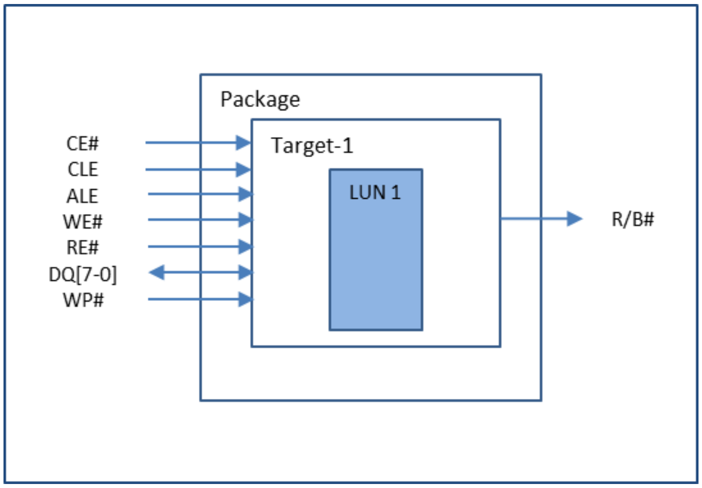


Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	L	L	CA13	CA12	CA11	CA10	CA9	CA8
Third	BA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	L	L	L	L	LUN	BA18	BA17	BA16

CA[n] = Column Address
PA[n] = Page Address
BA[n] = Bank Address
LUN = Logical Unit Address
Row Address = LUN, Bank, Page Address
BA[7] = Plane Select
Column Addresses above 8639 are invalid (page size = 8192 + 448)

Memory Organization
Bytes per page: 8192
Spare ECC bytes per page: 448
Pages per block: 128
Blocks per LUN: 4096
LUNs per chip enable: 1;
Column address cycles: 2
Row address cycles: 3
Bits per cell: 1
Programs per page: 4
Number of interleave address bits: 1

Package Organization



Architecture
Independent 8 bit buses per package: 1
Targets per 8 bit bus: 1
LUNS per Target: 1
(1 die per 8 bit bus)
(1 die per package)

DC Characteristics (VCC = 3.0 to 3.6V, VCCQ = 1.7 to 1.95V, 3.0 to 3.6V, TC = -55 to +125 °C) Subgroup (1,2,3)

Description	Symbol	Condition	Min	Max	Units
VCC Active Read array current (note 3)	ICC1_A		-	50	mA
VCC Program array Current (note 3)	ICC2_A		-	50	mA
VCC Active Erase Current (note 3))	ICC3_A		-	50	mA
I/O burst read current (note 3)	ICC4R_A	tRC = tRC min; Iout = 0mA	-	17	mA
I/O bust write current (note 3)	ICC4W_A	tWC = tWC min	-	19	mA
Bus idle current (note 4)	ICC5_A			5	mA
Current during first RESET command after power on (note 2)	ICC6			10	mA
Standby current – VCC (note 2) (typical 50uA at 85°C)	ISB	CE# = VCCQ-0.2V	-	100	uA
Standby current- VCCQ (note 2)	ISBQ	CE# = VCCQ-0.2V	-	10	uA
Staggered power-up current (note 1)	IST		-	10	mA

Note 1: Not Tested

Note 2: Per Die

Note 3: Per Active Die

Note 4: Per Die Per Enabled Target

DC Characteristics (VCC = 3.0 to 3.6V, VCCQ = 1.7 to 1.95V, 3.0 to 3.6V, TC = -55 to +125 °C) Subgroup (1,2,3)

Description	Symbol	Condition	Min	Max	Units
AC Input high voltage	VIH		0.8 x V_{CCQ}	Vcc_Q + .3V	V
AC Input low voltage, all inputs	VIL		-.3V	0.2 x V_{CCQ}	V
DC Input high voltage	$VIH_{(DC)}$		0.7 x V_{CCQ}	Vcc_Q + .3V	V
DC Input low voltage, all inputs	$VIL_{(DC)}$		-.3V	0.3 x V_{CCQ}	V
Individual Input leakage current, (per die) (note 2, & 3)	ILI	VIN = 0V to V_{CCQ}	-10000	10000	nA
Individual Output leakage current, (note 3)	OLI	VIN = 0V to V_{CCQ}	-10000	10000	nA
Output low current Ready/Busy	IOL_RB0	VOL = 0.4V	8	-	mA
Output Voltage High, Note 1	VOH	-100 mA	0.8 x V_{CCQ}	-	V
Output Voltage Low, , Note 1	VOL	100 mA	-	400	mV
Ready/Busy Output Voltage Low	VOL_RB	8 mA	-	400	mV

Note 1: Limits valid for full drive strength

Note 2: RE, CLE, ALE, WE, CE, WP

Note 3: Per Die

AC Characteristics (VCC = 3.0 to 3.6V, VCCQ = 1.7 to 1.95V, 3.0 to 3.6V, TC = -55 to +125 °C) Subgroup (9, 10, 11) Timing Mode 5, 20ns Clock period

Description	Symbol	Min	Max	Units
ALE to data start	tADL	70	-	ns
ALE hold time	tALH	5	-	ns
ALE setup time	tALS	10	-	ns
ALE to RE# delay	tAR	10	-	ns
CE# access time	tCEA	-	25	ns
CE# hold time	tCH	5	-	ns
CE# HIGH to output High –Z	tCHS	-	30	ns
CLE hold time	tCLH	5	-	ns
CLE to RE# delay	tCLR	10	-	ns
CLE setup time	tCLS	10	-	ns
CLE# HIGH to output hold	tCOH	15	-	ns
CE# setup time	tCS	15	-	ns
Data hold time	tDH	5	-	ns
Data setup time	tDS	7	-	ns
Output High-Z to RE# LOW (note 2)	tIR	0	-	ns
READ cycle time (note 1)	tRC	20	-	ns
RE# access time	tREA	-	16	ns
RE# HIGH hold time	tREH	7	-	ns
RE# HIGH to output hold	tRHOH	15	-	ns
RE# HIGH to WE# LOW	tRHW	100	-	ns
RE# HIGH to output High-Z	tRHZ	-	100	ns
RE# LOW to output hold	tRLOH	5	-	ns
RE# pulse width	tRP	10	-	ns
Ready to RE# LOW	tRR	20	-	ns
WE# High to busy	tWB	-	100	ns
WRITE cycle time	tWC	20	-	ns
WE# pulse width HIGH	tWH	7	-	ns
WE# HIGH to RE# LOW	tWHR	60	-	ns
WE# pulse width	tWP	10	-	ns
WP# transition to WE# LOW (note 2)	tWW	100	-	ns

Note 1: Test Condition, not measured.

Note 2: Not Tested

Note 3: All timing parameters may need to be relaxed if I/O strength is not set to full

Program Erase Characteristics (VCC = 3.0 to 3.6V, VCCQ = 1.7 to 1.95V, 3.0 to 3.6V, TC = -55 to +125 °C) Subgroup (9, 10, 11)

Description	Symbol	Min	Max	Units
Number of partial-page programs (note 2)	NOP	-	4	cycles
Erase block operation time	tBERS	-	7000	us
Change column setup time to data in/out or next command	tCCS	-	240	ns
Busy time for program cache operation	tCBSY	-	560	us
Busy time for TWO-PLANE PROGRAM PAGE or TWO-PLANE BLOCK ERASE (note 1)	tDBSY	-	1	us
Cache read busy time (note 1)	tRCBSY	-	35	us
Busy time for SET/GET FEATURES operations	tFEAT	-	1	us
Power-on reset time (note 2)	tPOR	-	1	ms
Program page operation time	tPROG	-	560	us
Data transfer from Flash array to data register	tR	-	35	us
Reset time (READ) measured, (PROGRAM/ERASE) (note 1)	tRST	-	5/10/100	us

Note 1: Test Condition, not measured.

Note 2: Not Tested

Absolute Maximum Ratings

Description	Symbol	Min	Typical	Max	Units
Voltage Input	VIN	-0.6	-	4.6	V
VCC Supply voltage	VCC	-0.6	-	4.6	V
Storage temperature	TSTG	-65	-	150	°C
Weight (RP)	W	-	19	-	grams
Weight (RT)	W	-	15	-	grams
Tjc	Tjc	-	0.69	-	C/W

Operating Conditions

Description	Symbol	Min	Max	Units
Temperature	Trng	-55	125	°C
VCC	VCC	3.0	3.6	V
VCCQ I/O Voltage (1.7 – 1.95) (3.0 – 3.6)	VCCQ	1.7	3.6	V

Valid Blocks – Beginning of Life

Description	Symbol	Min	Max	Units
Valid Blocks per Die	NVB	4076	-	Blocks
ECC for Block 0; bit errors per 540 bytes		-	1	bit errors per 540 B
ECC for Blocks >0; bit errors per 540 bytes		-	2	bit errors per 540 B

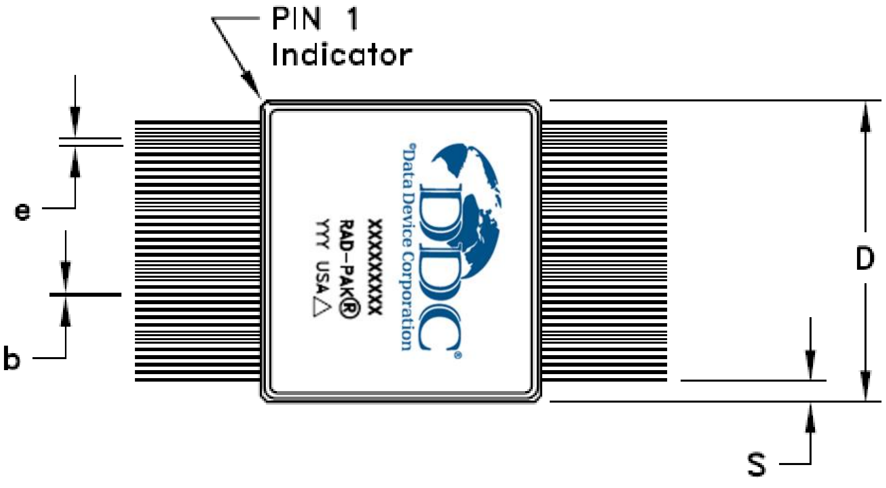
Delta Parameters

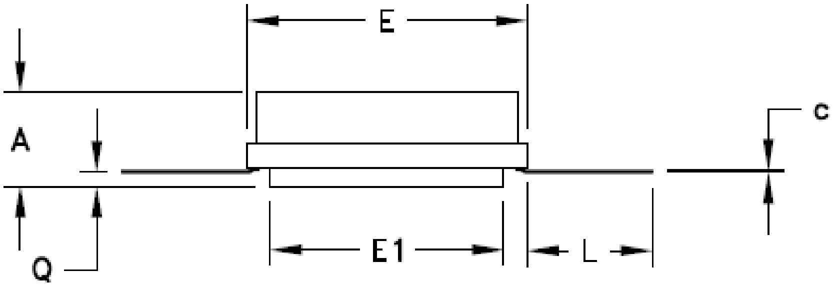
Description	Symbol	Delta Change
VCC Active Read array current	ICC1_A	10% of DS limit
VCC Program array Current)	ICC2_A	10% of DS limit
VCC Active Erase Current	ICC3_A	10% of DS limit
Icc Standby	ISB	10% of DS limit

Feature Summary

Description	Supported
ONFI 1.0, 2.0, 2.1, 2.2	Yes
Program page register clear enhancement	Yes
Extended parameter page	Yes
Interleaved(multi-plane) read operations	Yes
Synchronous interface	Yes
Odd to even page copyback	No
Interleaved (multi-plane) operations	Yes
Non-sequential page programming	No
Multiple LUN operations	Yes
16 bit data bus width per LUN	No
RESET LUN command	Yes
Small data move	Yes
CHANGE ROW ADDRESS	Yes
CHANGE READ COLUMN ENHANCED	Yes
READ UNIQE ID	Yes
COPYBACK	Yes
READ STATUS ENHANCED	Yes
GET FEATURES & SET FEATURES	Yes
Read cache commands	Yes
PROGRAM PAGE CACHE	Yes
Number of data bytes per page	8192
Number of spare bytes per page	448
Number of pages per block	128
Number of blocks per LUN	4096
Number of LUNs per chip enable	1
Number of address cycles	
Column address cycles	2
Row address cycles	3
Number of bits per cell	1
Bad blocks maximum per LUN	80
Block endurance	60,000
Guaranteed valid blocks at beginning	1
Block endurance for guranteed valid blocks	0
Number of programs per page	4
Number of bits ECC correctability	8
Number of interleaved address bits	1
Interleaved read cache	Yes
Interleaved address restrictions for cache operations	Yes
Interleaved program cache support	Yes
Interleaved block address restrictions	No
Overlapped/concurrent interleaving	Yes
Driver Strength; Overdrive 1 & 2	Yes

Description Cont'd	**Supported**
tPROG Typical (Page Program)	515 us
tBERS Typical (Block Erase)	7 ms
tR max (Page Read)	35 us
tCCS Typical (change column setup)	200 ns
Input pin capacitance, typical 32Gb	8 pF





68 LEAD FLAT PACKAGE			
	DIMENSION		
SYMBOL	MIN	NOM	MAX
A	0.235	0.255	0.276
b	0.006	0.008	0.010
c	0.006	0.008	0.010
D	0.990	1.000	1.010
e	0.025 BSC		
E	0.812	0.820	0.828
E1	0.665	0.670	0.675
L	0.360	0.370	0.380
Q	0.010	0.017	0.025
S	0.064	0.084	0.104
NOTE: ALL DIMENSIONS IN INCHES			

Pinout

Description	Pin #	Pin #	Description
VSS	1	68	VSS
VCC	2	67	NC
WP#	3	66	NC
WE#	4	65	NC
ALE	5	64	NC
CLE	6	63	NC
NC	7	62	NC
CE	8	61	NC
RE#	9	60	NC
RB#	10	59	NC
VSS	11	58	VSS
VCC	12	57	NC
VSS	13	56	VSS
VSSQ	14	55	NC
VCCQ	15	54	NC
DQ7	16	53	NC
DQ6	17	52	NC
DQ5	18	51	NC
DQ4	19	50	NC
VSSQ	20	49	NC
VCCQ	21	48	NC
VCC	22	47	NC
VSS	23	46	VSS
NC	24	45	NC
VCCQ	25	44	NC
VSSQ	26	43	NC
DQ3	27	42	NC
DQ2	28	41	NC
DQ1	29	40	NC
DQ0	30	39	NC
VCCQ	31	38	NC
VSSQ	32	37	NC
VSS	33	36	VSS
VCC	34	35	NC

NC = Not internally connected

Product Ordering Options

29F 32G 08 yy F z

Screening Flow*:
S = DDC Class S
B = DDC Class B
A = DDC Class A
I = Industrial (testing at -40°C, +25°C, +85°C)
E = Engineering (testing at +25°C)

Package:
F = Flat Pack

Radiation Feature:
RP = RAD-PAK® Package Shielding
RT = Radiation Tolerant

Data Width:
08 = 8 bits wide

Total Density:
32 = 32 Gigabits (Gb)

Base Product Nomenclature:
Memory, flash, monolithic 3.3V NAND SLC

*For a listing of all screening tests associated with each screening flow class, visit: www.ddc-web.com/monolithic-screening-flow