INTEGRATED CIRCUITS
UNITRODE

UC7502-2
UC7502-3
ADVANCED INFORMATION

Error Signal Isolator

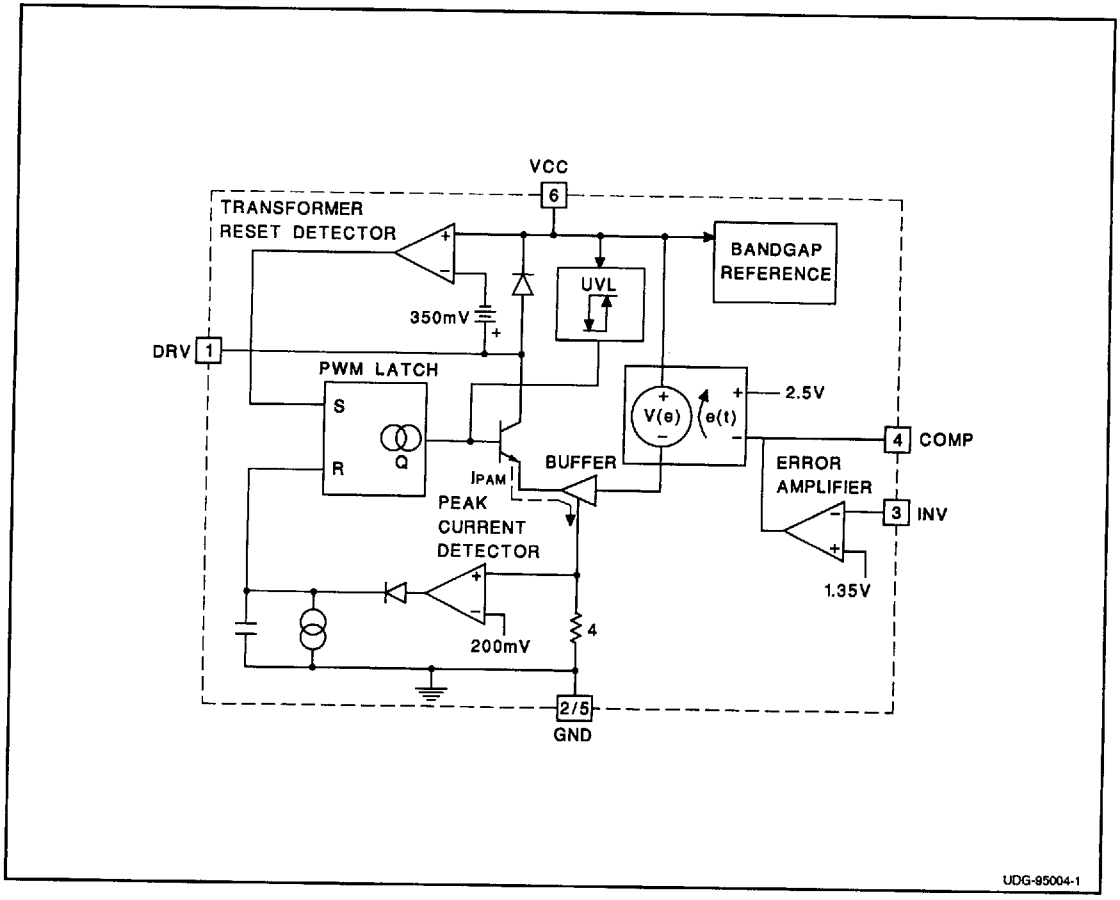
FEATURES

- Replaces Optocoupler in Primary Side Controlled Power Supplies
- Replaces TL431 and Eliminates Parasitic Zero
- Pulse Transformer Driver
- Same Transformer for Any Output Voltage
- Peak Current Controlled
- Functionality Integrated & Simplified 5-Pin Design

DESCRIPTION

The UC7502 is designed to monitor the output voltage of a power supply, generate an error signal, and transmit the error signal through an isolation barrier using a small pulse transformer. In conjunction with the pulse transformer, it replaces the TL431/optocoupler combination and eliminates the undesirable zero created by that combination. The transformer is driven with pulse amplitude modulation in a free-running oscillator configuration. The period of oscillation is proportional to the pulse transformer inductance. The voltage pulse magnitude is internally limited so that the pulse transformer design need not be changed for various output voltages.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Input Voltage $V_{CC_{MAX}}$ 17V
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature ..... -55°C to +150°C
Junction Temperature ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

All currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

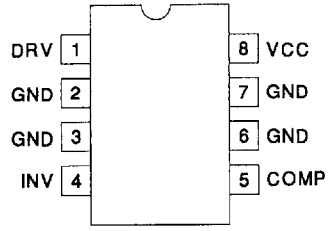
ORDERING INFORMATION

UC7502 □ — □
Temperature Range
Package

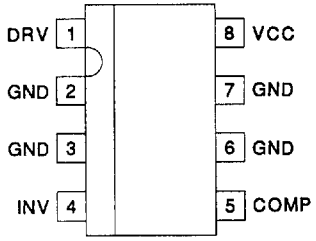
Package	Temperature Range
DP: Power SOIC	2: -40°C to +85°C
J: Ceramic DIL	3: 0°C to +70°C
N: Plastic DIL	

CONNECTION DIAGRAMS

DIL-8, (Top View)
(J or N Packages)



SOIC-8 (Top View)
(DP Package)



ELECTRICAL CHARACTERISTICS

Unless otherwise stated these specifications apply for T_A = -40°C to +85°C for UC7502-2, and 0°C to +70°C for UC7502-3; VCC = 5.0V, $T_A = T_J$.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Section						
V_{REF}	Error Amplifier Reference	T_J = 25°C	1.3365	1.35	1.3635	V
			1.323	1.35	1.377	V
Error Amplifier Section						
A_V	Open Loop Gain		60	95		dB
GBW	Gain Bandwidth Product			1		MHz
$I_{E/A}$	Source Current	V_{COMP} > 2.5V	-0.5	-1		mA
$I_{E/A}$	Sink Current	V_{COMP} < 1V		11		mA
I_{IB}	Input Bias Current			0.2	2.5	µA
Pulse Amplitude Modulator (PAM) Section						
V_F	Diode Clamp Voltage	I_F = 50 mA, T_J = 25°C		0.8		V
F_{PAM}	PAM Frequency (Recommended)				1.5	MHz
V_{CC} - V_{PAMmin}	PAM Peak Driving Voltage	$I_{PAM} = I_{PAMpk}$, VCC ≥ 5V	3.0	3.5		V
k	VCVS Level Shift Gain			1.3		V/V
Peak Current Detector Section						
I_{PAMpk}	Peak PAM Current Threshold			50		mA
t_{Doff}	Turn Off Delay			75		ns
Supply Voltage and Current Section						
I_{CC}	Supply Current	$I_{PAM} = I_F$ = 0, VCC 5V to 15V		9.5		mA
I_{CCoff}	Standby Current	VCC = 3.5V		600		µA
Under Voltage Lockout Section						
V_{UVLon}	Turn On Threshold of Vcc			4.1		V
ΔV_{UVL}	UVL Hysteresis			0.12		V

UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL (603) 424-2410 • FAX (603) 424-3460