OKI Semiconductor

Z365 PCMCIA

0.8μm Technology Mega Macrocell

DESCRIPTION

The Z365 PCMCIA Mega Macrocell is a featured library element in OKI's 0.8μm Sea of Gates and 0.8μm Customer Structured Array families. The OKI implementation of the Mega Macrocell is fully compatible with industry standard SE82365SL functions.

The Z365 provides an I/O memory function for the PCMCIA 2.0/JEIDA 4.1, 68-pin standard PC card. Using the Z365 enables designers to create custom chips with a PCMCIA interface.

The Memory Module Registers contain interface identity and version information. The maximum address is up to 26, with common read/write mode and attribute memory read/write mode provided. The battery and card detect circuit is also built-in.

The I/O Module consists of Card Information Structure (CIS) and Card Configuration Register (CCR) I/Os, with the battery and card detect circuit built-in.

The I/O Memory Module enables the OKI bus to interface with other modules. For example, the PCMCIA module can go through the OKI bus to an additional OKI bus, with either a PCI module or an AT bus interface. The operating voltage is 3V or 5V, and the module signal buffering enables card insertion and removal without mechanical interlocks. Flexible timing generators also provide different system speeds.

FEATURES

- Functionally compatible with SE82365SL
- ISA bus interface
- Compliant with PCMCIA 2.0/JEIDA 4.1
- 8-bit or 16-bit access supported
  - 8-bit access, 0 WAIT (standard)
  - 16-bit access, 0 WAIT (standard) 1-3 WAIT
- Range of window setting: 0-FFFFh (64 Kbytes)
- Card memory access space: 0-3FFFFFFh (64 Mbytes) (common attribute)
- $\overline{GPI}$ (Card Lock Detect) signal status
- One of the following IRQs can be allocated: IRQ3, IRQ4, IRQ5, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, or IRQ15
- CD1, CD2 (Card Detect) signal change
- Software card detect signal change
- Battery warning and battery dead interrupt by BVD1 and BVD2
- Card output signal shutdown control
- External data buffer, and address buffer effective and ineffective

This Mega Macrocell data sheet contains all the necessary information to enable the user to design a circuit using the Z365 functions for OKI 0.8μm technology.

0.8μm Technology Generation	Family Name	Family Type
1st	MSM10S0000	Sea of Gates
	MSM91S000	Customer Structured Array
2nd	MSM38S0000	Sea of Gates
	MSM98S000	Customer Structured Array

Recommended Operating Conditions (V_{SS} = 0V)

Parameter	Symbol	Rated value			Units
		Min	Typ	Max	
Power supply voltage	V_{DD}	2.7	3.3	3.6	V
		4.5	5.0	5.5	V
Operating temperature	T_j	-40	+25	+85	°C

Z365 PCMCIA Mega Macrocell

Mega Macrocell	Description	Logic Gate Count	Number of Mega Macrocell Pins
Z365	PCMCIA interface controller	15445	175

GENERAL CONVENTIONS

- In the logic symbol and signal descriptions, the prefix A indicates slot A and prefix B indicates slot B, e.g., $\overline{\text{AGPI}}$, $\overline{\text{BGPI}}$.
- Overscores on signal names indicate active-low signals, e.g. $\overline{\text{GPI}}$ is active low.
- The description of the register bits are only found under the corresponding functions.
- The names of the register bits sometimes use acronyms, e.g. GPI Enable = General Purpose Input Enable.
- Some intermediate signals are indicated by a prefix I. These signals are not directly coming in or going out of the mega macrocell. Examples include $\overline{\text{IREG}}$, $\overline{\text{IIORD}}$, $\overline{\text{IIOWR}}$, $\overline{\text{IAEN}}$, $\overline{\text{IBALE}}$, $\overline{\text{IMEMW}}$, and $\overline{\text{IMEMR}}$.

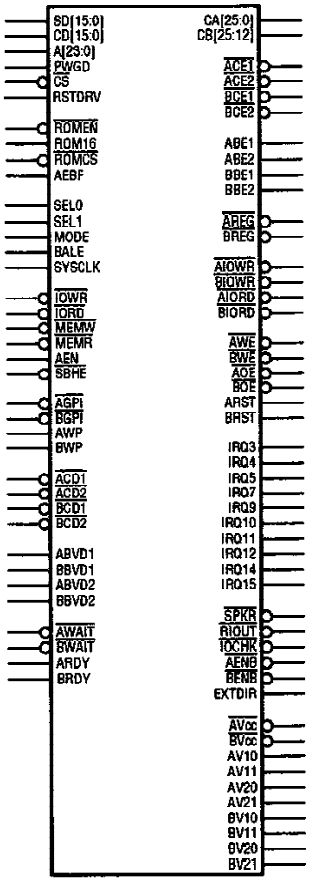

Figure 1. Logic Symbol

SIGNAL DESCRIPTIONS

Signal Name	I/O	Fan-In	Fan-Out	Description
SD[15:0]	I/O	1–2	15–22	**Data input/output.** Data input/output lines, integrating a bidirectional bus. D[7:0] accesses the PCIC internal registers.
CD[15:0]	I/O	1	6–15	**Address/data bus internal buffer.**
A[23:0]	I	1	–	**Address bus.** Address bus lines, driven by the host system, enable direct addressing of up to 16 Mbytes of memory per card. In a 16-bit ISA system, LA[23:17] should be connected to A[23:17], and SA[16:0] should be connected to A[16:0]. A0 is not used in Word Access mode, with A23 being the most significant bit.

SIGNAL DESCRIPTIONS (Continued)

Signal Name	I/O	Fan-In	Fan-Out	Description
Inputs				
PWGD	I	2	–	**Power good**. Active high signal indicating stable power to the system. Implementation not using the power good signal should tie this signal low.
$\overline{CS}$	I	2	–	**Chip select**. Signal driven from an address decode
RSTDRV	I	2	–	**Reset drive**. Active high signal indicating a main system cold reset, generated by the Intel386 SL CPU, as a combination of power good and the Intel386 SL CPU resume function.
$\overline{ROMEN}$	I	6.1	–	**ROM enable**. Memory enable signal
ROM16	I	2	–	**ROM16 enable**. Signal asserted by the PC card when the bus address corresponds to an address the PC card responds to. The addressed I/O port is capable of 16-bit accesses.
$\overline{ROMCS}$	I	1	–	**ROM chip select**. Memory chip select signal
AEBF	I	2	–	**Extend buffer**. Extend buffer signal indicating an extend buffer
SEL0, SEL1	I	2	–	**Select PCIC base I/O address**. Strapping options which determine the PCIC registers base I/O address. All PCIC registers are accessed indirectly using an offset from the base I/O address. These signals allow chaining several PCICs together.
MODE	I	1	–	**Decode mode**. Determines the port address chip select decoded internally as mode = 0, or with external logic as mode = 1.
BALE	I	1	–	**Bus address latch enable**. Active high input used to latch A[23:17] at the beginning of any bus cycle
SYSCLK	I	1	–	**System clock** (4.77 MHz to 8.33 MHz). The system clock value determines the $\overline{IOCHK}$ timing characteristics. $\overline{IOCHK}$ pulse width is 3 SYSCLKs in length with a 16-bit $\overline{MEMR}$ and 16-bit $\overline{MEMW}$ delay.
$\overline{IOWR}$	I	1	–	**I/O port write**. Driven to an active state (low) indicating the PCIC has an I/O write cycle occurring on the system bus.
$\overline{IORD}$	I	1	–	**I/O port read**. Driven to an active state (low) indicating the PCIC has an I/O read cycle occurring on the system bus.
$\overline{MEMW}$	I	1	–	**System memory write**. Active low signal indicating a write cycle
$\overline{MEMR}$	I	1	–	**System memory read**. Active low signal indicating a read cycle
AEN	I	1	–	**System address enable**. Active high signal indicating system address enable
$\overline{SBHE}$	I	1	–	**System bus high enable**. Low signal indicating data is valid on the upper byte of the 16-bit data bus.
$\overline{AGPI}$*, $\overline{BGPI}$*	I	3	–	**General purpose input ($\overline{GPI}$, Card Lock Detect)**. When $\overline{GPI}$ is active, interrupts by CDIN are prevented.
AWP*, BWP*	I	1	–	**Write protect (WP)**. Reflects the status of the write protect switch on memory PC cards. If present, the signal is asserted when the switch is enabled and deasserted when the switch is disabled. If the memory PC card does not have a write protect switch, depending on the condition of the card memory, the card connects this line to ground or V_{CC}. If the memory PC card can always be written, the pin connects to ground. If the memory PC card is permanently write protected, the pin connects to V_{CC}. For I/O PC cards, write protect is used for the 16-bit port ($\overline{IOIS16}$) function. Signal status is available by reading the interface status register.
$\overline{ACD1}$*, $\overline{ACD2}$* $\overline{BCD1}$*, $\overline{BCD2}$*	I	3.6	–	**Card detect ($\overline{CD1}$, $\overline{CD2}$)**. Used for proper card insertion detection. To enable the detection process, the signals are positioned at opposite ends of the connector. Signals are connected to ground internally on the PC card and are forced low whenever a card is placed in a host socket. Signal status is available by reading the interface status register.

SIGNAL DESCRIPTIONS (Continued)

Signal Name	I/O	Fan-In	Fan-Out	Description
ABVD1*, BBVD1*, ABVD2*, BBVD2*	I	2 1	–	**Battery voltage detect (BVD1, BVD2).** Generated by memory PC cards including batteries. The signals indicates the battery condition on the memory PC card. When the battery is in good condition, both BVD1 and BVD2 are asserted (high); when BVD2 is negated while BVD1 is asserted, the battery is in warning condition and should be replaced, although data integrity on the memory PC card is still assured. If BVD1 is negated (low) with BVD2 either asserted or negated, the battery is no longer serviceable and data is lost. Signal status is available by reading the interface status register.
AWAIT*, BWAIT*	I	1	–	**Bus cycle WAIT (WAIT).** Signal driven by the PC card to delay completion of the memory or I/O cycle in progress.
ARDY*, BRDY*	I	2	–	**Ready/Busy (RDY/BSY).** Driven low by memory PC cards indicating the memory card circuits are busy processing a previous write command. RDY/BSY is set high when memory PC cards can accept new data transfer commands. RDY/BSY is used as an interrupt request for I/O PC cards. Signal status is available by reading the interface status register.
Outputs				
CA[25:0], CB[25:12]	O	–	5 12	**Card addresses.** Used with the lower 11 bits of address bus to generate card address
ACE1*, ACE2* BCE1*, BCE2*	O	–	28 6	**Card enable (CE1, CE2).** Active low card enable signals driven by the PCIC. CE1 enables even bytes and CE2 for odd bytes. A multiplexing scheme based on A0, CE1, and CE2 allows 8-bit hosts to access all data on D[7:0].
ABE1*, ABE2* BBE1*, BBE2*	O	–	16	**Buffer enable (BE1, BE2).** External buffer enable signals
AREG*, BREG*	O	–	7	**Attribute memory select (REG).** Inactive (high) for all normal accesses to main memory of the PC card. I/O PC cards will not respond to IORD or IOWR when REG is kept inactive. During DMA operations, REG must be kept inactive to ensure PC cards do not respond to the I/O portion of the DMA transfer, and to ensure that DMA accesses to the memory portion of the PC card take place to the common memory of the PC card. This may be accomplished on an ISA-compatible signal by forcing REG inactive whenever the ISA bus signal AEN is inactive. When this signal is active (low), access is limited to attribute memory when WE or OE are active, and to I/O ports when IORD or IOWR are active. Configurable memory PC cards and I/O PC cards contain configuration and status registers in attribute memory space.
AIOWR*, BIOWR*	O	–	15	**I/O write (CIOWR).** This signal is driven by the host system and used together with the REG line for gating I/O write data to the memory PC card. IOWR gates the I/O write data to the PC card only when the REG line is also asserted.
AIORD*, BIORD*	O	–	11	**I/O read (CIORD).** An active low signal driven by the host system and used with the REG line to gate I/O read data from the PC card. IORD gates I/O read data from the memory PC card only when the REG line is also asserted.
AWE*, BWE*	O	–	7	**Write enable (WE).** WE is used by the host for gating memory write data and also used for memory PC cards employing programmable memory technologies.
AOE*, BOE*	O	–	5 24	**Output enable (OE).** OE is an active low signal driven by the host system and used to gate memory read data from memory PC cards.
ARST*, BRST*	O	–	13	**Card reset (RST).** Forces a hard reset to a PC card
IRQ[5:3], IRQ7, IRQ[12:9], IRQ[15:14]	O	–	5–8	**System interrupt backplane requests.** Active high signals used to request interrupt service.
SPKR	O	–	5	**Speaker out.** Digital audio signal used to provide a single amplitude (digital) audio waveform intended to be driven to the system speaker, with pass through of SPKR from the I/O PC card. When audio signal is not present, this signal is held high.
RIOUT	O	–	32	**Ring indicate output.** Pass through ring indicating output from the I/O PC card

SIGNAL DESCRIPTIONS (Continued)

Signal Name	I/O	Fan-In	Fan-Out	Description
$\overline{\text{IOCHK}}$	O	–	15	**I/O Check (Interrupt request).** An active low output requests a standard maskable interrupt to the CPU. This signal is intended to be connected to the $\overline{\text{EXTSMI}}$ of the Intel386 SL CPU.
$\overline{\text{AENB}}$*, $\overline{\text{BENB}}$*	O	–	8 4	**External Buffer Enable ($\overline{\text{ENB}}$).** Signal used to select PC card socket to activate. This signal controls the external address buffer logic.
EXTDIR	O	–	10	**External transceiver direction control.** Signal is high during a read and low during a write, with write (low) being the default power up condition.
$\overline{\text{AVcc}}$*, $\overline{\text{BVcc}}$* AV10, AV11 AV20, AV21 BV10, BV11 BV20, BV21	O	–	8 6, 3 3, 6 3, 6 6, 3	**Power control ($\overline{\text{VccEN}}$, Vpp1EN0, Vpp1EN1, Vpp2EN0, Vpp2EN1).** Five signals (for each slot) used to control voltages for PCMCIA/JEIDA socket interface (V_{PP1}, V_{PP2} and V_{CC}). Logic is detailed in Power and RSTDRV Control Register.

* The prefix A indicates slot A; B indicates slot B

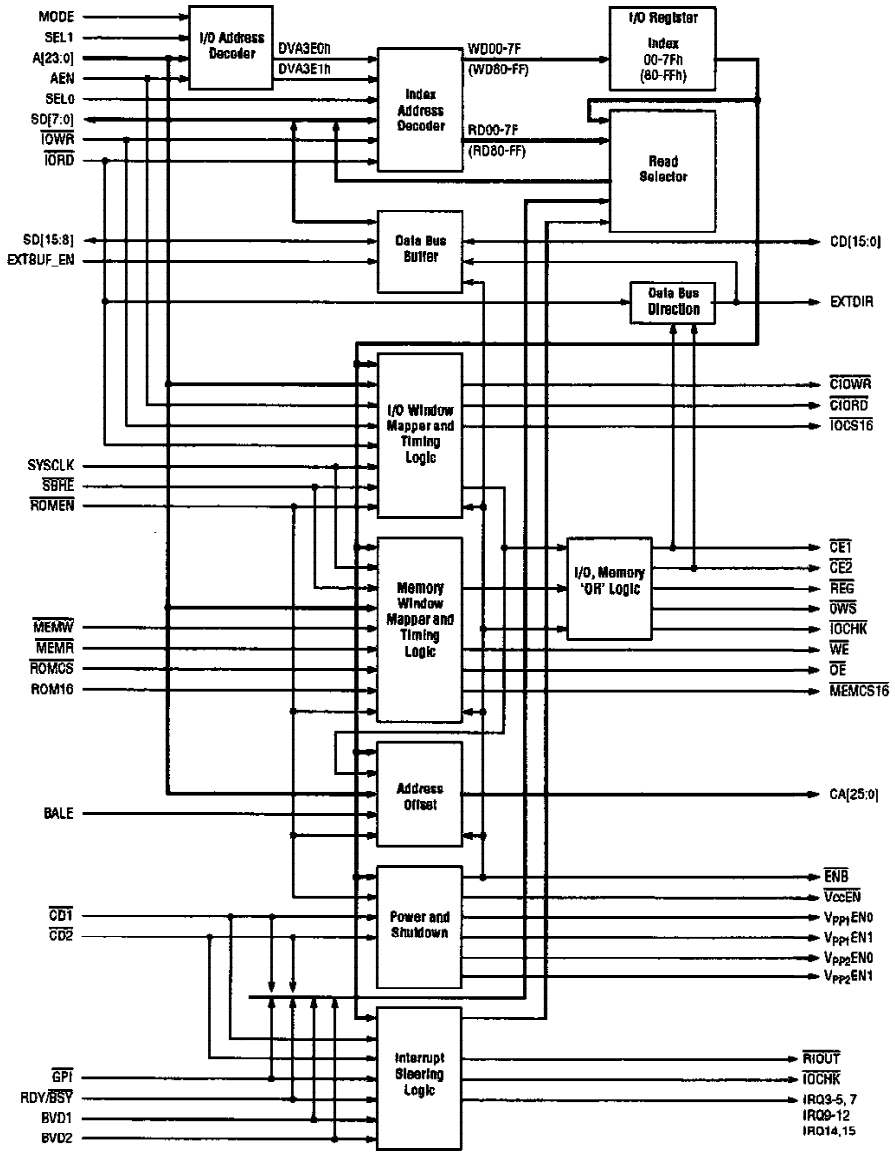

Figure 2. Block Diagram of the ISA and Slot A Interfaces

FUNCTIONAL DESCRIPTION

The Z365 implements a card interface which is functionally compatible with SE82365SL functions (Step B). General specifications for the Z365 include a system interface, and an ISA bus and card interface. The card interface is compliant with PCMCIA 2.0/JEIDA 4.1 and supports two slots.

I/Os

The Z365 has three types of I/Os, consisting of an I/O chip address, an I/O window, and an I/O access control interface. The I/O chip address is selectable from four types of internal decoding and also supports external decoding. The I/O window has two windows per slot, with 1 byte as the unit of window setting, and the window range supports 0 -FFFFh (64K bytes). I/O access control supports both 8-bit and 16-bit access, with 8-bit access 0 WAIT (standard) supported and 0 WAIT (standard)/1 WAIT supported for 16-bit access. Both WAIT and $\overline{\text{IOIS16}}$ signals are supported.

Memory Window and Memory Access Control

The Z365 contains both Memory window functions and Memory Access Control functions. The Memory window supports five windows per slot and operates with 4 Kbytes. It has ranges of 10000 - FFFFFFh when the I/O window is effective, and 0 - FFFFFFh (16 Mbytes) when the I/O window is ineffective. The Card Memory Access Space is 0 - 3FFFFFFh (64 Mbytes) and is common attribute. The Memory Access Control function supports both 8-bit and 16-bit access, with 8-bit access 0 WAIT (standard) supported, and 0 WAIT (standard)/1 to 3 WAIT supported for 16-bit access. Both WAIT and $\overline{\text{IOIS16}}$ signals are supported. A forceful write protect function is also included. I/Os, $\overline{\text{OE}}$, and $\overline{\text{WE}}$ are synchronized for 16-bit access function use.

Card Interface Status Detect

The Z365 includes a Card Interface Status Detect function and consists of six status signals. These signals are Card Lock Detect Signal Status ($\overline{\text{GPI}}$), Card Power Active Status, RDY/$\overline{\text{BSY}}$ Signal Status, WP Signal Status, CD1, CD2 Signal Status, and BVD1, BVD2 Signal Status functions.

Interrupts

The Z365 consists of an Interrupt Control and an Interrupt by Card Interface Status Change. The Interrupt Control is an interrupt by $\overline{\text{IREQ}}$ which allocates one of the following: IRQ3, IRQ4, IRQ5, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, or IRQ15. Two types of interrupts, Edge Trigger Interrupt and Level Interrupt, are also supported.

An Interrupt by Card Interface Status Change implements the interrupt. This is found to be most common in the Memory and I/O modes. The interrupt operates with the $\overline{\text{GPI}}$ signal change, CD1, CD2 (Card Detect) signal changes, and the software card detect change.

Memory and I/O Modes

Memory mode operates with the RDY/$\overline{BSY}$ Signal Change, and the Battery Warning and Battery Dead Interrupt enabling BVD1 and BVD2. The I/O mode operates with the STSCHG/$\overline{RI}$ Signal Change. One of the following IRQs can be allocated: IRQ3, IRQ4, IRQ5, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, IRQ15, or $\overline{IOCHK}$. An $\overline{RI}$ signal and a Card Detect Interrupt can be output to $\overline{RIOUT}$. Two types of interrupts, Edge Trigger Interrupt and Level Interrupt, are also supported. Interrupt clearing for read-clear/write-clear operates from I/O mode.

- The speaker function operates from I/O mode when the speaker signal is ON.
- The card reset function sends a RESET signal to the card. The Z365 also has a card power control through V_{CC}, V_{PP1}, V_{PP2}, and through the card output signal shutdown control.
- The Chip I/O Register value reset control operates with the RSTDRV effective/ineffective control. Card detection by the Z365 selects the control area to be reset.
- The Chip Power-Down Control Register controls the external data buffer and address buffer effective/ineffective control.

FUNCTIONAL BLOCKS AND REGISTERS

I/O Register and Decode

As shown in *Figure 3*, a schematic block diagram of the controller illustrates both the ISA interface and the slot A interface.

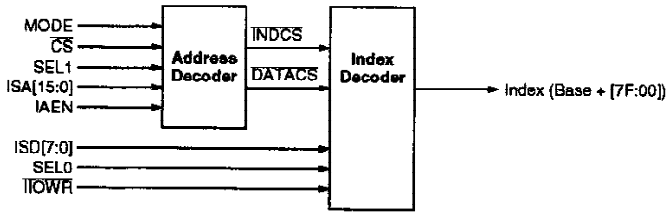

Figure 3. I/O Register and Decode Function

The controller consists of 98 internal registers, with 49 registers of slot A and 49 registers of slot B. Sixteen addresses of A[15:0] are decoded and the index form is adopted for addresses. Refer to *Table 1* for a listing of index and data I/O address decoding conditions. Refer to *Table 2* for a listing of index registers.

Table 1. I/O Address Decoding

Mode	$\overline{CS}$	SEL1	SEL0	Base	Index I/O Address	Data I/O Address
0	0	0	0	00h	3E0h	3E1h
0	0	0	1	80h	3E0h	3E1h
0	0	1	0	00h	3E2h	3E3h
0	0	1	1	80h	3E2h	3E3h
1	0	X	0	00h	A0 = 0	A0 = 1
1	0	X	0	80h	A0 = 0	A0 = 1
X	1	X	X	XXh	Not selected	

Table 2. Index Registers

Slot A Offset	Slot B Offset	Register Name
+00h	+40h	Identification and Revision
+01h	+41h	Interface Status
+02h	+42h	Power and RSTDRV Control
+03h	+43h	Interrupt and General Control
+04h	+44h	Card Status Change
+05h	+45h	Card Status Change Interrupt Configuration
+06h	+46h	Address Window Enable
+07h	+47h	I/O Control
+08h	+48h	I/O Address 0 Start Low Byte
+09h	+49h	I/O Address 0 Start High Byte
+0Ah	+4Ah	I/O Address 0 Stop Low Byte
+0Bh	+4Bh	I/O Address 0 Stop High Byte
+0Ch	+4Ch	I/O Address 1 Start Low Byte
+0Dh	+4Dh	I/O Address 1 Start High Byte
+0Eh	+4Eh	I/O Address 1 Stop Low Byte
+0Fh	+4Fh	I/O Address 1 Stop High Byte
+10h	+50h	System Memory Address 0 Mapping Start Low Byte
+11h	+51h	System Memory Address 0 Mapping Start High Byte
+12h	+52h	System Memory Address 0 Mapping Stop Low Byte
+13h	+53h	System Memory Address 0 Mapping Stop High Byte
+14h	+54h	Card Memory Offset Address 0 Low Byte
+15h	+55h	Card Memory Offset Address 0 High Byte
+16h	+56h	Card Detect and General Control
+17h	+57h	Reserved
+18h	+58h	System Memory Address 1 Mapping Start Low Byte
+19h	+59h	System Memory Address 1 Mapping Start High Byte
+1Ah	+5Ah	System Memory Address 1 Mapping Stop Low Byte
+1Bh	+5Bh	System Memory Address 1 Mapping Stop High Byte
+1Ch	+5Ch	Card Memory Offset Address 1 Low Byte
+1Dh	+5Dh	Card Memory Offset Address 1 High Byte
+1Eh	+5Eh	Global Control
+1Fh	+5Fh	Reserved
+20h	+60h	System Memory Address 2 Mapping Start Low Byte
+21h	+61h	System Memory Address 2 Mapping Start High Byte
+22h	+62h	System Memory Address 2 Mapping Stop Low Byte
+23h	+63h	System Memory Address 2 Mapping Stop High Byte
+24h	+64h	Card Memory Offset Address 2 Low Byte
+25h	+65h	Card Memory Offset Address 2 High Byte

Table 2. Index Registers (Continued)

Slot A Offset	Slot B Offset	Register Name
+26h	+66h	Reserved
+27h	+67h	Reserved
+28h	+68h	System Memory Address 3 Mapping Start Low Byte
+29h	+69h	System Memory Address 3 Mapping Start High Byte
+2Ah	+6Ah	System Memory Address 3 Mapping Stop Low Byte
+2Bh	+6Bh	System Memory Address 3 Mapping Stop High Byte
+2Ch	+6Ch	Card Memory Offset Address 3 Low Byte
+2Dh	+6Dh	Card Memory Offset Address 3 High Byte
+2Eh	+6Eh	Reserved
+2Fh	+6Fh	Reserved
+30h	+70h	System Memory Address 4 Mapping Start Low Byte
+31h	+71h	System Memory Address 4 Mapping Start High Byte
+32h	+72h	System Memory Address 4 Mapping Stop Low Byte
+33h	+73h	System Memory Address 4 Mapping Stop High Byte
+34h	+74h	Card Memory Offset Address 4 Low Byte
+35h	+75h	Card Memory Offset Address 4 High Byte
+36h	+76h	OKI Revision
+37h	+77h	Extension
+38h	+78h	Reserved
+39h	+79h	Reserved
+3Ah	+7Ab	Reserved
+3Bh	+7Bh	Reserved
+3Ch	+7Ch	Reserved
+3Dh	+7Dh	Reserved
+3Eh	+7Eh	Reserved
+3Fh	+7Fb	Reserved

Chip Revision

PCIC Revision Register

The Identification and Revision Register, as shown in *Figure 1*, is for read purposes only. 83h can be read from the Identification and Revision Register, similar to the 82365SL (Step B).

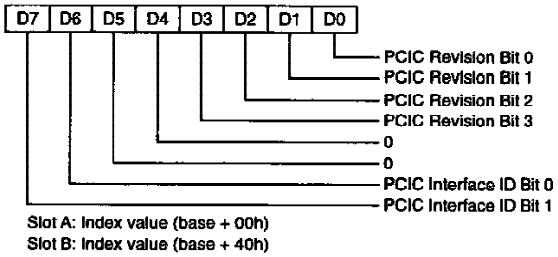

Figure 1. Identification and Revision Register (Read Only)

OKI Revision Register

The OKI revision register, as shown in *Figure 2*, is for read purposes only.

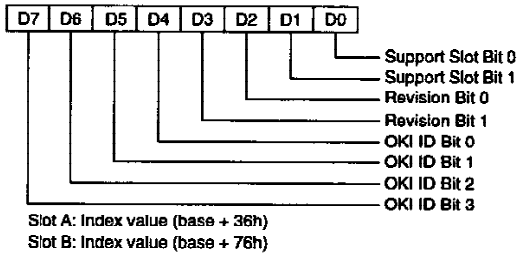

Figure 2. OKI Revision Register (Read Only)

The OKI Revision Register shows the ID number of an OKI chip (B2h), as shown in *Table 1* below.

Table 1. OKI Revision Register

Bits	Value
ID	1011
Revision	00
Support Slot	10

Card Status

The Card Status Function Block is shown in *Figure 3*.

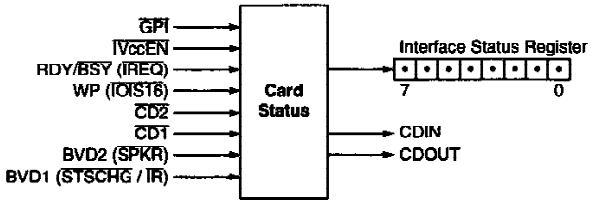

Figure 3. Card Status Function Block

Interface Status Register

The Interface Status Register is shown in *Figure 4*. The bits are defined below.

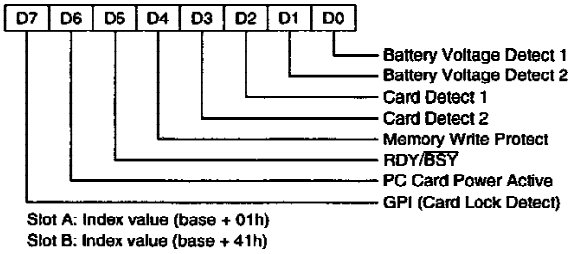

Figure 4. Interface Status Register (Read Only)

Table 2. Interface Status Register Description

D Bit(s)	Description
Bit 7	**Card Lock Detect Signal**. When set to "1", this bit indicates that $\overline{GPI}$ is active ($\overline{GPI}$="0"). When set to "0", this bit indicates that $\overline{GPI}$ is inactive ($\overline{GPI}$="1").
Bit 6	**PC Card Power Active**. When set to "1", this bit indicates that $\overline{VccEN}$ is active ($\overline{VccEN}$="0"). When set to "0" this bit indicates that $\overline{VccEN}$ is inactive ($\overline{VccEN}$="1").
Bit 5	**RDY/$\overline{BSY}$**. When set to "1", this bit indicates that RDY/$\overline{BSY}$ is active (RDY/$\overline{BSY}$="1"). When set to "0" this bit indicates that RDY/$\overline{BSY}$ is inactive (RDY/$\overline{BSY}$="0").
Bit 4	**Memory Write Protect**. When set to "1", this bit indicates that WP is active (WP="1"). When set to "0", this bit indicates that WP is inactive (WP="0").
Bit 3	**Card Detect 2**. When set to "1", this bit indicates that $\overline{CD2}$ is active ($\overline{CD2}$="0"). When set to "0", this bit indicates that $\overline{CD2}$ is inactive ($\overline{CD2}$="1").
Bit 2	**Card Detect 1**. When set to "1", this bit indicates that $\overline{CD1}$ is active ($\overline{CD1}$="0"). When set to "0", this bit indicates that $\overline{CD1}$ is inactive ($\overline{CD1}$="1").
Bit 1	**Battery Voltage Detect 2**. When set to "1", this bit indicates that BVD2 is active (BVD2="1"). When set to "0", this bit indicates that BVD2 is inactive (BVD2="0").
Bit 0	**Battery Voltage Detect 1**. When set to "1", this bit indicates that BVD1 is active (BVD1="1"). When set to "0", this bit indicates that BVD1 is inactive (BVD1="0").

The output status of CDIN and CDOUT signals are shown in *Table 3*.

Table 3. Output Status of CDIN and CDOUT Signals

$\overline{CD1}$	$\overline{CD2}$	CDIN	CDOUT	Status
0	0	1	0	The card is inserted
0	1	0	0	The card has been taken out
1	0	0	0	The card has been taken out
1	1	0	1	The card has been completely removed (used for resetting)

BVD1 and BVD2 signals show the Memory Card Battery Status. Signals and the corresponding battery status is shown in *Table 4*.

Table 4. Corresponding Signals

BVD1	BVD2	Status
0	0	Battery dead
0	1	Battery dead
1	0	Battery warning
1	1	Battery good

Card Power Control

The Card Power Control Function Block shuts down output signals to the card and controls $\overline{VccEN}$, V_{PP1}, and V_{PP2}, as shown in *Figure 5*.

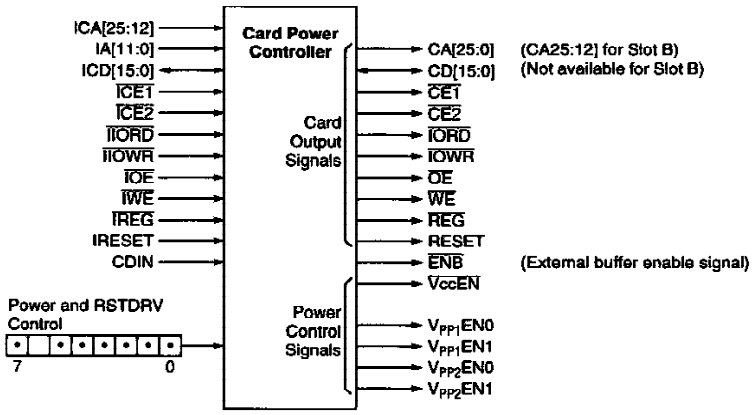

Figure 5. Card Power Control Function Block

Power and RSTDRV Control Register

The Power and RSTDRV Control Register is shown in *Figure 6*.

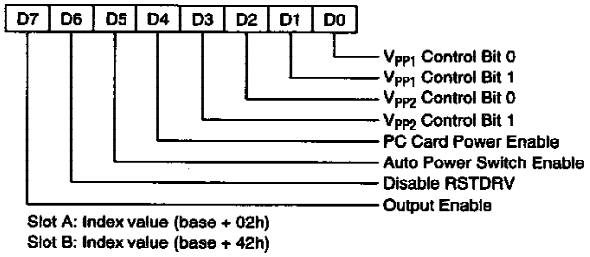

Figure 6. Power and RSTDRV Control Register (Read/Write)

The status of bit 7, bit 5, bit 4, CDIN signals, and the states of output signals to the card (CD[25:0], CD[15:0], $\overline{CE1}$, $\overline{CE2}$, $\overline{IORD}$, $\overline{IOWR}$, $\overline{OE}$, $\overline{WE}$, $\overline{REG}$, and RESET), as well as the $\overline{VccEN}$ signal is shown in *Table 5.*

Table 5. States of Bits, CDIN and Output Signals

Bit 7	Bit 5	Bit 4	CDIN	Tri-Output	$\overline{VccEN}$
X	X	0	X	Off	1
0	0	1	X	Off	0
X	0	1	0	Off	0
0	0	1	1	Off	0
1	0	1	1	On	0
X	1	1	0	Off	1
0	1	1	1	Off	0
1	1	1	1	On	0

The relationship with a $\overline{VccEN}$ signal and the respective correspondence of bit 3, bit 2, bit 1, and bit 0 to $V_{PP2}EN1$, $V_{PP2}EN0$, $V_{PP1}EN1$, and $V_{PP1}EN0$ are shown in *Table 6* and *Table 7.*

Table 6. Power Control Status (Bit 3 / Bit 2)

$\overline{VccEN}$	Bit 3	Bit 2	$V_{PP2}EN1$	$V_{PP2}EN0$
1	X	X	0	0
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	0

Table 7. Power Control Status (Bit 1 / Bit 0)

$\overline{VccEN}$	Bit 1	Bit 0	$V_{PP1}EN1$	$V_{PP1}EN0$
1	X	X	0	0
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	0

PC Card Reset Control

A RESET signal to the PC card is accomplished by writing to bit 6 of the Interrupt and General Control Register (Index 03h, 43h). The RESET signal to PC Card is shown in *Figure 7*. The bit is defined below.

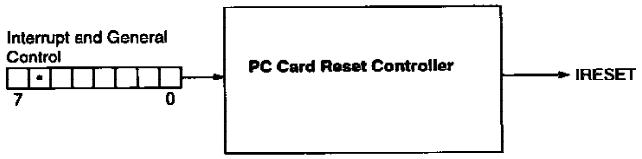

Figure 7. RESET Signal to PC Card

Interrupt and General Control Register

The Interrupt and General Control Registeris shown in *Figure 8*.

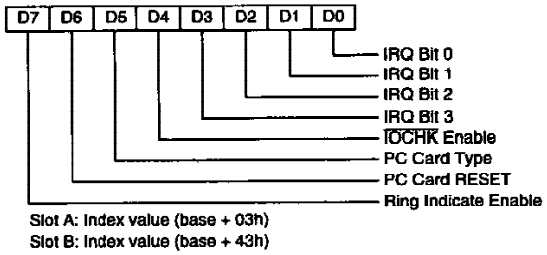

Figure 8. Interrupt and General Control Register (Read/Write)

Table 8. RESET Signal to PC Card Register Description

Bit	Description
Bit 6	**PC Card Reset.** When set to "1", this bit produces a RESET signal to the PC Card.

Card Mode Control

The Memory I/O Multiplex Function Block multiplexes four signals, (RDY/$\overline{BSY}$($\overline{IREQ}$), WP ($\overline{IOIS16}$), BVD2 ($\overline{SPKR}$), and BVD1 ($\overline{STSCHG}$/$\overline{RI}$)], all have different functions depending on the mode (Memory Card or I/O Card) by writing to bit 5 of the Interrupt and General Control Register , as shown in *Figure 9*. The bits are defined below.

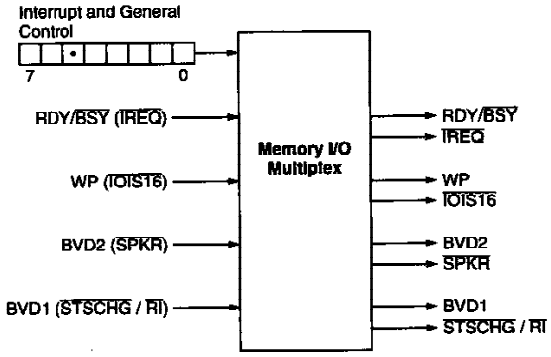

Figure 9. Memory I/O Multiplex Function Block

Interrupt and General Control Register

Card mode is controlled by the Interrupt and General Control Register, shown in *Figure 10*.

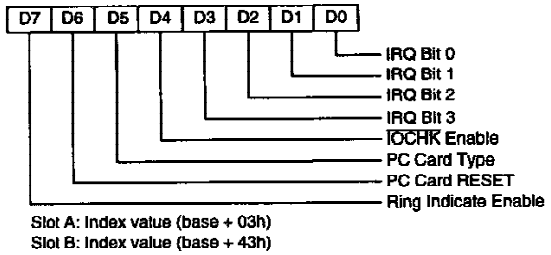

Figure 10. Interrupt and General Control Register (Read/Write)

Table 9. Memory I/O Multiplex Function Block Register Description

Bits	Description
Bit 5	**PC Card Type.** When set to "1", this bit enables I/O Card mode; when set to "0" this bit enable Memory Card mode.

Chip Register Reset

The Chip Register Reset Function Block is shown in *Figure 11*. The Chip Register Reset Function Block has two systems, a system that resets the A11 Register by a RSTDRV signal, and a system that resets only the Configuration Register by a CDOUT signal.

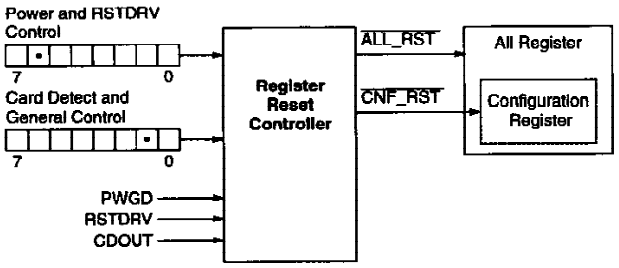

Figure 11. Chip Register Reset Function Block

Power and RSTDRV Control Register

The Power and RSTDRV Control Register is shown in *Figure 12*. The bit is defined below.

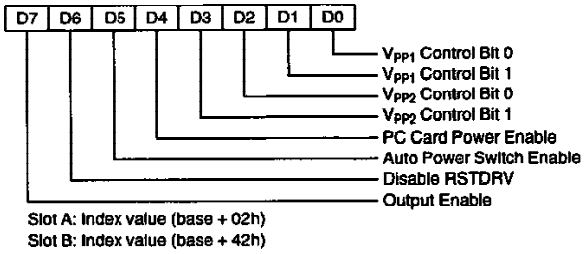

Figure 12. Power and RSTDRV Control Register (Read/Write)

Table 10. Power and RSTDRV Control Register Description

Bit	Description
Bit 6	**Disable RSTDRV.** When set to "0" this bit resets the A11 Register when RSTDRV is active; when set to "1" this bit does not reset the A11 Register when the PWGD signal is active, even if RSTDRV is active. Their relationship is shown in *Table 11*.

Table 11. A11 Register Reset

PWGD	RSTDRV	Bit 6	A11 Register Reset
X	0	X	No
0	1	0	Yes
0	1	1	Yes
1	1	0	Yes
1	1	1	No

Card Detect and General Control Register

The Card Detect and General Control Register is shown in *Figure 13*. The bits are defined below.

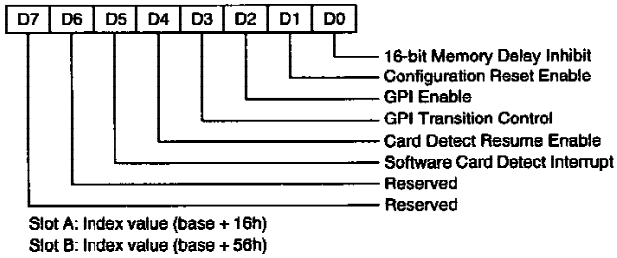

Figure 13. Card Detect and General Control Register (Read/Write)

The Configuration Register Reset output functions are shown in *Table 12*.

Table 12. Configuration Register Reset

CDOUT	Bit 1	Configuration Register Reset
0	0	No
0	1	No
1	0	No
1	1	Yes

The Configuration Register is shown in *Table 13.*

Table 13. Configuration Register

Slot A Offset	Slot B Offset	Register Name
+03h	+43h	Interrupt and General Control (except IOCHK enable bit)
+06h	+46h	Address Window Enable (except MEMCS16 decode A[23:12] bit)
+07h	+47h	I/O Control
+08h	+48h	I/O Address 0 Start Low Byte
+09h	+49h	I/O Address 0 Start High Byte
+0Ah	+4Ah	I/O Address 0 Stop Low Byte
+0Bh	+4Bh	I/O Address 0 Stop High Byte
+0Ch	+4Ch	I/O Address 1 Start Low Byte
+0Dh	+4Dh	I/O Address 1 Start High Byte
+0Eh	+4Eh	I/O Address 1 Stop Low Byte
+0Fh	+4Fh	I/O Address 1 Stop High Byte
+10h	+50h	System Memory Address 0 Mapping Start Low Byte
+11h	+51h	System Memory Address 0 Mapping Start High Byte
+12h	+52h	System Memory Address 0 Mapping Stop Low Byte
+13h	+53h	System Memory Address 0 Mapping Stop High Byte
+14h	+54h	Card Memory Offset Address 0 Low Byte
+15h	+55h	Card Memory Offset Address 0 High Byte
+18h	+58h	System Memory Address 1 Mapping Start Low Byte
+19h	+59h	System Memory Address 1 Mapping Start High Byte
+1Ah	+5Ah	System Memory Address 1 Mapping Stop Low Byte
+1Bh	+5Bh	System Memory Address 1 Mapping Stop High Byte
+1Ch	+5Ch	Card Memory Offset Address 1 Low Byte
+1Dh	+5Dh	Card Memory Offset Address 1 High Byte
+20h	+60h	System Memory Address 2 Mapping Start Low Byte
+21h	+61h	System Memory Address 2 Mapping Start High Byte
+22h	+62h	System Memory Address 2 Mapping Stop Low Byte
+23h	+63h	System Memory Address 2 Mapping Stop High Byte
+24h	+64h	Card Memory Offset Address 2 Low Byte
+25h	+65h	Card Memory Offset Address 2 High Byte
+28h	+68h	System Memory Address 3 Mapping Start Low Byte
+29h	+69h	System Memory Address 3 Mapping Start High Byte
+2Ah	+6Ah	System Memory Address 3 Mapping Stop High Byte
+2Bh	+6Bh	System Memory Address 3 Mapping Stop High Byte
+2Ch	+6Ch	Card Memory Offset Address 3 Low Byte
+2Dh	+6Dh	Card Memory Offset Address 3 High Byte
+30h	+70h	System Memory Address 4 Mapping Start Low Byte
+31h	+71h	System Memory Address 4 Mapping Start High Byte
+32h	+72h	System Memory Address 4 Mapping Stop High Byte
+33h	+73h	System Memory Address 4 Mapping Stop High Byte
+34h	+74h	Card Memory Offset Address 4 Low Byte
+35h	+75h	Card Memory Offset Address 4 High Byte

Power-Down Control

The Power-Down Control Function Block is shown in *Figure 14*. It stops input of SD[15:0], LA[23:17], SA[16:0], SYSCLK, $\overline{IOWR}$, $\overline{IORD}$, $\overline{MEMW}$, $\overline{MEMR}$, AEN, $\overline{SBHE}$, and BALE by setting bit 0 of the Global Control Register, and setting the $\overline{CS}$ pin to "H".

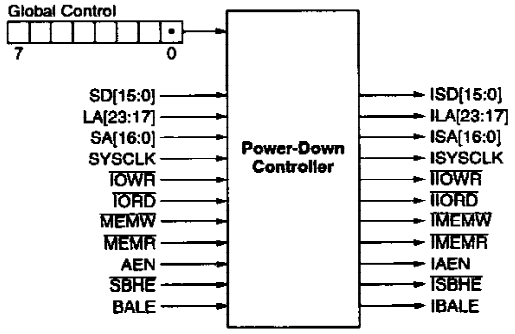

Figure 14. Power-Down Control Function Block

Global General Control Register

The Global General Control Register is shown in *Figure 15*.

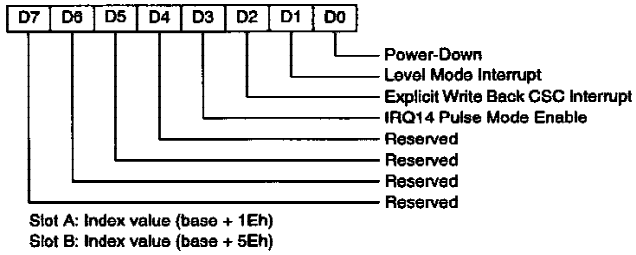

Figure 15. Global General Control Register (Read/Write)

Table 14. Global General Control Register Description

Bit	Description
Bit 0	**Power-Down**. When set to "1" this bit enables power-down mode. When set to "0" this bit disables power-down mode.

$\overline{RI}$ Signal Output

The $\overline{RIOUT}$ Signal Output Function Block is shown in *Figure 16*. When I/O Card mode is selected, the $\overline{RIOUT}$ output is enabled by writing "1" to bit 7 of the Interrupt and General Control Register, as shown in *Figure 16*. The bit is defined below.

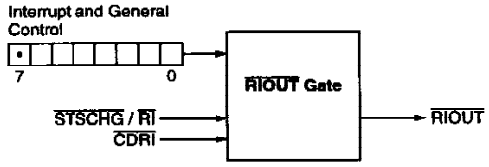

Figure 16. $\overline{RI}$ Signal Output Function Block

$\overline{RI}$ Signal Output is controlled by the Interrupt and General Control Register, shown in *Figure 17*.

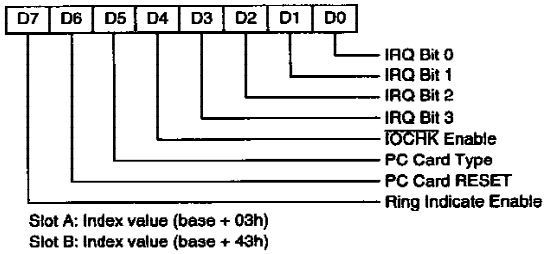

Figure 17. Interrupt and General Control Register (Read/Write)

Table 15. $\overline{RI}$ Signal Output Function Block Register Description

Bit	Description
Bit 7	**Ring Indicate Enable.** When set to "1" this bit enables $\overline{RIOUT}$; when set to "0" this bit disables $\overline{RIOUT}$.

The $\overline{RIOUT}$ signal output waveform is shown in *Figure 18*. A $\overline{CDRI}$ signal is generated by a card status change and is output to $\overline{RIOUT}$, regardless of the status of bit 7.

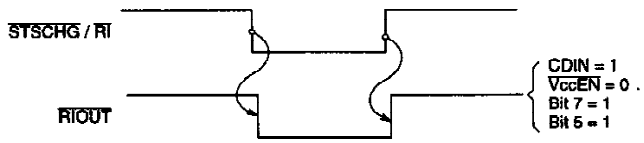

Figure 18. Card Status Change Interrupt Function Block

Card Status Change Interrupt Control

The Card Status Change Interrupt Control Function Block executes an interrupt when detecting a status change of $\overline{GPI}$, CDIN ($\overline{CD1}$, $\overline{CD2}$), RDY/$\overline{BSY}$, BVD1, BVD2, and $\overline{STSCHG}$/$\overline{RI}$ signals, and then generates $\overline{CSC\_INT}$ signals. An interrupt identical to an interrupt by a CDIN signal change by software can also be generated, as shown in *Figure 19*.

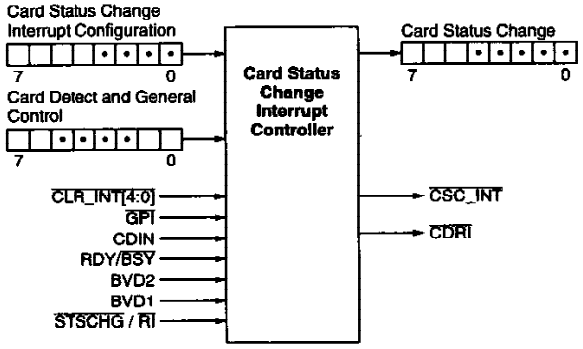

Figure 19. Card Status Change Interrupt Control Function Block

Card Status Change Interrupt Configuration Register

The Card Status Change Interrupt Configuration Register is shown in *Figure 20*. The bits are defined below.

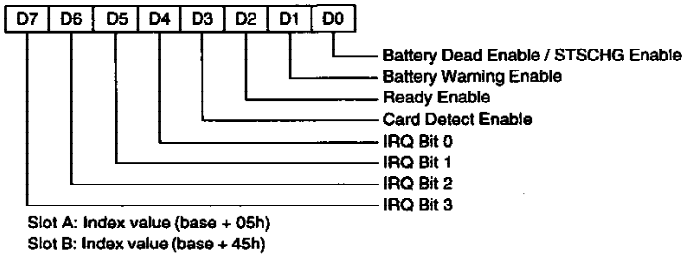

Figure 20. Card Status Interrupt Configuration Register (Read/Write)

Table 16. Card Status Interrupt Configuration Register Description

Bits	Description
Bit 3	**Card Detect Enable**. When set to "1", this bit enables an interrupt to CDIN (L↔H). When set to "0", this bit enables an interrupt to CDIN (L↔H).
Bit 2	**Ready Enable**. When set to "1", this bit enables an interrupt to RDY/$\overline{BSY}$ (L↔H). When set to "0", this bit enables an interrupt to RDY/$\overline{BSY}$ (L↔H).
Bit 1	**Battery Warning Enable**. When set to "1", this bit enables an interrupt to Battery Warning State (Good→Warning, Dead→Warning). When set to "0", this bit enables an interrupt to Battery Warning State (Good→Warning, Dead→Warning).
Bit 0	**Battery Dead Enable**. When set to "1", this bit enables an interrupt to Battery Dead State (Good→Dead, Warning→Dead) and also enables an interrupt to the $\overline{STSCHG}$ Signal Status Change in I/O card mode. When set to "0", this bit disables Battery Dead State.

Card Detect and General Control Register

The Card Detect and General Control Register is shown in *Figure 21*. The bits are defined below.

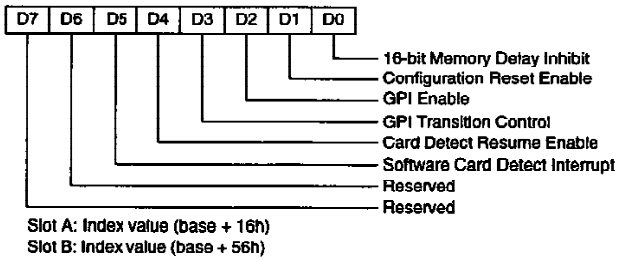

Figure 21. Card Detect and General Control Register (Read/Write)

Table 17. Card Detect and General Control Register Description

Bits	Description
Bit 5	**Software Card Detect Resume Enable.** When this bit is set to "1" and bit 3 of the Card Status Change Interrupt Configuration Register is also set to "1", this bit enables an interrupt similar to CDIN; when set to "0" this bit disables the interrupt. Note that no signal may be output to $\overline{CDRI}$.
Bit 4	**Card Detect Resume Enable.** When this bit is set to "1" and bit 3 of the Card Status Change Interrupt Configuration Register is also set to "1", this bit generates a $\overline{CDRI}$ signal by a CDIN signal change; when set to "0" this bit disables the signal. Note that no signal is output to IRQ*, $\overline{IOCHK}$.
Bit 3	**GPI Transition Control.** When set to "1" this bit enables $\overline{GPI}$ low-to-high status change (L⟶H); when set to "0" this bit enables $\overline{GPI}$ high-to-low status change (H⟶L).
Bit 2	**GPI Enable.** When set to "1" this bit enables $\overline{GPI}$; when set to "0" this bit disables $\overline{GPI}$.

Card Status Change Register

The Card Status Change Register indicates the cause of an interrupt, as shown in *Figure 22*. The bits are defined below.

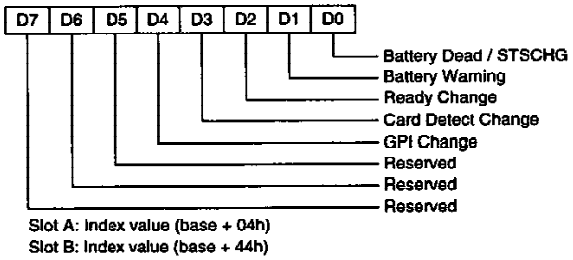

Figure 22. Card Status Change Register (Read/Write)

Table 18. Card Status Change Register Description

Bits	Description
Bit 4	**GPI Change.** When set to "1", this bit indicates a $\overline{GPI}$ signal status change.
Bit 3	**Card Detect Change.** When set to "1", this bit indicates a CDIN Signal Status Change (L←→H).
Bit 2	**Ready Change.** When set to "1", this bit indicates a RDY/$\overline{BSY}$ Signal Status Change (L→H).
Bit 1	**Battery Warning.** When set to "1" this bit indicates a Battery Warning Status Change (Good→Warning, Dead→Warning).
Bit 0	**Battery Dead.** When set to "1" this bit indicates a Battery Dead Status Change (Good→Dead, Warning→Dead). Note that a $\overline{STSCHG}$ signal status change has taken place in I/O Card mode.

Interrupt Select

The Interrupt Select Function Block is shown in *Figure 23*. An $\overline{CSC\_INT}$ signal generated by the Card Status Change Interrupt Controller can be assigned, and an $\overline{IREQ}$ signal from the I/O card to one of the following signals: $\overline{IOCHK}$, IRQ15, IRQ14, IRQ12, IRQ11, IRQ10, IRQ9, IRQ7, IRQ5, IRQ4, or IRQ3. Edge Trigger mode and Level mode are supported.

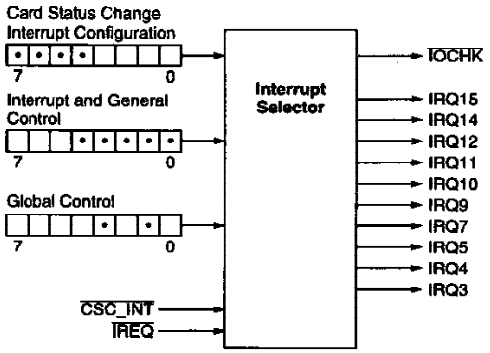

Figure 23. Interrupt Select Function Block

Card Status Change Interrupt Configuration Register

The Card Status Change Interrupt Configuration Register as shown in *Figure 24*. The bits are defined below.

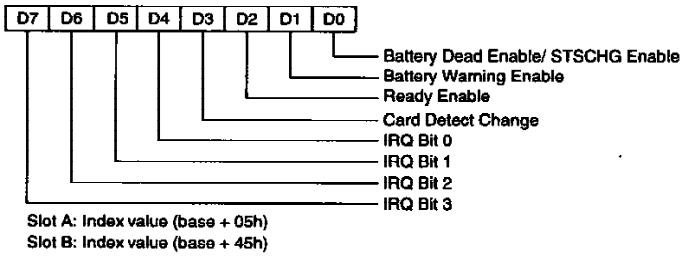

Figure 24. Card Status Change Interrupt Configuration Register (Read/Write)

The relationship between bit 7 through bit 4, and the $\overline{\text{IOCHK}}$ Enable bit of the Interrupt and General Register is shown in *Table 20.*

Table 19. $\overline{\text{IREQ}}$ Level Selected by Card Status Interrupt Configuration Register

$\overline{\text{IOCHK}}$ Enable Bit	IRQ Bit 3	IRQ Bit 2	IRQ Bit 1	IRQ Bit 0	IRQ Level
0	0	0	0	0	Not selected
0	0	0	0	1	Not selected
0	0	0	1	0	Not selected
0	0	0	1	1	IRQ3
0	0	1	0	0	IRQ4
0	0	1	0	1	IRQ5
0	0	1	1	0	Not selected
0	0	1	1	1	IRQ7
0	1	0	0	0	Not selected
0	1	0	0	1	IRQ9
0	1	0	1	0	IRQ10
0	1	0	1	1	IRQ11
0	1	1	0	0	IRQ12
0	1	1	0	1	Not selected
0	1	1	1	0	IRQ14
0	1	1	1	1	IRQ15
1	X	X	X	X	$\overline{\text{IOCHK}}$

Interrupt and General Control Register

The Interrupt and General Control Register is shown in *Figure 25*.

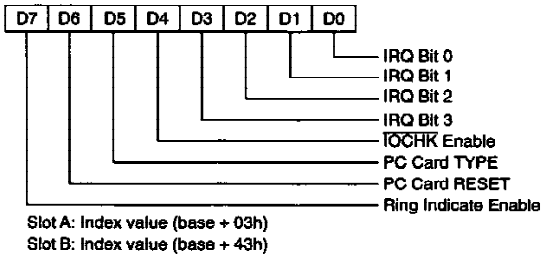

Figure 25. Interrupt and General Control Register (Read/Write)

Bit 4 determines whether to output a $\overline{CSC\_INT}$ signal to IRQ# or $\overline{IOCHK}$. When the I/O Card mode is selected, bit 3 through bit 0 of the Interrupt and General Control Register determine the output pin of a $\overline{IREQ}$ signal from the card, as shown in *Table 20*.

Table 20. $\overline{IREQ}$ Level Selected by Interrupt General Control Register

IRQ Bit 3	IRQ Bit 2	IRQ Bit 1	IRQ Bit 0	IREQ Level
0	0	0	0	Not selected
0	0	0	1	Not selected
0	0	1	0	Not selected
0	0	1	1	IRQ3
0	1	0	0	IRQ4
0	1	0	1	IRQ5
0	1	1	0	Not selected
0	1	1	1	IRQ7
1	0	0	0	Not selected
1	0	0	1	IRQ9
1	0	1	0	IRQ10
1	0	1	1	IRQ11
1	1	0	0	IRQ12
1	1	0	1	Not selected
1	1	1	0	IRQ14
1	1	1	1	IRQ15

Global Control Register

The Global Control Register is shown in *Figure 26*. The bits are defined below.

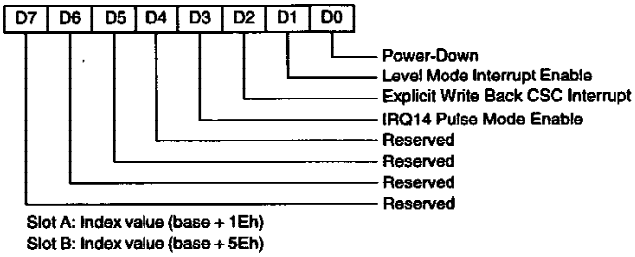

Figure 26. Global Control Register (Read/Write)

Table 21. Global Control Register Description

Bits	Description
Bit 3	**IRQ14 Pulse Mode Enable.** When this bit is "1" and bit 1 is "0," an interrupt assigned to IRQ14 is set to level mode. Note that when bit 1 is set to "1" for level mode this bit is ineffective.
Bit 1	**Level Mode Interrupt Enable.** This bit selects a mode for an interrupt signal, which is output to the IRQ#.When set to "1", level mode interrupt is selected. When set to "0", edge-triggered mode interrupt is selected.

Interrupt Timing Diagrams

The interrupt timing diagrams in different modes are shown *Figure 27* and *Figure 28*.

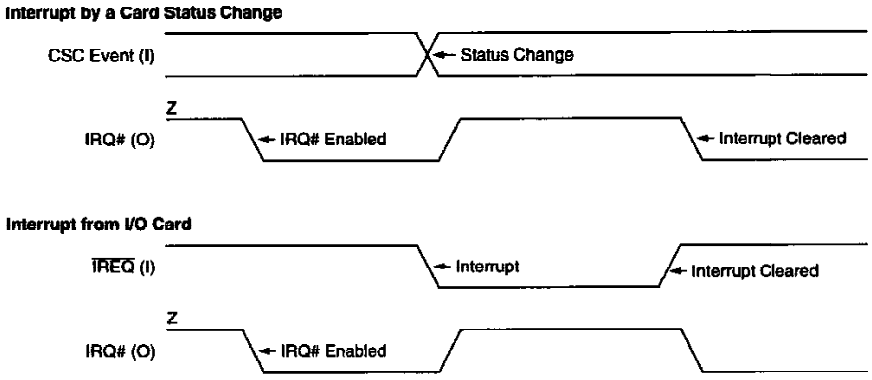

Figure 27. Edge Trigger Mode

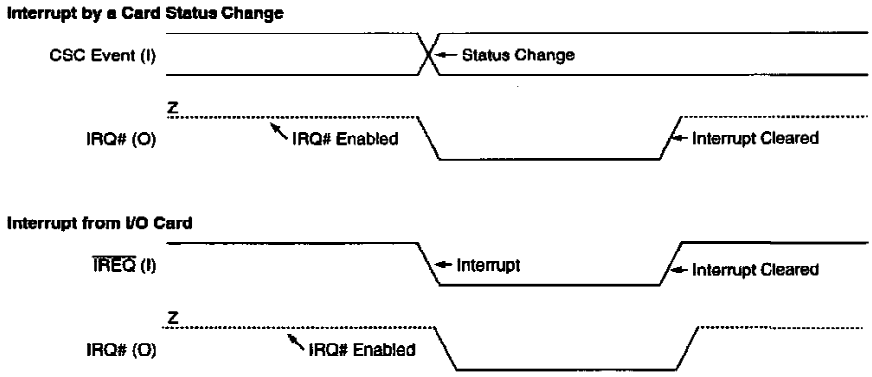

Figure 28. Level Mode

Interrupt Clear

The Card Status Change Interrupt Clear Control Function Block is shown in *Figure 29.*

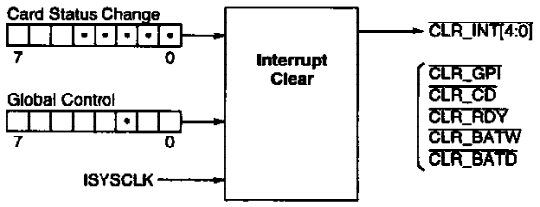

Figure 29. Interrupt Clear Function Block

Global Control Register

The Global Control Register is shown in *Figure 30.* The bit is defined below.

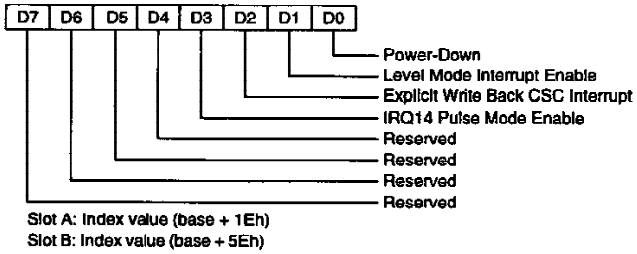

Figure 30. Global Control Register (Read/Write)

Table 22. Global Control Register Description

Bit	Description
Bit 2	**Explicit Write Back CSC Interrupt.** When set to "0", this bit clears all interrupts by reading the Card Status Change Register (Index +04h, +44h). When set to "1" an interrupt is cleared by writing "1" to the corresponding bit of the Card Status Status Change Register (Index +04h, +44h). When the interrupt enable bit of the Card Status Change Interrupt Configuration Register (Index +05h, +55h) and the Card Detect and General Control Register (Index +16h, +56h) are set to disable, the corresponding interrupts are cleared.

I/O Window Mapping

The PCMCIA controller has two I/O windows per slot. The I/O Window Mapping Function Block is shown in *Figure 31*. It decodes a system address IA[15:0] by comparing it according to the following set value of the register.

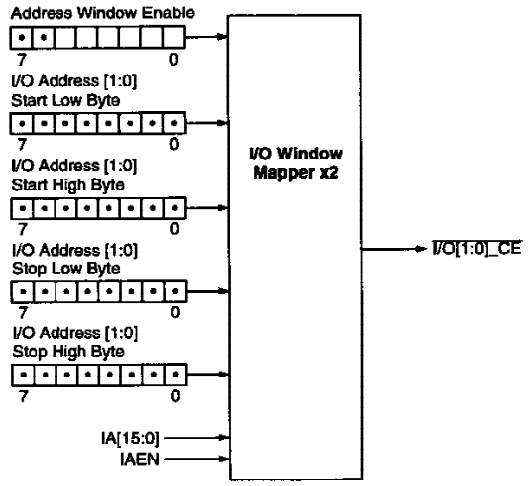

Figure 31. I/O Window Mapping Function Block

Address Window Enable Register

The Address Window Enable Register is shown in *Figure 32*. The bits are defined below.

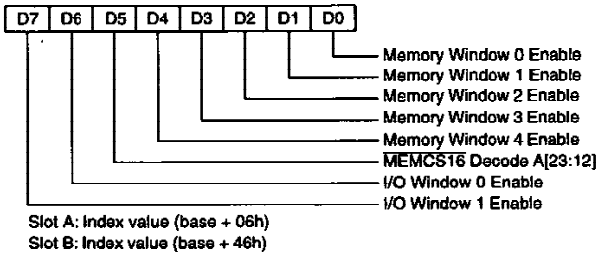

Figure 32. Address Window Enable Register (Read/Write)

Table 23. Address Window Enable Register Description

Bits	Description
Bit 7	**I/O Window 1 Enable.** When set to "1" this bit enables the I/O Window 1.
Bit 6	**I/O Window 0 Enable.** When set to "1" this bit enables the I/O Window 0.

The values set in the next two registers are the start addresses of the I/O windows.

I/O Address # Start Low Byte Register

The I/O Address # Start Low Byte Register is shown in *Figure 33.*

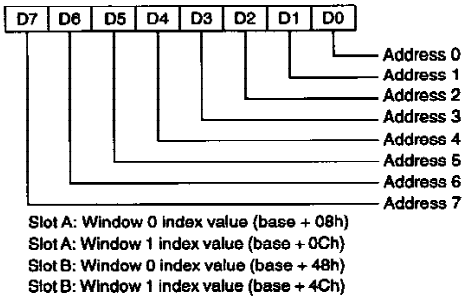

Figure 33. I/O Address # Start Low Byte Register (Read/Write)

I/O Address # Start High Byte Register

The I/O Address # Start High Byte Register is shown in *Figure 34.*

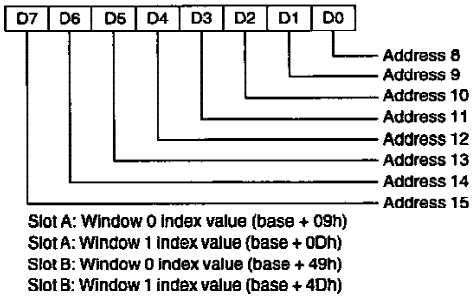

Figure 34. I/O Address # Start High Byte Register (Read/Write)

The values set in the next two registers are the end addresses of the I/O Windows.

I/O Address # Stop Low Byte Register

The I/O Address # Stop Low Byte Register is shown in *Figure 35*.

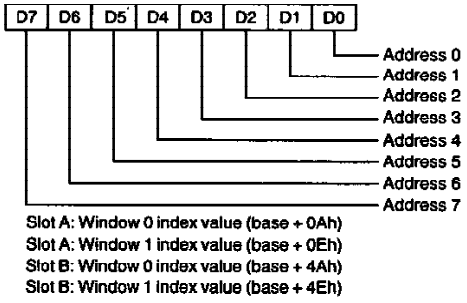

Figure 35. I/O Address # Stop Low Byte Register (Read/Write)

I/O Address # Stop High Byte Register

The I/O Address # Stop High Byte Register is shown in *Figure 36*.

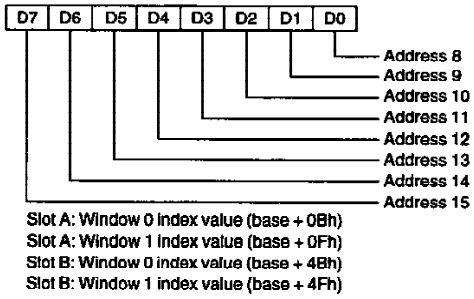

Figure 36. I/O Address # Stop High Byte Register (Read/Write)

I/O Window Control

The I/O Window Control Function Block is shown in *Figure 37*.

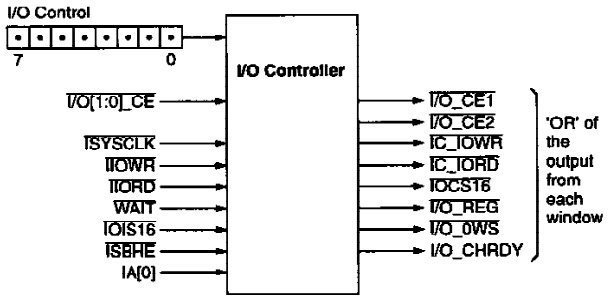

Figure 37. I/O Window Control Function Block

I/O Control Register

The I/O Control Register is shown in *Figure 38*. The bits are defined below.

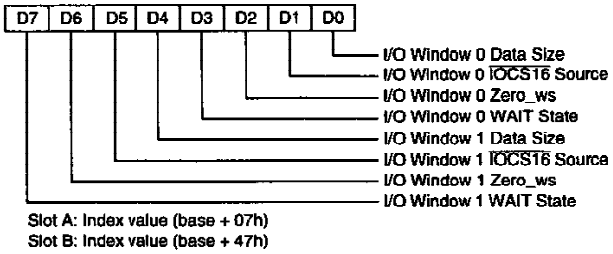

Figure 38. I/O Control Register (Read/Write)

Table 24. I/O Control Register Description

Bits	Description
Bit 7 / Bit 3	**I/O Window 1 WAIT State / I/O Window 0 WAIT State.** When these bits are set to "1" and a 16-bit I/O access is carried out, an I/O_CHRDY signal is made effective. *Table 25* shows the I/O_CHRDY output function.
Bit 6 / Bit 2	**I/O Window 1 Zero_ws/ I/O Window 0 Zero_ws.** When these bits are set to "1" and an 8-bit I/O access is carried out, an $\overline{\text{I/O\_0WS}}$ signal is effective. *Table 26* shows the $\overline{\text{I/O\_0WS}}$ output functions.
Bit 5/ Bit 1	**I/O Window 1 $\overline{\text{IOCS16}}$ Source / I/O Window 0 $\overline{\text{IOCS16}}$ Source.** When these bits are set to "1" a $\overline{\text{IOCS16}}$ signal is generated from a $\overline{\text{IOIS16}}$ signal; when these bits are set to "0" a $\overline{\text{IOCS16}}$ signal is generated from bit 4/bit 0.
Bit 4 / Bit 0	**I/O Window 1 Data Size / I/O Window 0 Data Size.** When these bits are set to "1" a 16-bit access is enabled; when sese bits are set to "0" an 8-bit access is enabled. Note that the value is "No" when IA[0] = 0 and $\overline{\text{ISBHE}}$ = 0. *Table 27* shows the $\overline{\text{IOCS16}}$ output function.

Table 25. I/O_CHRDY Output Function

$\overline{WAIT}$	Bit 7 / Bit 3	$\overline{IOCS16}$	I/O_CHRDY
1	0	0	No
1	0	1	No
1	1	0	Yes
1	1	1	No
0	X	X	Yes

Table 26. $\overline{I/O\_0WS}$ Output Functions

$\overline{WAIT}$	Bit 6 / Bit 2	$\overline{IOCS16}$	$\overline{I/O\_0WS}$
1	0	0	No
1	0	1	No
1	1	0	No
1	1	1	Yes
0	X	X	No

Table 27. $\overline{IOCS16}$ Output Function

Bit 5 / Bit 1	Bit 4 / Bit 0	$\overline{IOIS16}$	$\overline{IOCS16}$
0	0	X	1
0	1	X	0
1	X	0	0
1	X	1	1

The control of $\overline{I/O\_CE1}$ and $\overline{I/O\_CE2}$ is shown in *Table 28.*

Table 28. $\overline{I/O\_CE1}$ and $\overline{I/O\_CE2}$ Output Function

$\overline{IOCS16}$	$\overline{SBHE}$	IA[0]	$\overline{I/O\_CE1}$	$\overline{I/O\_CE2}$
0	0	0	0	0
0	0	1	1	0
0	1	X	0	1
1	X	X	0	1

Memory Window Mapping

The PCMCIA controller has five memory windows per slot. The Memory Window Mapping Function Block is shown in *Figure 39*. $\overline{\text{MEM[4:0]\_CE}}$ is obtained by decoding a system address ISA[23:12]. ISA[23:17] is obtained by latching ILA[23:17] with IBALE. $\overline{\text{MEM[4:0]\_CE16}}$ is obtained by decoding ILA[23:17] and is used for generating a $\overline{\text{MEMCS16}}$ signal.

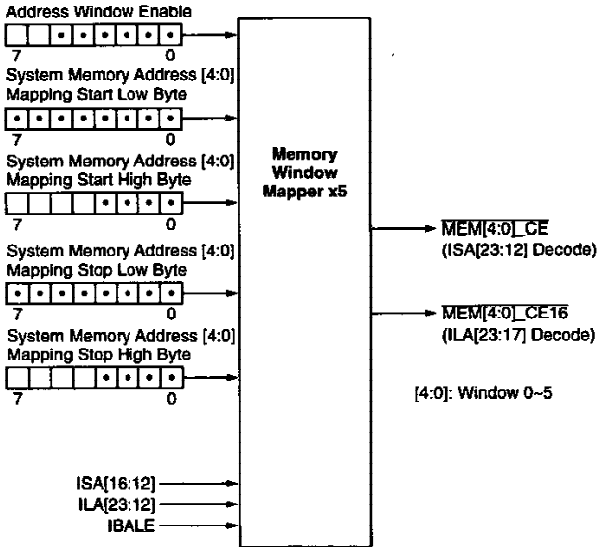

Figure 39. Memory Window Mapping Function Block

Address Window Enable Register

The Address Window Enable Register is shown in *Figure 40*. The bits are defined below.

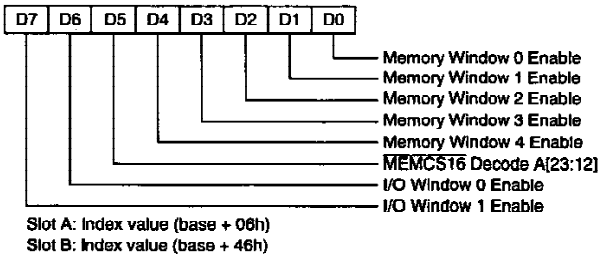

Figure 40. Address Window Enable Register (Read/Write)

Table 29. Address Window Enable Register Description

Bits	Description
Bit 5	**MEMCS16 Decode A[23:12].** When this bit is set to "1" a $\overline{\text{MEMCS16}}$ signal is generated by decoding ISA[23:12]; when this bit is set to "0" a $\overline{\text{MEMCS16}}$ signal is generated by decoding ILA[23:17].
Bit 4	**Memory Window 4 Enable.** When this bit is set to "1" Memory Window 4 is active.
Bit 3	**Memory Window 3 Enable.** When this bit is set to "1" Memory Window 3 is active.
Bit 2	**Memory Window 2 Enable.** When this bit is set to "1" Memory Window 2 is active.
Bit 1	**Memory Window 1 Enable.** When this bit is set to "1" Memory Window 1 is active.
Bit 0	**Memory Window 0 Enable.** When this bit is set to "1" Memory Window 0 is active.

The values set in the next two registers are the start addresses of the Memory Windows.

System Memory Address # Mapping Start Low Byte Register

The System Memory Address # Mapping Start Low Byte Register is shown in *Figure 41*.

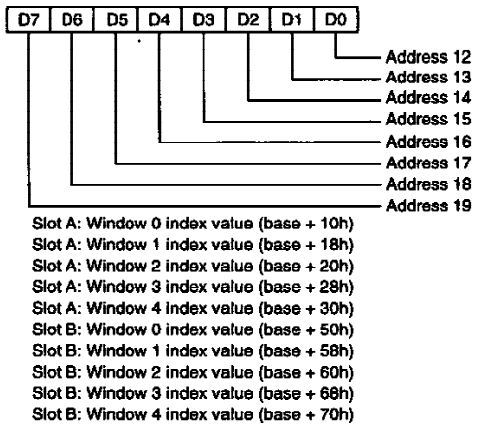

Figure 41. Address Window Enable Register (Read/Write)

System Memory Address # Mapping Start High Byte Register

The System Memory Address # Mapping Start High Byte Register is shown in *Figure 42*.

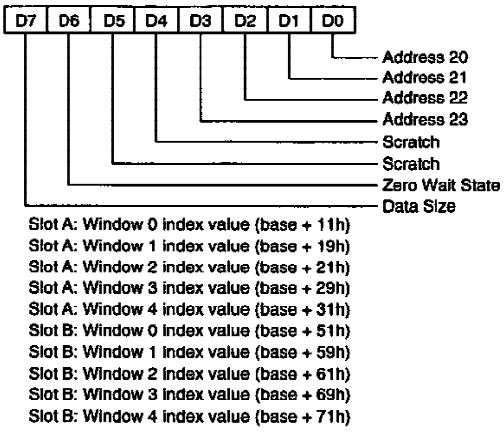

Figure 42. System Memory Address # Mapping Start High Byte Register (Read/Write)

The values set in the next two registers are the end addresses of the Memory Windows.

System Memory Address # Mapping Stop Low Byte Register

The System Memory Address # Mapping Stop Low Byte Register is shown in *Figure 43*.

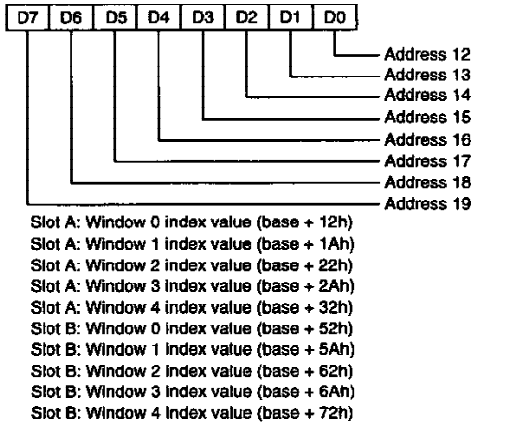

Figure 43. System Memory Address # Mapping Stop Low Byte Register (Read/Write)

System Memory Address # Mapping Stop High Byte Register

The System Memory Address # Mapping Stop High Byte Register is shown in *Figure 44*.

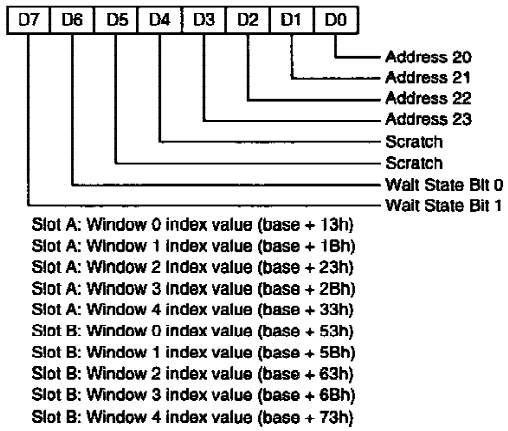

Figure 44. System Memory Address # Mapping Stop High Byte Register (Read/Write)

Card Memory Address Relocation

The Card Memory Address Relocation Function Block and the Card Memory Address Multiplex Function Block is shown in *Figure 45*. The card memory address relocation function enables access to a maximum of 64M bytes of the memory in the card via the allocated system Memory Window. MEM4_CA[25:12] to MEM0_CA[25:12] are generated by adding the offset value of the card memory to be accessed to ISA[23:12]. An offset value is set in the following registers.

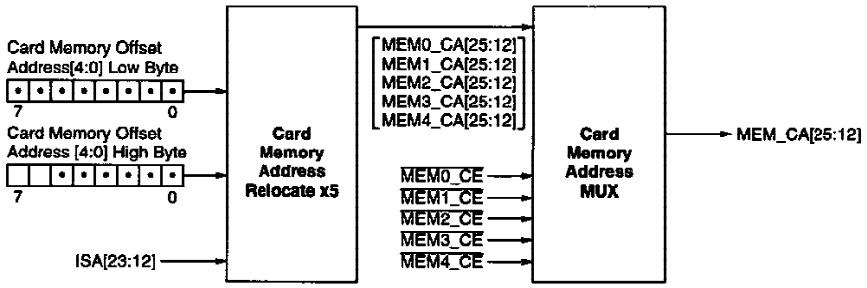

Figure 45. Memory Window Mapping Function Block

The card memory address multiplex selects MEM4_CA[25:12] to MEM0_CA[25:12] which corresponds to a window that becomes active ($\overline{MEM4\_CE}$ to $\overline{MEM0\_CE}$ = 0). Note that MEM4_CA[25:12] to MEM0_CA[25:12] have priority relationship. MEM0_CA[25:12] has the highest priority, while MEM4_CA[25:12] has the lowest.

Card Memory Offset Address # Low Byte Register

The Card Memory Offset Address # Low Byte Register is shown in *Figure 46*.

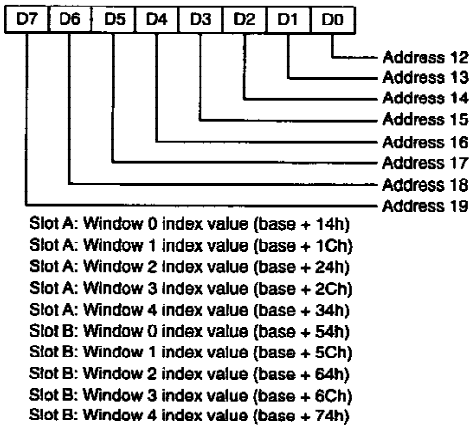

Figure 46. Card Memory Offset Address # Low Byte Register (Read/Write)

Card Memory Offset Address # Low Byte Register

The Card Memory Offset Address # Low Byte Register as shown in *Figure 47*.

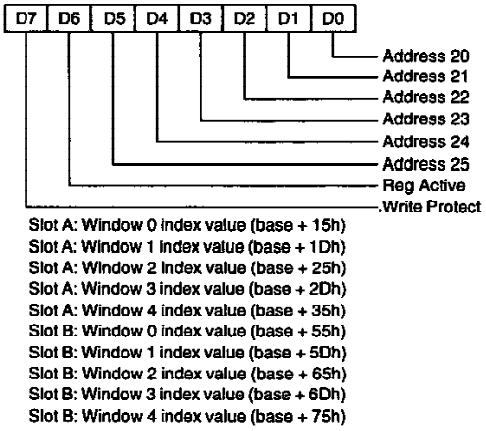

Figure 47. Card Memory Offset Address # High Byte Register (Read/Write)

Set value of address 25-12 = start address of card memory to be accessed, and start address of system Memory Window.

Memory Window Control

The Memory Window Control Function Block controls 8-bit/16-bit access to the system bus, memory commands to the card, as well as common/attribute and card enable, as shown in *Figure 48.*

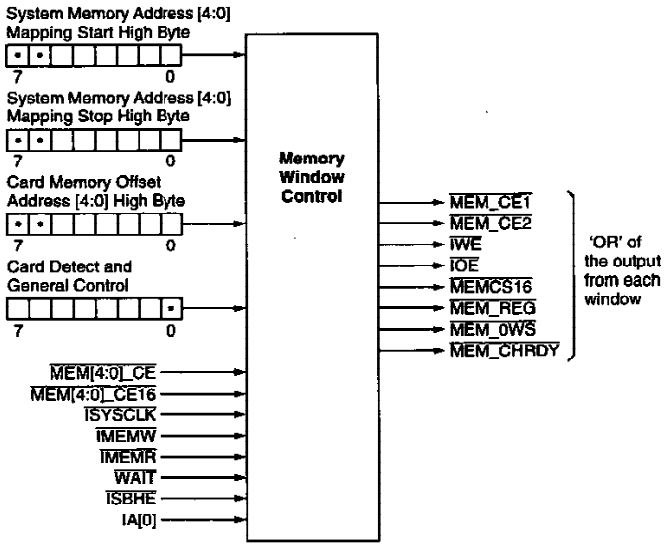

Figure 48. Memory Window Control Function Block

System Memory Address # Mapping Start High Byte Register

The System Memory Address # Mapping Start High Byte Register as shown in *Figure 49*. The bits are defined below.

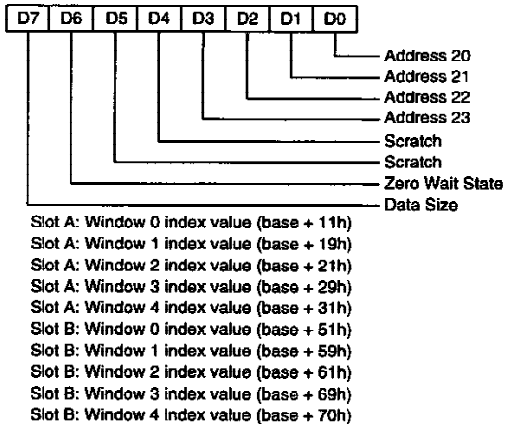

Figure 49. System Memory Address # Mapping Start High Byte Register (Read/Write)

Table 30. System Memory Address # Mapping Start High Byte Register Description

Bits	Description
Bit 7	**Data Size.** When this bit is set to "0", an 8-bit memory access is active; when this bit is set to "1", a 16-bit memory access with $\overline{\text{MEMCS16}}$ signal is made active. *Table 31* shows the control of $\overline{\text{MEM\_CE1}}$ and $\overline{\text{MEM\_CE2}}$.
Bit 6	**Zero Wait State.** When this bit is set to "0," no $\overline{\text{MEM\_0WS}}$ signal is generated; when this bit is set to "1" and $\overline{\text{MEM\_CHRDY}}$ is inactive, the $\overline{\text{MEM\_0WS}}$ signal is generated. Note that the $\overline{\text{MEM\_0WS}}$ signal does not become active in case of 8 bits, A0=0, and $\overline{\text{SBHE}}$=0. *Table 32* shows the $\overline{\text{MEM\_0WS}}$ output function.

Table 31. $\overline{\text{MEM\_CE1}}$ and $\overline{\text{MEM\_CE2}}$ Control

Bit 7	$\overline{\text{SBHE}}$	IA [0]	$\overline{\text{MEM\_CE1}}$	$\overline{\text{MEM\_CE2}}$
1	0	0	0	0
1	0	1	1	0
1	1	X	0	1
0	X	X	0	1

Table 32. $\overline{\text{MEM\_0WS}}$ Output Function

Bit 7	Bit 6	$\overline{\text{MEM\_CHRDY}}$	$\overline{\text{MEM\_0WS}}$
X	0	X	No
0	1	No	Yes
1	1	No	Yes
X	1	Yes	No

Note: $\overline{\text{MEM\_0WS}}$=No if A0=0 and $\overline{\text{SBHE}}$=0

System Memory Address # Mapping Stop High Byte Register

The System Memory Address # Mapping Stop High Byte Register is shown in *Figure 50*. The bits are defined below.

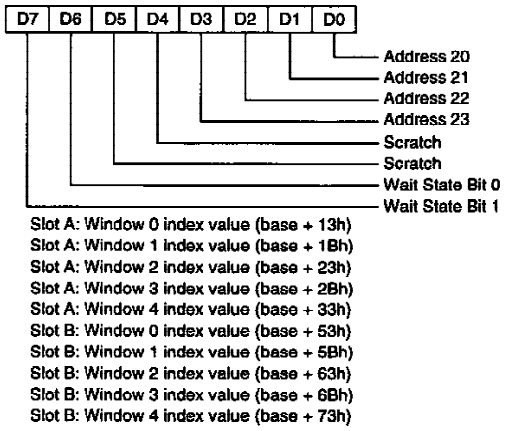

Figure 50. System Memory Address # Mapping Stop High Byte Register (Read/Write)

Table 33. System Memory Address # Mapping Stop High Byte Register Description

Bits	Description
Bit 7 / Bit 6	**Wait State Bit 1/0.** The wait count of $\overline{\text{MEM\_CHRDY}}$ generated within the controller is set. It is effective at the time of 16-bit access only. The $\overline{\text{MEM\_CHRDY}}$ output function is shown in *Table 34*.

Table 34. $\overline{\text{MEM\_CHRDY}}$ Output Function

Start High Byte Register Bit 7	Bit 7	Bit 6	$\overline{\text{WAIT}}$	$\overline{\text{MEM\_CHRDY}}$
0	X	X	No	No
0	X	X	Yes	Yes ($\overline{\text{WAIT}}$)
1	0	0	No	No
1	0	1	No	Yes (1 WAIT)
1	1	0	No	Yes (2 WAIT)
1	1	1	No	Yes (3 WAIT)
1	0	1	Yes	Yes (1 WAIT or $\overline{\text{WAIT}}$)
1	1	0	Yes	Yes (2 WAIT or $\overline{\text{WAIT}}$)
1	1	1	Yes	Yes (3 WAIT or $\overline{\text{WAIT}}$)

Card Detect and General Control Register

The Card Detect and General Control Register as shown in *Figure 51*. The bit is defined below.

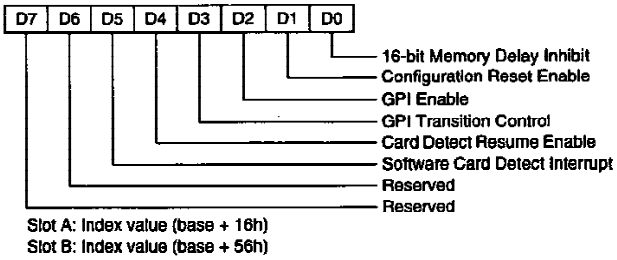

Figure 51. Card Detect and General Control Register (Read/Write)

Table 35. Card Detect and General Control Register Description

Bit	Description
Bit 0	**16-Bit Memory Delay Inhibit.** When this bit is set to "0" if 16-bit access (bit 7 of System Memory Address # Mapping Start High Byte Register is "1"), $\overline{IWE}$ and $\overline{IOE}$ signals are output by one-stage synchronization of $\overline{IMEMW}$ and $\overline{IMEMR}$, with the falling edge of ISYSCLK. When this bit is set to "1" $\overline{IWE}$ and $\overline{IOE}$ signals are always output asynchronously with ISYSCLK. The timing diagram of ISYSCLK synchronization of $\overline{IWE}$, $\overline{IOE}$ is shown in *Figure 52*.

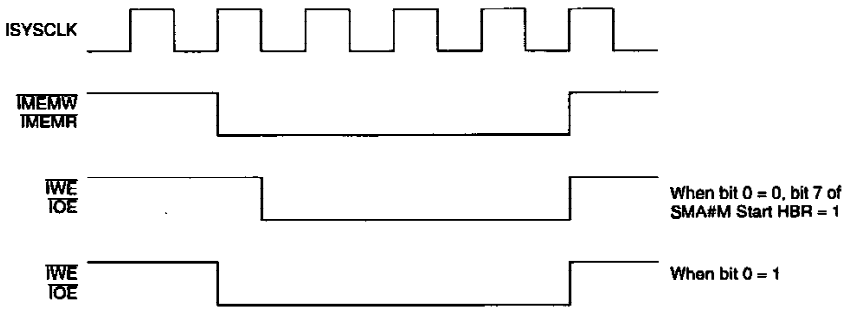

Figure 52. Timing Diagram of ISYSCLK Synchronization of $\overline{IWE}$, $\overline{OWE}$

The ISYSCLK synchronization of the $\overline{IWE}$, $\overline{IOE}$ is shown in *Table 36*.

Table 36. ISYSCLK Synchronization of the $\overline{IWE}$, $\overline{IOE}$

Bit 7 of SMA#M Start HBR	Bit 0	ISYSCLK Sychronization of $\overline{IWE}$, $\overline{IOE}$
0	X	No
1	0	Yes
1	1	No

Card Memory Offset Address # High Byte Register

The Card Memory Offset Address # High Byte Register is shown in *Figure 53*. The bits are defined below.

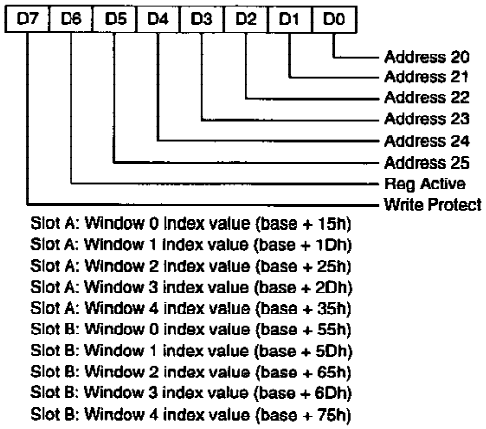

Figure 53. Card Memory Offset Address # High Byte Register (Read/Write)

Table 37. Card Memory Offset Address # High Byte Register Description

Bits	Description
Bit 7	**Write Protect.** When this bit is set to "1," it enables forced write protection by making $\overline{IWE}$ 'H'.
Bit 6	**Reg Active.** When this bit is set to "1," access to the attribute memory space is enabled by outputting an active $\overline{IREG}$ signal.

I/O, Memory Signal OR

The I/O, Memory Signal 'OR' Function Block is shown in *Figure 54*. It outputs $\overline{0WS}$, IOCHRDY, $\overline{ICE1}$, $\overline{ICE2}$, and $\overline{IREG}$ signals by taking the OR of the $\overline{I/O\_0WS}$, I/O_CHRDY, / $\overline{I/O\_CE1}$, $\overline{I/O\_CE2}$, and $\overline{I/O\_REG}$ signals generated by the I/O Control Block, and the $\overline{MEM\_0WS}$, MEM_CHRDY, $\overline{MEM\_CE1}$, $\overline{MEM\_CE2}$, and $\overline{MEM\_REG}$ signals generated by the Memory Control Block.

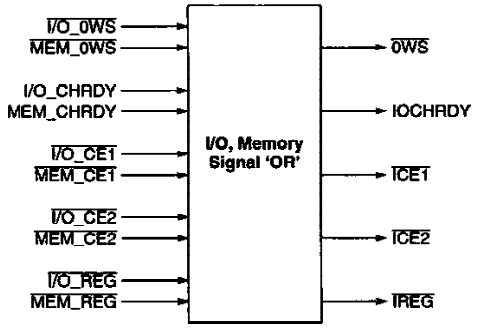

Figure 54. I/O, Memory Signal 'OR' Function Block