

54193, 54LS193 Counters

Presettable 4-Bit Binary Up/Down Counters

Product Specification

Military Logic Products

FEATURES

- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset (clear)
- Expandable without external logic

DESCRIPTION

The 54193 and 54LS193 are 4-bit synchronous up/down counters – that count in

the binary mode. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the Low-to-High transition of either Clock input. If the CP_U clock is pulsed while CP_D is held High, the device will count up ... if CP_D is pulsed while the CP_U is held High, the device will count down. Only one Clock input can be held High at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous reset pin –

it may also be loaded in parallel by activating the asynchronous parallel load pin.

ORDERING INFORMATION

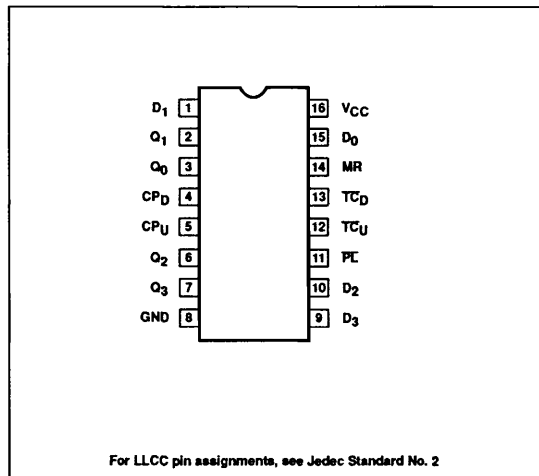
| DESCRIPTION | ORDER CODE |
|-------------------|--------------------------|
| Ceramic DIP | 54193/BEA 54LS193/BEA |
| Ceramic Flat Pack | 54193/BFA 54LS193/BFA |
| Ceramic LLCC | 54LS193/B2A |

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

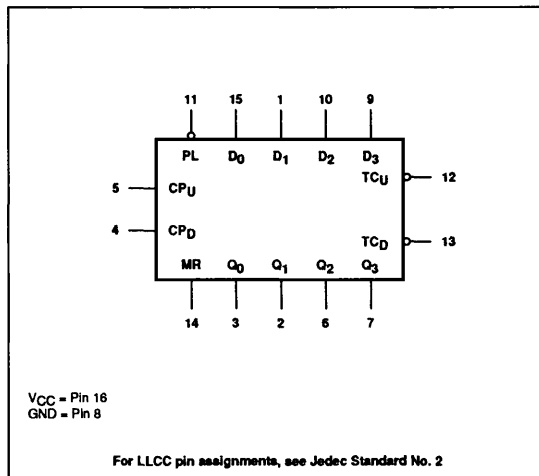
| PINS | DESCRIPTION | 54 | 54LS |
|------|-------------|------|--------|
| All | Inputs | 1UL | 1LSUL |
| All | Outputs | 10UL | 10LSUL |

NOTE: Where a 54 Unit Load (UL) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 54LS Unit Load (LSUL) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

PIN CONFIGURATION



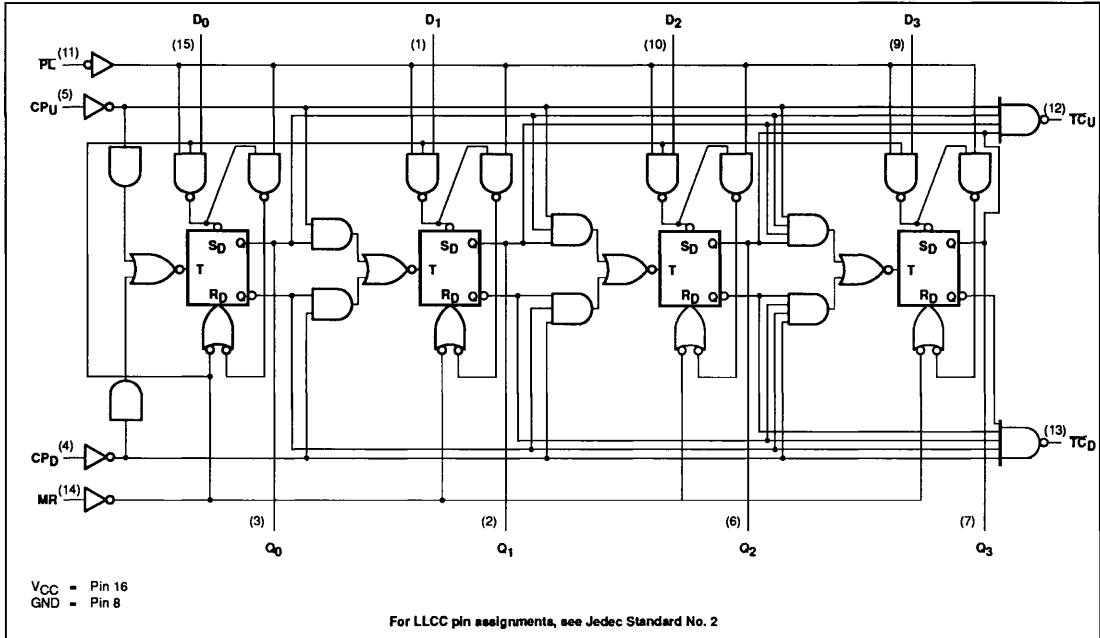
LOGIC SYMBOL



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LOGIC DIAGRAM



Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count-up and count-down functions.

Each flip-flop contains JK feedback from slave to master, such that a Low-to-High transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

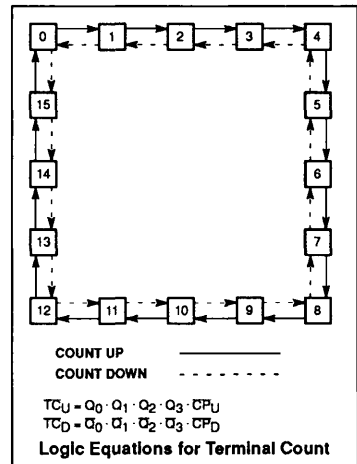
One clock should be held High while counting with the other, because the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is Low. Applications requiring reversible operation must make the reversing decision while the activating clock is High to avoid erroneous counts.

The Terminal Count Up (TC_U) and Terminal Count down (TC_D) outputs are normally High. When the circuit has reached the maximum count state of the next High-to-Low transition of CP_U will cause TC_U to go Low. TC_U will stay Low until CP_U goes High again, duplicating the

count up clock, although delayed by two gate delays. Likewise, the TC_D output will go Low when the circuit is in the zero state and the CP_D goes Low. The TC outputs can be used as the Clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a two-gate delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs ($D_0 - D_3$) is loaded into the counter and appears on the outputs regardless of the conditions of the Clock inputs when the Parallel Load (PL) input is Low. A High level on the Master Reset (MR) input will disable the parallel load gates, override both Clock inputs, and set all Q outputs Low. If one of the Clock inputs is Low during and after a reset or load operation, the next Low-to-High transition of that clock will be interpreted as a legitimate signal and will be counted.

STATE DIAGRAM



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MODE SELECT — FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | | | | | OUTPUTS | | | | | |
|----------------|--------|----|-----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|
| | MR | PL | CP _U | CP _D | D ₀ | D ₁ | D ₂ | D ₃ | Q ₀ | Q ₁ | Q ₂ | Q ₃ | TC _U | TC _D |
| Reset (clear) | H | X | X | L | X | X | X | X | L | L | L | L | H | L |
| | H | X | X | H | X | X | X | X | L | L | L | L | H | H |
| Parallel load | L | L | X | L | L | L | L | L | L | L | L | L | H | L |
| | L | L | X | H | L | L | L | L | L | L | L | L | H | H |
| | L | L | L | X | H | H | H | H | H | H | H | H | L | H |
| | L | L | H | X | H | H | H | H | H | H | H | H | H | H |
| Count up | L | H | ↑ | H | X | X | X | X | Count up | | | | H ^(c) | H |
| Count down | L | H | H | ↑ | X | X | X | X | Count down | | | | H | H ^(d) |

H = High voltage level

L = Low voltage level

X = Don't care

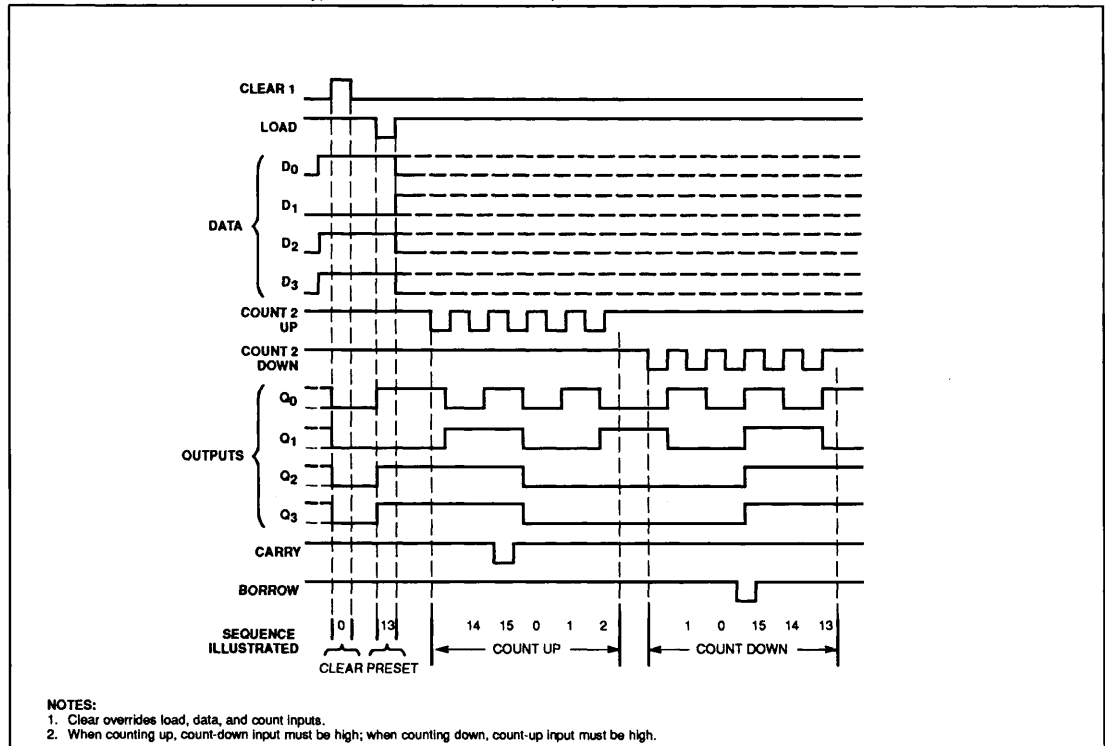
↑ = Low-to-High clock transition

NOTES:

c. TC_U = CP_U at terminal count up (HHHH)

d. TC_D = CP_D at terminal count down (LLLL)

FUNCTIONAL WAVEFORMS Typical clear, load, and count sequences



NOTES:

1. Clear overrides load, data, and count inputs.

2. When counting up, count-down input must be high; when counting down, count-up input must be high.

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ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | 54 | 54LS | UNIT |
|------------------|--|--------------------------|--------------------------|------|
| V _{CC} | Supply voltage | 7.0 | 7.0 | V |
| V _I | Input voltage range | -0.5 to +5.5 | -0.5 to +7.0 | V |
| I _I | Input current range | -30 to +5 | -30 to +1 | mA |
| V _O | Voltage applied to output in High output state range | -0.5 to +V _{CC} | -0.5 to +V _{CC} | V |
| T _{STG} | Storage temperature range | -65 to +150 | | °C |

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | 54 | | | 54LS | | | UNIT |
|-----------------|--------------------------------------|-----|-----|------|------|-----|------|------|
| | | Min | Nom | Max | Min | Nom | Max | |
| V _{CC} | Supply voltage | 4.5 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | High-level input voltage | 2.0 | | | 2.0 | | | V |
| V _{IL} | Low-level input voltage | | | +0.8 | | | +0.7 | V |
| I _{IK} | Input clamp current | | | -12 | | | -18 | mA |
| I _{OH} | High-level output current | | | -800 | | | -400 | μA |
| I _{OL} | Low-level output current | | | 16 | | | 4 | mA |
| T _A | Operating free-air temperature range | -55 | | +125 | -55 | | +125 | °C |

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS ¹ | 54193 | | | 54LS193 | | | UNIT |
|------------------|---|--|-----------------------|------------------|------|---------|------------------|------|------|
| | | | Min | Typ ² | Max | Min | Typ ² | Max | |
| V _{OH} | High-level output voltage | V _{CC} = Min, V _{IH} = Min, V _{IL} = Max, I _{OH} = Max | 2.4 | 3.4 | | 2.5 | 3.4 | | V |
| V _{OL} | Low-level output voltage | V _{CC} = Min, V _{IH} = Min, V _{IL} = Max, I _{OL} = Max | | 0.2 | 0.4 | | 0.25 | 0.4 | V |
| V _{IK} | Input clamp voltage | V _{CC} = Min, I _I = I _{IK} | | | -1.5 | | | -1.5 | V |
| I _{IH2} | Input current at maximum input voltage | V _{CC} = Max | V _I = 5.5V | | 1.0 | | | | mA |
| | | | V _I = 7.0V | | | | | 0.1 | mA |
| I _{IH1} | High-level input current | V _{CC} = Max | V _I = 2.4V | | 40 | | | | μA |
| | | | V _I = 2.7V | | | | | 20 | μA |
| I _{IL} | Low-level input current | V _{CC} = Max, V _I = 0.4V | | | -1.6 | | -0.4 | mA | |
| I _{OS} | Short-circuit output current ³ | V _{CC} = Max | -20 | | -65 | -20 | -100 | mA | |
| I _{CC} | Supply current ⁴ (total) | V _{CC} = Max | | 65 | 89 | | 19 | 34 | mA |

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V⁵

| SYMBOL | PARAMETER | TEST CONDITIONS | 54 | | 54LS | | UNIT |
|--------------------------------------|---|-----------------|-----------------------|----------|-----------------------|----------|----------|
| | | | C _L = 15pF | | C _L = 15pF | | |
| | | | Min | Max | Min | Max | |
| f _{MAX} | Maximum input count frequency | Waveform 1 | 25 | | 25 | | MHz |
| t _{PLH} t _{PHL} | Propagation delay CP _U input to TC _U output | Waveform 2 | | 26 24 | | 26 24 | ns ns |
| t _{PLH} t _{PHL} | Propagation delay CP _D input to TC _D output | Waveform 2 | | 24 24 | | 24 24 | ns ns |
| t _{PLH} t _{PHL} | Propagation delay CP _U or CP _D to Q _n outputs | Waveform 1 | | 38 47 | | 38 47 | ns ns |
| t _{PLH} t _{PHL} | Propagation delay PC input to Q _n output | Waveform 3 | | 40 40 | | 40 40 | ns ns |
| t _{PHL} | Propagation delay MR to output | Waveform 4 | | 35 | | 35 | ns |

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AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

| SYMBOL | PARAMETER | TEST CONDITIONS | 54 | | 54LS | | UNIT |
|-----------|-------------------------|-----------------|-----|-----|------|-----|------|
| | | | Min | Max | Min | Max | |
| t_{W} | CP_U pulse width | Waveform 1 | 20 | | 20 | | ns |
| t_{W} | CP_D pulse width | Waveform 1 | 20 | | 20 | | ns |
| t_{W} | PL pulse width | Waveform 3 | 20 | | 20 | | ns |
| t_{W} | MR pulse width | Waveform 4 | 20 | | 20 | | ns |
| t_s | Setup time, data to PL | Waveform 5 | 20 | | 20 | | ns |
| t_h | Hold time, data to PL | Waveform 5 | 0 | | 5 | | ns |
| t_{rec} | Recovery time, PL to CP | Waveform 3 | 40 | | 40 | | ns |
| t_{rec} | Recovery time, MR to CP | Waveform 4 | 40 | | 40 | | ns |

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

| SYMBOL | PARAMETER | TEST CONDITIONS | 54 | | 54LS | | UNIT |
|------------------------|--|-----------------|---------------------|----------|---------------------|----------|----------|
| | | | $C_L = 50\text{pF}$ | | $C_L = 50\text{pF}$ | | |
| | | | Min | Max | Min | Max | |
| f_{MAX} | Maximum input count frequency | Waveform 1 | 25 | | 25 | | MHz |
| t_{PLH} t_{PHL} | Propagation delay CP_U input to TC_U output | Waveform 2 | | 30 28 | | 31 29 | ns ns |
| t_{PLH} t_{PHL} | Propagation delay CP_D input to TC_D output | Waveform 2 | | 28 28 | | 29 29 | ns ns |
| t_{PLH} t_{PHL} | Propagation delay CP_U or CP_D to Q_n outputs | Waveform 1 | | 42 51 | | 43 52 | ns ns |
| t_{PLH} t_{PHL} | Propagation delay PL input to Q_n output | Waveform 3 | | 44 44 | | 45 45 | ns ns |
| t_{PHL} | Propagation delay MR to output | Waveform 4 | | 39 | | 40 | ns |

AC ELECTRICAL CHARACTERISTICS $T_A = -55^\circ\text{C}$ and $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V}^5$

| SYMBOL | PARAMETER | TEST CONDITIONS | 54 | | 54LS | | UNIT |
|------------------------|--|-----------------|---------------------|----------|---------------------|----------|----------|
| | | | $C_L = 50\text{pF}$ | | $C_L = 50\text{pF}$ | | |
| | | | Min | Max | Min | Max | |
| f_{MAX} | Maximum input count frequency | Waveform 1 | 25 | | 25 | | MHz |
| t_{PLH} t_{PHL} | Propagation delay CP_U input to TC_U output | Waveform 2 | | 39 36 | | 40 38 | ns ns |
| t_{PLH} t_{PHL} | Propagation delay CP_D input to TC_D output | Waveform 2 | | 36 36 | | 38 38 | ns ns |
| t_{PLH} t_{PHL} | Propagation delay CP_U or CP_D to Q_n outputs | Waveform 1 | | 55 66 | | 56 68 | ns ns |
| t_{PLH} t_{PHL} | Propagation delay PL input to Q_n output | Waveform 3 | | 57 57 | | 59 59 | ns ns |
| t_{PHL} | Propagation delay, MR to output | Waveform 4 | | 51 | | 52 | ns |

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AC SETUP REQUIREMENTS $T_A = -55^\circ\text{C}$ and $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V}^5$

| SYMBOL | PARAMETER | TEST CONDITIONS | 54 | | 54LS | | UNIT |
|-----------|--------------------------------------|-----------------|-----|-----|------|-----|------|
| | | | Min | Max | Min | Max | |
| t_W | CP_U pulse width | Waveform 1 | 26 | | 20 | | ns |
| t_W | CP_D pulse width | Waveform 1 | 26 | | 20 | | ns |
| t_W | PL pulse width | Waveform 3 | 20 | | 20 | | ns |
| t_W | MR pulse width | Waveform 4 | 20 | | 20 | | ns |
| t_s | Setup time, data to \overline{PL} | Waveform 5 | 20 | | 30 | | ns |
| t_h | Hold time, data to \overline{PL} | Waveform 5 | 0 | | 10 | | ns |
| t_{rec} | Recovery time, \overline{PL} to CP | Waveform 3 | 40 | | 40 | | ns |
| t_{rec} | Recovery time, MR to CP | Waveform 4 | 40 | | 40 | | ns |

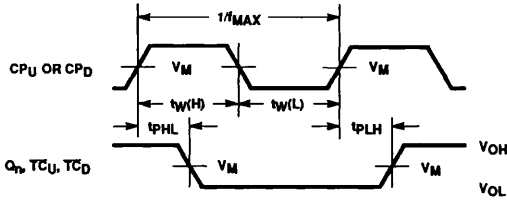
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
3. Not more than one output should be shorted at a time, and duration of the short should not exceed one second.
4. Measure I_{CC} with Parallel Load and Master Reset inputs grounded, all other outputs $\geq 4.0\text{V}$ and all outputs open.
5. These parameters are guaranteed, but not tested.

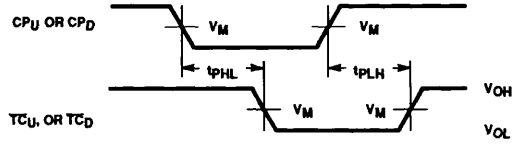
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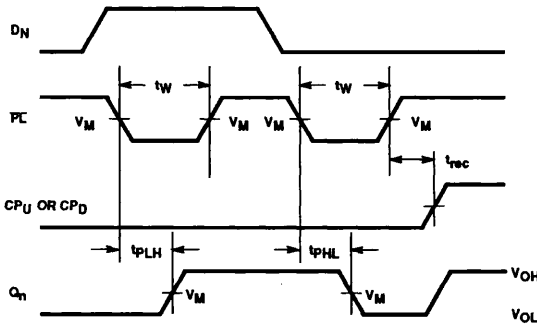
AC WAVEFORMS



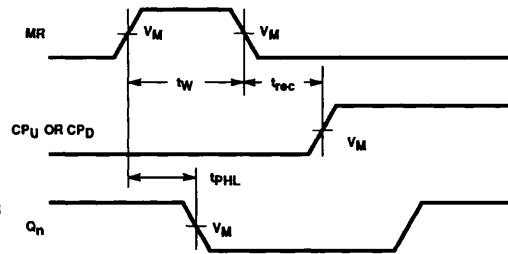
Waveform 1. Clock to Output Delays and Clock Pulse Width



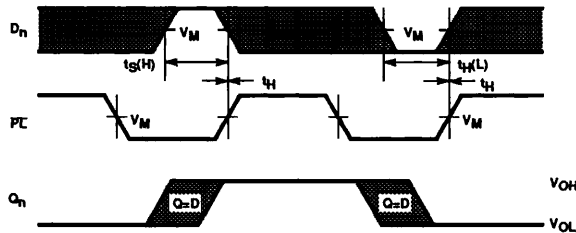
Waveform 2. Clock to Terminal Count Delays



Waveform 3. Parallel Load Pulse Width, Parallel Load to Output Delays, and Parallel Load to Clock Recovery Time



Waveform 4. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 5. Setup and Hold Times Data to Parallel Load (PL)

NOTE: $V_M = 1.3V$ for 54LS; $V_M = 1.5V$ for all other TTL families.
The shaded areas indicate when the input is permitted to change for predictable output performance.

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TEST CIRCUIT AND WAVEFORM

Test Circuit for 54 Totem-Pole Outputs

Input Pulse Definition

| FAMILY | INPUT PULSE CHARACTERISTICS | | | | | |
|---------|-----------------------------|------|-----------|-------|-------|------|
| | RL | VM | Rep. Rate | TW | TLH | TTHL |
| 54LSXXX | 2.0kΩ | 1.3V | 1MHz | 500ns | ≤15ns | ≤6ns |
| 54XXX | 400Ω | 1.5V | 1MHz | 500ns | ≤7ns | ≤7ns |

DEFINITIONS:
 CL = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
 RT = Termination resistance should be equal to ZOUT of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 Vx = Undocked pins must be held at ≤0.8V, ≥2.7V or open per Function Table.

APPLICATION DIAGRAM

