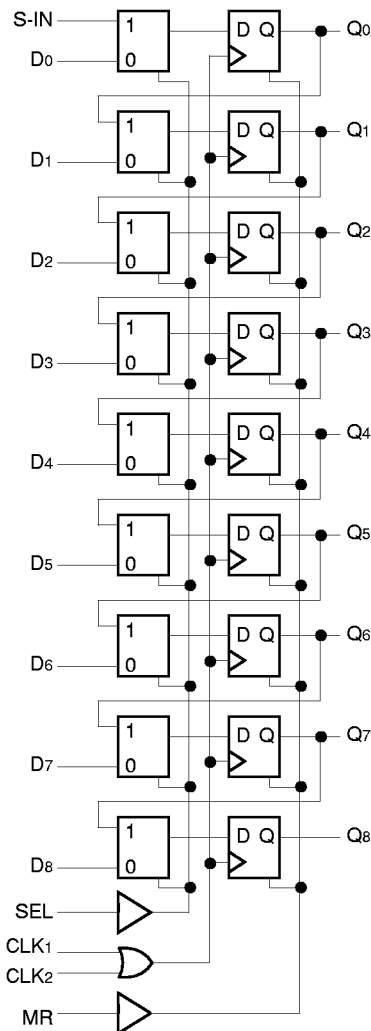


FEATURES

- 700MHz min. shift frequency
- Extended 100E VEE range of -4.2V to -5.5V
- 9 bits wide for byte-parity applications
- Asynchronous Master Reset
- Dual clocks
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- ESD protection of 2000V
- Fully compatible with Motorola MC10E/100E142
- Available in 28-pin PLCC package

BLOCK DIAGRAM



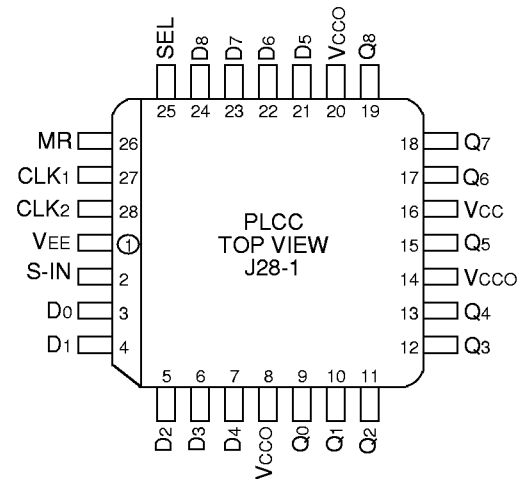
DESCRIPTION

The SY10/100E142 are high-speed 9-bit shift registers designed for use in new, high-performance ECL systems. The E142 can accept serial or parallel data to be shifted out in one direction as both serial and parallel outputs. The nine inputs, D₀-D₈, accept parallel input data, while S-IN accepts serial input data.

The SEL (Select) control pin serves to determine the mode of operation, either SHIFT or LOAD. The shift direction is from bit 0 to bit 8. The input data has to meet the set-up time before being clocked into the nine input registers on the rising edge of CLK₁ or CLK₂. Shifting is also performed on the rising edge of either CLK₁ or CLK₂. The MR (Master Reset) control signal asynchronously resets all nine registers to a logic LOW when a logic HIGH is applied to MR.

The E142 is designed for applications such as diagnostic scan registers, parallel-to-serial conversions and is also suitable for byte-wide parity.

PIN CONFIGURATION



PIN NAMES

Pin	Function
D ₀ -D ₈	Parallel Data Inputs
S-IN	Serial Data Input
SEL	Mode Select Input
CLK ₁ , CLK ₂	Clock Inputs
MR	Master Reset
Q ₀ -Q ₈	Data Outputs
V _{CCO}	V _{CC} to Output

TRUTH TABLE

SEL	MODE
L	LOAD
H	SHIFT

DC ELECTRICAL CHARACTERISTICS
 $V_{EE} = V_{EE} (\text{Min.}) \text{ to } V_{EE} (\text{Max.}); V_{CC} = V_{CC0} = \text{GND}$

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current	—	—	—	—	—	—	—	—	—	mA	—
		10E	120	145	120	145	120	145				
		100E	120	145	120	145	138	165				

AC ELECTRICAL CHARACTERISTICS
 $V_{EE} = V_{EE} (\text{Min.}) \text{ to } V_{EE} (\text{Max.}); V_{CC} = V_{CC0} = \text{GND}$

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f _{SHIFT}	Max. Shift Frequency	700	900	—	700	900	—	700	900	—	MHz	—
t _{PLH} t _{PHL}	Propagation Delay to Output CLK MR	600 600	800 800	1000 1000	600 600	800 800	1000 1000	600 600	800 800	1000 1000	ps	—
t _s	Set-up Time D SEL	50 300	-100 150	— —	50 300	-100 150	— —	50 300	-100 150	— —	ps	—
		300 75	100 -150	— —	300 75	100 -150	— —	300 75	100 -150	— —	ps	—
t _{RR}	Reset Recovery Time	900	700	—	900	700	—	900	700	—	ps	—
t _{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t _{skew}	Within-Device Skew	—	75	—	—	75	—	—	75	—	ps	1
t _r t _f	Rise/Fall Time 20% to 80%	300	525	800	300	525	800	300	525	800	ps	—

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E142JC	J28-1	Commercial
SY10E142JCTR	J28-1	Commercial
SY100E142JC	J28-1	Commercial
SY100E142JCTR	J28-1	Commercial

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

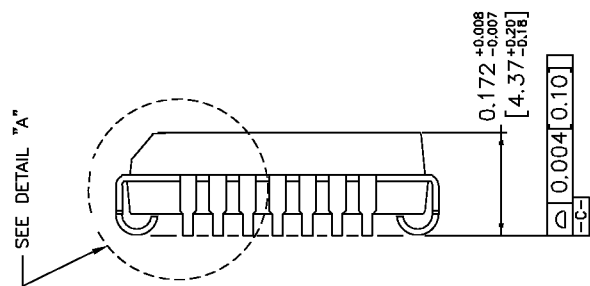
FILE/REV #: PD0008A03

PD/0008/ASCORP

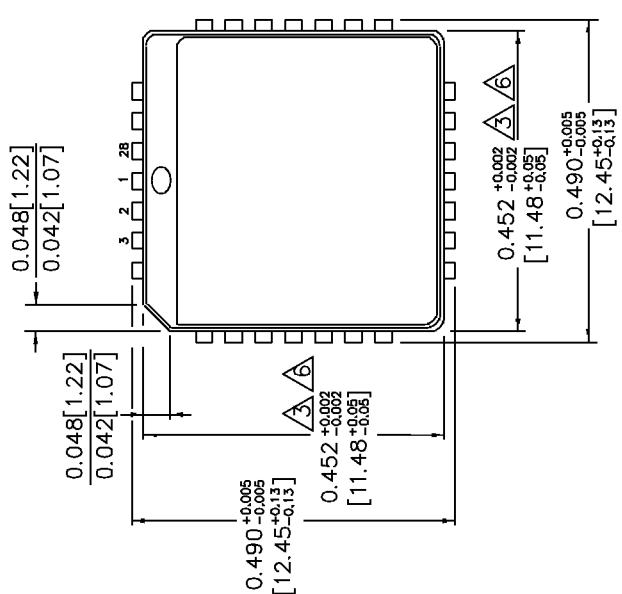
PAGE 1 OF 1

REV	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION A.0. FORMAT. ADD COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450[11.43] TO 0.443[11.25]. TYPOGRAPHICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD. REL. 12. REFERENCE AMKOR DWG. NO. 34853 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98

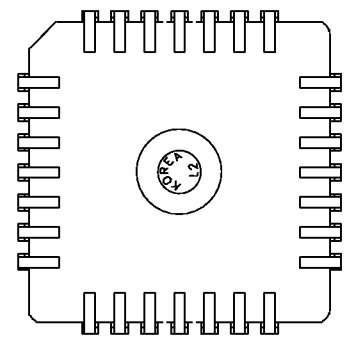
SIDE VIEW



TOP VIEW

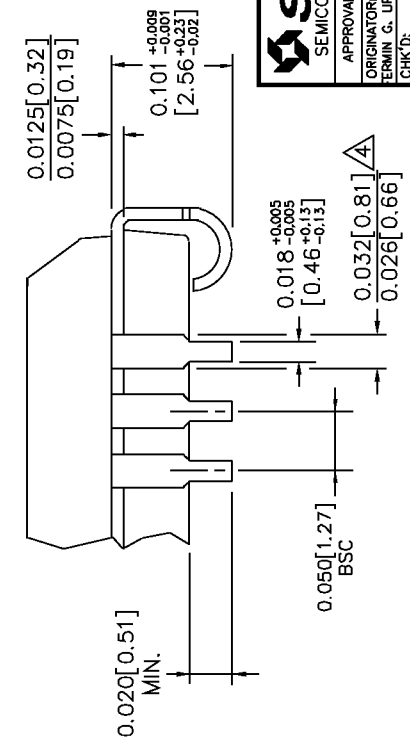


BOTTOM VIEW



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



DETAIL "A"

SYNERGY
SEMICONDUCTOR

3250 SCOTT BOULEVARD
SANTA CLARA, CA. 95054
TEL: 408-980-9191
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	28 LEAD PLCC
ORIGINATOR: ERMIN C. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	PACKAGE OUTLINE
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					

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SCALE: N/A
REVISION: 03