1Mx1 Dynamic RAM
CMOS, Monolithic

PRELIMINARY

The EDI411024C is a high performance, low power CMOS Dynamic RAM organized as 1Megabit x1. The use of triple-layer polysilicon process, combined with silicide technology and a single transistor dynamic storage cell, provide high circuit density with high performance.

The use of dynamic circuitry, including sense amplifiers, assures low power dissipation.

Multiplexed address inputs permit a low pin count for maximum system density.

In addition to the RAS\-only refresh mode, the hidden refresh mode and CAS\ before RAS\ refresh mode are available.

All inputs and outputs are TTL compatible and operate from a single 5 volt supply.

Military product compliant to MIL-STD-883, paragraph 1.2.1, is available.

Features

1Mx1 bit CMOS Dynamic
Random Access Memory

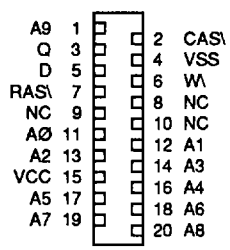
- Access Times 70, 80, 100, 120, and 150ns
- Low Operating Power Dissipation
- Low Standby Power
- All Inputs/Outputs TTL Compatible

Package Styles

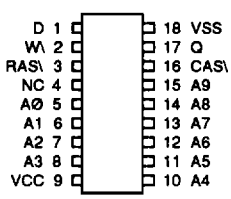
- 18 Pin DIP, No. 1
- 20(26) Lead Ceramic SOJ, No. 16
- 20 pin Ceramic ZIP, No.18
- 20 Lead Flatpack, No. 78

Single +5V (±10%) Supply Operation

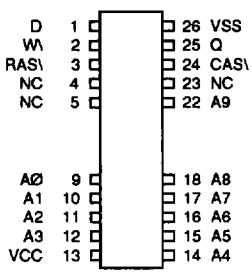
Pin Configurations and Block Diagram



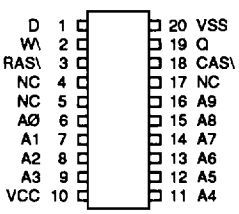
ZIP



DIP



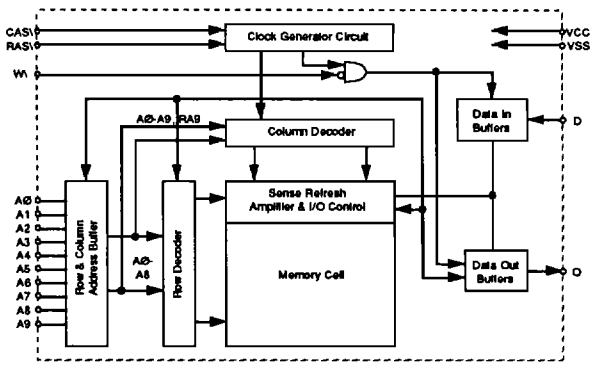
CSOJ



Flatpack

Pin Names

AØ-A9	Address Inputs
CAS\	Column Address Strobe
RAS\	Row Address Strobe
W\	Write Control Input
D	Data Input
Q	Data Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



Absolute Maximum Ratings*

Voltage on any pin relative to VSS .....-1.0V to 7.0V
Operating Temperature TA (Ambient)
Military..... -55°C to +125°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation..... 1 Watt
Output Current..... 50 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

(Note 1)

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.4	--	6.5	V
Input Low Voltage	VIL	-1.0	--	0.8	V

Notes: 1. All voltage values are with respect to VSS.

Electrical Characteristics

(TA = -55°C to +125°C; VCC = 5.0V ±10%) Note 2.

Parameter	Sym	Conditions	ns	Min	Typ	Max	Units
Average Supply Current from VCC	ICC1	RAS\, CAS\ Cycling	70			80	mA
Operating (Notes 3, 4)		TRC = TWC = Min, Output Open	80			70	mA
			100			60	mA
			120			60	mA
			150			55	mA
Supply Current from VCC	ICC2	RAS\ = CAS\ = VIH, Output Open				2	mA
Standby		RAS\ = CAS\ ≥ VCC-0.5, Output Open				0.5	mA
Average Supply Current from VCC	ICC3	RAS\ Cycling, CAS\ = VIH	70			80	mA
Refreshing (Note 3)		TRC = Min, Output Open	80			70	mA
			100			60	mA
			120			60	mA
			150			55	mA
Average Supply Current from VCC	ICC4	RAS\ = VIL, CAS\ = Cycling	70			70	mA
Fast Page Mode (Notes 3, 4)		TPC = Min, Output Open	80			60	mA
			100			50	mA
			120			45	mA
			150			35	mA
Average Supply Current from VCC	ICC6	CAS\ before RAS\ Refresh Cycling	70			80	mA
CAS\ before RAS\ Refresh Mode (Note 3)		TRC = Min Output Open	80			70	mA
			100			60	mA
			120			60	mA
			150			55	mA
Input Current	II	0V ≤ VIN ≤ VCC		-10		10	µA
		VCC = 6.5V, All Other Pins = 0V					
Off-State Output Current	IOZ	Q Floating 0V≤ V OUT ≤ 5.5V		-10		10	µA
Output High Voltage	VOH	IOH = -5mA		2.4	—	VCC	V
Output Low Voltage	VOL	IOL= 4.2mA		0	—	0.4	V

Notes: 2. Current flowing into an IC is positive, out is negative.
3. ICC1(av), ICC3(av), ICC4(av), and ICC6 are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. ICC1(av), and ICC4(av) are dependent on output loading. Specified values are obtained with the output open.

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Test Conditions	Min	Typ	Max	Unit
Address Input Capacitance (Note 5)	CA	VI = VSS			5	pF
Input Capacitance (D)	CD	f = 1MHz			5	pF
Input Capacitance (CAS\,W\, RAS\)	CC, CW, CR	Vi = 25mVrms			7	pF
Output Capacitance (Q)	CQ	VO = VSS, f = 1MHz, Vi = 25mVrms			7	pF

Notes: 5. CI (av) of ZIP is 6pF.

Input Conditions for Each Mode

The EDI411024C provides, in addition to normal Read, Write, and Read-modify-Write operations, a number of other functions, e.g. Fast Page Mode, RAS\-only Refresh, and Delayed Write. The input conditions for each are shown below.

ACT = Active
NAC= Non-active
DNC= Don't care

VLD = Valid
APD = Applied
OPN = Open

Operation	Inputs						Output	Refresh
	RAS\	CAS\	W\	D	Row Address	Column Address	Q	
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	Yes*
Early Write	ACT	ACT	ACT	VLD	APD	APD	OPN	Yes*
Read-Modify-Write	ACT	ACT	ACT	VLD	APD	APD	VLD	Yes*
RAS\-only Refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	Yes
Hidden Refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	Yes
CAS\ before RAS\ Refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	Yes
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	No

* Fast Page Mode Identical.

Switching Charateristics

(TA = -55°C to +125°C; VCC = 5.0V ±10%) Note 6.

		70ns		80ns		100ns		120ns		150ns			
Parameter	Sym	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Access Time from CAS\	TCAC		20		20		25		30		40	ns	7, 8
Access Time From RAS\	TRAC		70		80		100		120		150	ns	7, 9
Column Address Access Time	TCAA		35		40		50		55		70	ns	7, 10
Access Time frorm CAS\ Precharge	TCPA		40		45		55		60		75	ns	7, 11
Output Low Impedance Time from CAS\ low	TCLZ	5		5		5		5		5		ns	7
Output Disable Time after CAS\ High	TOFF	0	20	0	20	0	25	0	30	0	35	ns	12

Notes: 6. An initial pause of 500µs is required after power-up, followed by any 8 RAS\ or RAS\-CAS\ cycles before proper device operation is achieved. Note that RAS\ may be cycled during the initial pause. Any 8 RAS\ or RAS\-CAS\ cycles are required after prolonged periods of RAS\ inactivity before proper device operation.

7. Measured with a load circuit equivalent to 2TTL loads and 100pF.
8. Assume that TRCD(max) ≤ TRAD and TRAD(max) ≥ TRAD.
9. Assume that TRCD ≤ TRCD(max) and TRAD ≤ TRAD(max).
10. Assume that TRCD - TRAD ≤ TCAA(max) and TRCD ≥ TRCD(max).
11. Assume that TCP ≤ TCP(max) and TASC ≥ TASC(max).
12. TOFF(max) defines the time at which the output achieves the high impedance state (IOUT ≤ |±10µA|) and is not reference to VOH(min) or VOL(max).

Timing Requirements

Read, Write, Read-Modify-Write, Refresh, and Fast Page Mode Cycles

(TA = -55°C to +125°C; VCC = 5.0V±10%) Notes 13, 14

		70ns		80ns		100ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Refresh Cycle	TREF		8		8		8	ms	
RAS\ Precharge Time	TRP	60		70		80		ns	
RAS\ to CAS\ Delay Time	TRCD	20	50	25	60	25	75	ns	15
Delay CAS\ High to RAS\ Low	TCRP	10		10		10		ns	16
CAS\ Precharge Time (Non Page Mode)	TCPN	30		35		35		ns	17
Column Address Delay from RAS\ Low	TRAD	15	35	20	40	20	50	ns	18
Row Address Set Up Time	TASR	0		0		0		ns	
Column Address Set Up Time	TASC	0	10	0	15	0	20	ns	19
Row Address Hold Time	TRAH	10		15		15		ns	
Column Address Hold Time	TCAH	15		20		20		ns	
Transition Time	TT	3	50	3	50	3	50	ns	20

Notes: 13. The timing requirements are assumed TT = 5ns.
14. VIH(min) and VIL (max) are reference levels for measuring timing of input signals.
15. TRCD(max) is specified as a reference point only. If TRCD is less than TRCD(max), access time is TRAC. If TRCD is greater than TRCD(max), access time is defined as TCAC and TCAA as shown in notes 7, 9.
16. TCRP requirement is applicable for all RAS\-CAS\ cycles.
17. TCPN(min) is specified as TCPN(min) =TCRD(min) +TCRP(min) except for TCP of fast page mode cycle.
18. TRAD(max) is specified as a reference point only. If TRAD ≥ TRAD(max), access time is assumed byTCAA for read cycle.
19. TASC(max) is specified as a reference point only of address acess time.
20. TT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

(TA = -55°C to +125°C; VCC = 5.0V±10%)

		70ns		80ns		100ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read Cycle Time	TRC	140		160		190		ns	
RAS\ Low Pulse Width	TRAS	70	10,000	80	10,000	100	10,000	ns	
CAS\ Low Pulse Width	TCAS	20	10,000	20	10,000	25	10,000	ns	
CAS\ Hold Time after RAS\ Low	TCSH	70		80		100		ns	
RAS\ Hold Time after CAS\ Low	TRSH	20		20		25		ns	
Read Set Up Time before CAS\ Low	TRCS	0		0		0		ns	
Read Hold Time after CAS\ High	TRCH	0		0		0		ns	21
Read Hold Time after RAS\ High	TRRH	10		10		10		ns	21
Column Address to RAS\ Setup	TRAL	35		40		50		ns	
Precharge to CAS\ Active	TRPC	0		0		0		ns	

Notes: 21. Either TRCH or TRRH must be satisfied for a read cycle.

Timing Requirements
Read, Write, Read-Modify-Write, Refresh, and Fast Page Mode Cycles

(TA = -55°C to +125°C; VCC = 5.0V±10%) Notes 13, 14

		120ns		150ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Refresh Cycle	TREF		8		8	ms	
RAS\ Precharge Time	TRP	90		100		ns	
RAS\ to CAS\ Delay Time	TRCD	25	95	30	115	ns	15
Delay CAS\ High to RAS\ Low	TCRP	10		10		ns	16
CAS\ Precharge Time (Non Page Mode)	TCPN	35		35		ns	17
Column Address Delay from RAS\ Low	TRAD	20	65	25	80	ns	18
Row Address Set Up Time	TASR	0		0		ns	
Column Address Set Up Time	TASC	0	25	0	30	ns	19
Row Address Hold Time	TRAH	15		20		ns	
Column Address Hold Time	TCAH	20		25		ns	
Transition Time	TT	3	50	3	50	ns	20

Notes: 13. The timing requirements are assumed TT = 5ns.
14. VIH(min) and VIL (max) are reference levels for measuring timing of input signals.
15. TRCD(max) is specified as a reference point only. If TRCD is less than TRCD(max), access time is TRAC. If TRCD is greater than TRCD(max), access time is defined as TCAC and TCAA as shown in notes 7, 9.
16. TCRP requirement is applicable for all RAS\-CAS\ cycles.
17. TCPN(min) is specified as TCPN(min) =TCRD(min) +TCRP(min) except for TCP of fast page mode cycle.
18. TRAD(max) is specified as a reference point only. If TRAD ≥ TRAD(max), access time is assumed byTCAA for read cycle.
19. TASC(max) is specified as a reference point only of address acess time.
20. TT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

(TA = -55°C to +125°C; VCC = 5.0V±10%)

		120ns		150ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read Cycle Time	TRC	220		260		ns	
RAS\ Low Pulse Width	TRAS	120	10,000	150	10,000	ns	
CAS\ Low Pulse Width	TCAS	30	10,000	40	10,000	ns	
CAS\ Hold Time after RAS\ Low	TCSH	100		100		ns	
RAS\ Hold Time after CAS\ Low	TRSH	30		40		ns	
Read Set Up Time before CAS\ Low	TRCS	0		0		ns	
Read Hold Time after CAS\ High	TRCH	0		0		ns	21
Read Hold Time after RAS\ High	TRRH	10		10		ns	21
Column Address to RAS\ Setup	TRAL	55		70		ns	
Precharge to CAS\ Active	TRPC	0		0		ns	

Notes: 21. Either TRCH or TRRH must be satisfied for a read cycle.

Write Cycle

(TA = -55°C to +125°C; VCC = 5.0V±10%)

		70ns		80ns		100ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write Cycle Time	TWC	140		160		190		ns	
RAS\ Low Pulse Width	TRAS	70	10,000	80	10,000	100	10,000	ns	
CAS\ Low Pulse Width	TCAS	20	10,000	20	10,000	25	10,000	ns	
CAS\ Hold Time after RAS\ Low	TCSH	70		80		100		ns	
RAS\ Hold Time after CAS\ Low	TRSH	20		20		25		ns	
Write Setup Time before CAS\ Low	TWCS	0		0		0		ns	24
Write Hold Time after CAS\ Low	TWCH	15		15		20		ns	
Write Pulse Width	TWP	15		15		20		ns	
Data Set up Time	TDS	0		0		0		ns	
Data Hold Time after CAS\ Low	TDH	15		15		20		ns	

Read-Write and Read-Modify-Write Cycles

(TA = -55°C to +125°C; VCC = 5.0V±10%)

		70ns		80ns		100ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-Write CycleTime	TRWC	165		185		220		ns	22
Read-Modify-Write CycleTime	TRMWC	165		185		220		ns	23
RAS\ Low Pulse Width	TRASRW	95	10,000	105	10,000	130	10,000	ns	
CAS\ Low Pulse Width	TCASRW	45	10,000	45	10,000	55	10,000	ns	
CAS\ Hold Time after RAS\ Low	TCSHRW	95		105		130		ns	
RAS\ Hold Time after CAS\ Low	TRSHRW	45		45		55		ns	
Read Setup time before CAS\ Low	TRCS	0		0		0		ns	
CAS\ Low to W\ Low Delay	TCWD	20		20		25		ns	24
RAS\ Low to W\ Low Delay	TRWD	70		80		100		ns	24
CAS\ Hold after W\ Low	TCWL	20		20		25		ns	
RAS\ Hold after W\ Low	TRWL	20		20		25		ns	
Write Pulse Width	TWP	15		15		20		ns	
Data Set up Time	TDS	0		0		0		ns	
Data Hold Time after W\ Low	TDH	15		15		20		ns	
Address to W\ Low Delay	TAWD	35		40		50		ns	24

Notes: 22. TRWC is specified as TRWC(min) = TRCD(max) + TCWD (min) +TRWL(min) + TRP(min) +3TT.

23. TRMWC is specified as TRMWC(min) = TRAC(max) +TRWL(min) +TRP(min) +3TT.

24. TWCS, TRWD, TCWD, and TAWD do not define the limits of operation, but are included as electrical characteristics only. When TWCS ≥ TWCS(min), an early write cycle is performed, and the data output keeps the high-impedance state. When TRWD ≥ TRWD(min), TCWD ≥ TCWD(min) and TAWD ≥ TAWD(min), a read write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above conditions is satisfied, the condition of Q (at the access time and until CAS\ goes back to VIH) is indeterminate.

Write Cycle

(TA = -55°C to +125°C; VCC = 5.0V±10%)

		120ns		150ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write Cycle Time	TWC	220		260		ns	
RAS\ Low Pulse Width	TRAS	120	10,000	150	10,000	ns	
CAS\ Low Pulse Width	TCAS	30	10,000	40	10,000	ns	
CAS\ Hold Time after RAS\ Low	TCSH	120		150		ns	
RAS\ Hold Time after CAS\ Low	TRSH	30		40		ns	
Write Setup Time before CAS\ Low	TWCS	0		0		ns	24
Write Hold Time after CAS\ Low	TWCH	25		30		ns	
Write Pulse Width	TWP	20		25		ns	
Data Set up Time	TDS	0		0		ns	
Data Hold Time after CAS\ Low	TDH	25		30		ns	

Read-Write and Read-Modify-Write Cycles

(TA = -55°C to +125°C; VCC = 5.0V±10%)

		120ns		150ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-Write CycleTime	TRWC	255		305		ns	22
Read-Modify-Write CycleTime	TRMWC	255		305		ns	23
RAS\ Low Pulse Width	TRASRW	150	10,000	190	10,000	ns	
CAS\ Low Pulse Width	TCASRW	60	10,000	80	10,000	ns	
CAS\ Hold Time after RAS\ Low	TCSHRW	150		190		ns	
RAS\ Hold Time after CAS\ Low	TRSHRW	60		80		ns	
Read Setup time before CAS\ Low	TRCS	0		0		ns	
CAS\ Low to W\ Low Delay	TCWD	30		40		ns	24
RAS\ Low to W\ Low Delay	TRWD	120		150		ns	24
CAS\ Hold after W\ Low	TCWL	30		40		ns	
RAS\ Hold after W\ Low	TRWL	30		40		ns	
Write Pulse Width	TWP	20		25		ns	
Data Set up Time	TDS	0		0		ns	
Data Hold Time after W\ Low	TDH	20		25		ns	
Address to W\ Low Delay	TAWD	55		70		ns	24

Notes: 22. TRWC is specified as TRWC(min) = TRCD(max) + TCWD (min) +TRWL(min) + TRP(min) +3TT.

23. TRMWC is specified as TRMWC(min) = TRAC(max) +TRWL(min) +TRP(min) +3TT.

24. TWCS, TRWD, TCWD, and TAWD do not define the limits of operation, but are included as electrical characteristics only. When TWCS ≥ TWCS(min), an early write cycle is performed, and the data output keeps the high-impedance state. When TRWD≥ TRWD(min), TCWD ≥ TCWD(min) and TAWD ≥ TAWD(min), a read write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above conditions is satisfied, the condition of Q (at the access time and until CAS\ goes back to VIH) is indeterminate.

Fast Page Mode Cycle
Read, Early Write, Read-Write, Read-Modify-Write Cycles

(TA = -55°C to +125°C; VCC = 5.0V±10%)

		70ns		80ns		100ns		120ns		150na		
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Fast Page Mode Cycle Time	TPC	45		50		60		65		80		ns
Fast Page Mode for R/W, R/M/W Cycle Time	TRWPC	70		75		90		100		125		ns
RAS\ Low Pulse Width for Read, Write Cycle	TRAS	115	100,000	130	100,000	160	100,000	185	100,000	230	100,000	ns
CAS\ Low Pulse Width for Read Cycle	TCAS	20	10,000	20	10,000	25	10,000	30	10,000	40	10,000	ns
CAS\ Pulse Width (Page Mode)	TCP	10		10		10		10		10		ns
RAS\ Hold Time after CAS\ Low	TRSH	20		20		25		30		40		ns

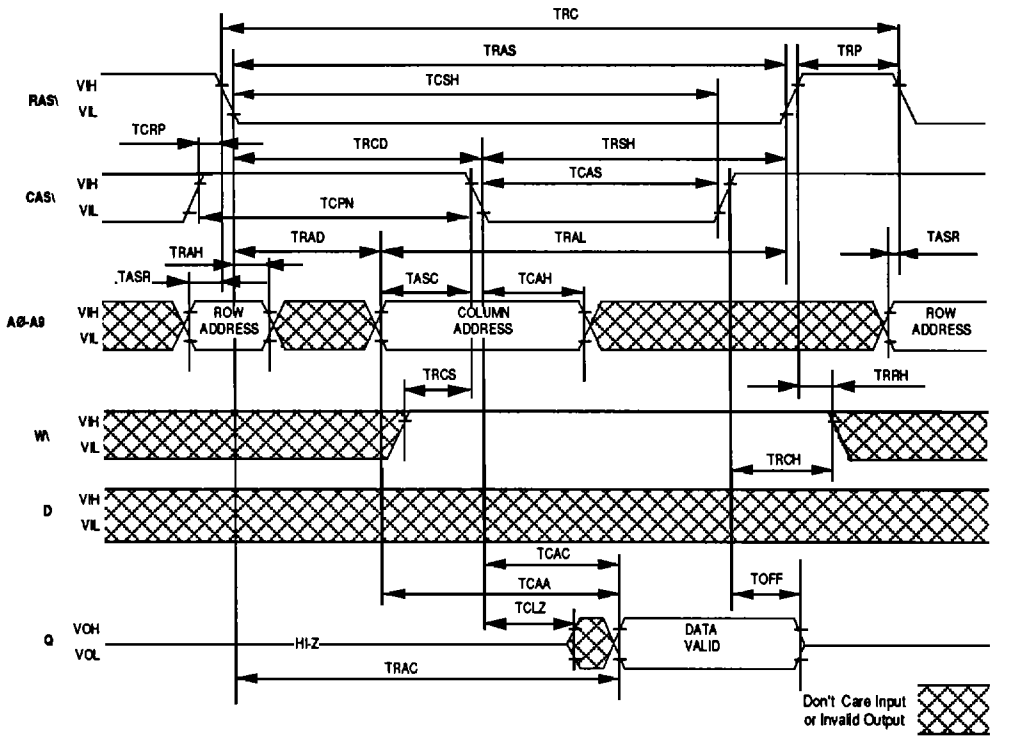
CAS\ before RAS\ Refresh Cycle

(TA = -55°C to +125°C; VCC = 5.0V±10%)

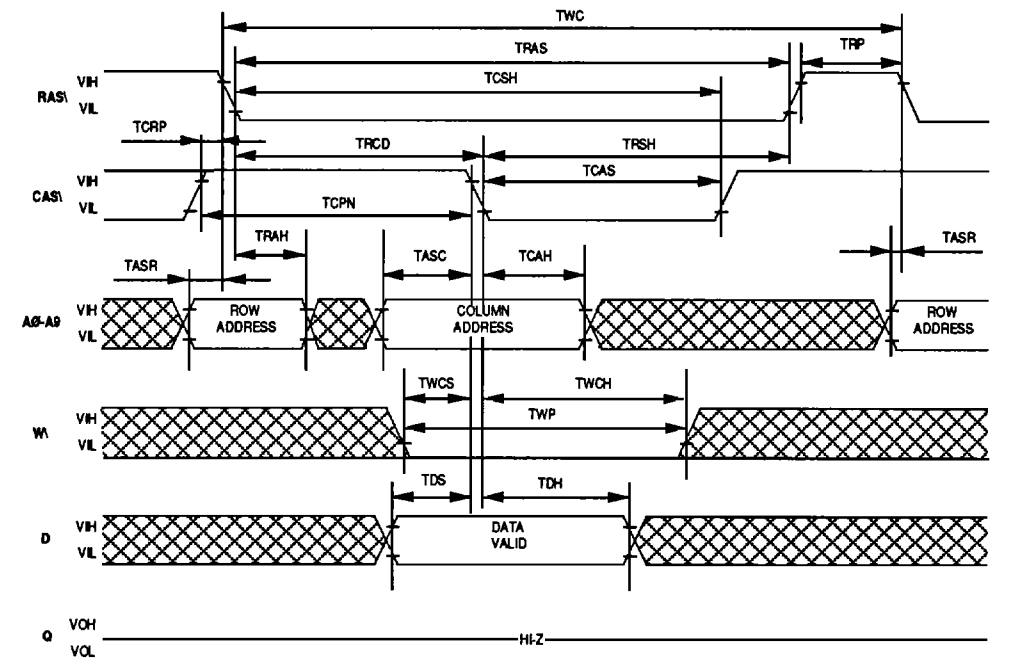
		70ns		80ns		100ns		120ns		150ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
CAS\ Setup for CAS\ before RAS\ Refresh	TCSR	10		10		10		10		10		ns	25
CAS\ Hold for CAS\ before RAS\ Refresh	TCHR	15		15		20		25		30		ns	25
Precharge to CAS\ Active	TRPC	0		0		0		0		0		ns	25

Note: 25. Eight or more CAS\ before RAS\ cycles are necessary for proper operation of CAS\ before RAS\ refresh mode.

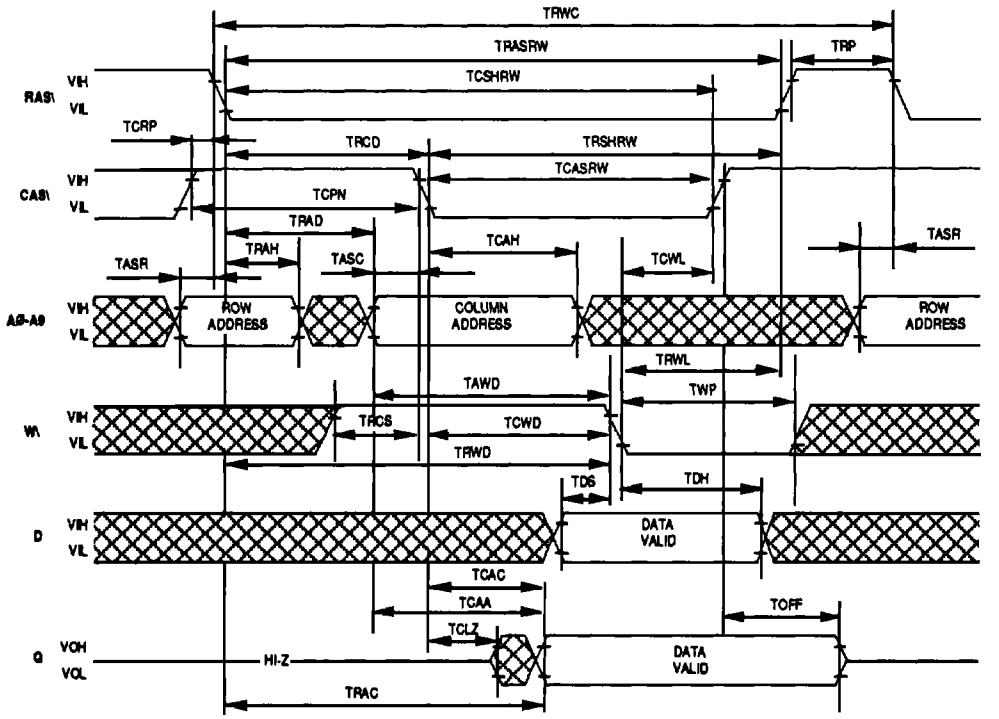
Read Cycle



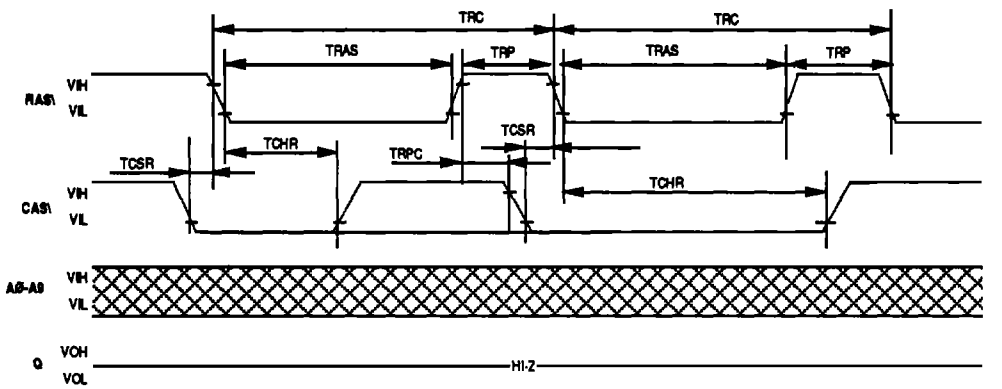
Write Cycle, Early Write



Read-Write, Read-Modify-Write Cycle

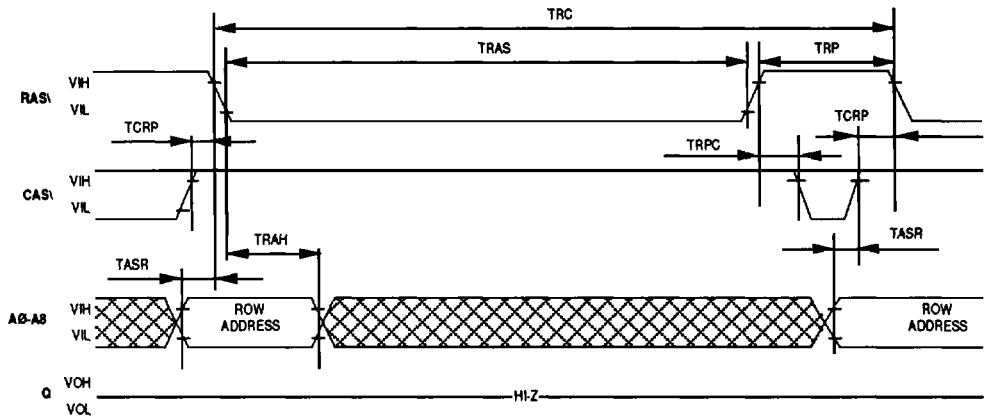


CAS\ before RAS\ Refresh Cycle *Note 26*



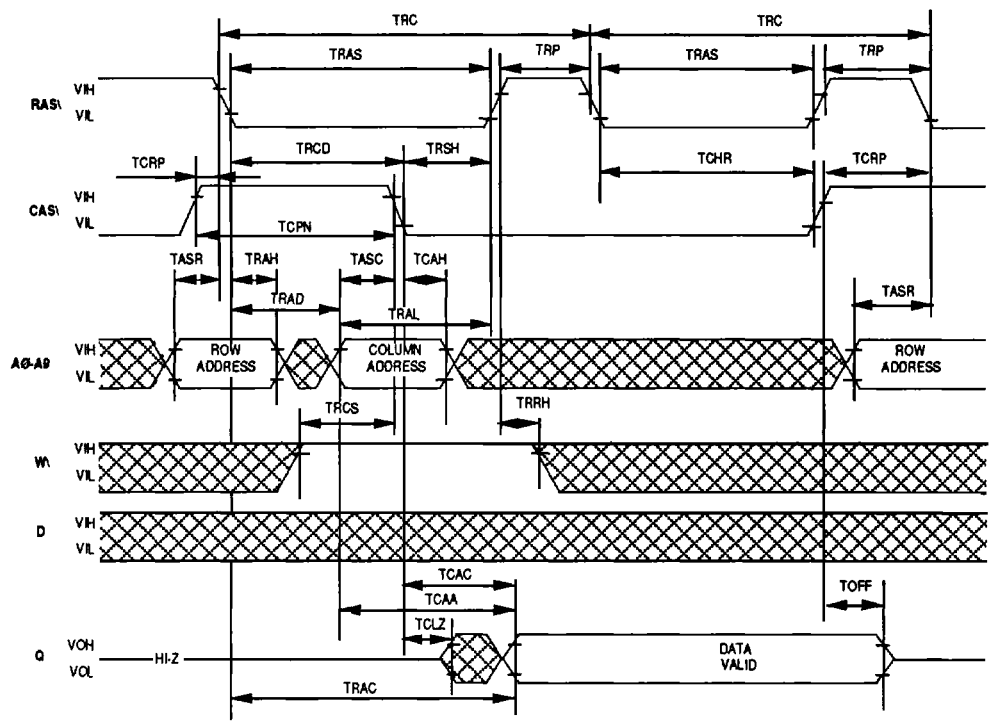
Note: 26. W\, D = Don't care.

RAS\-only Refresh Cycle *Note 27*

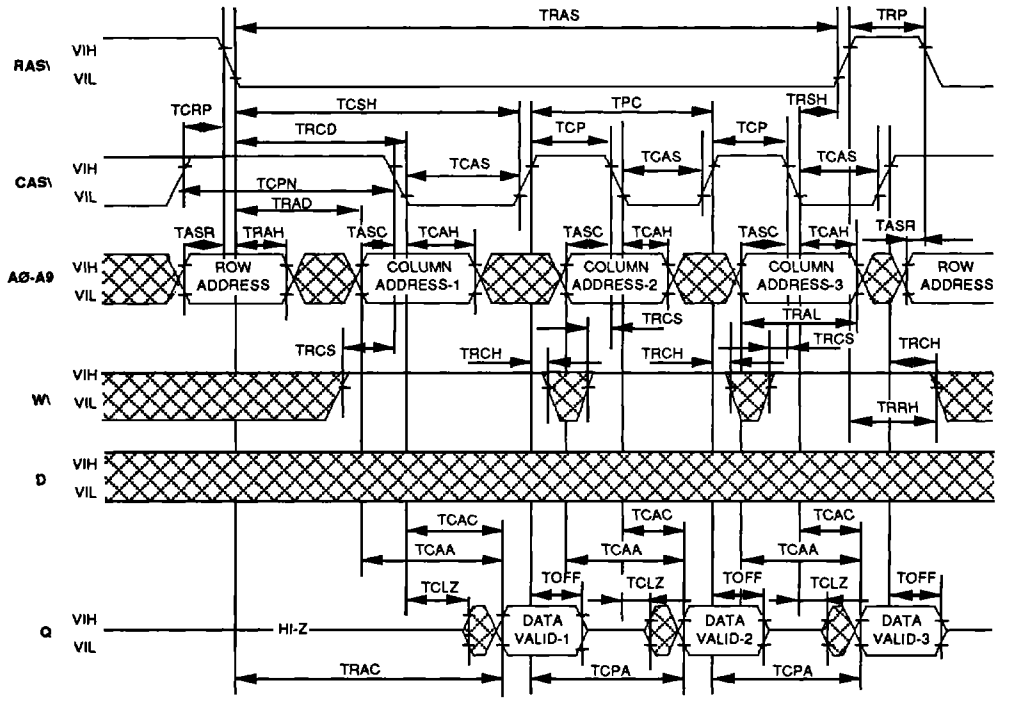


Note: 27. W\, D = Don't care; A9 = VIH or VIL.

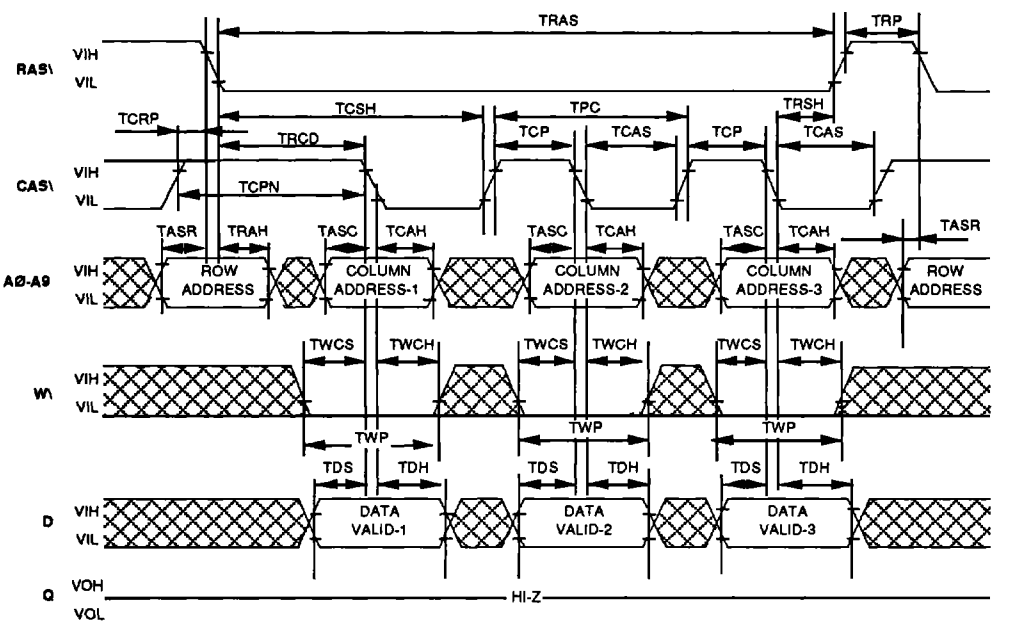
Hidden Refresh Cycle



Fast-Page-Mode, Read Cycle



Fast-Page-Mode, Early Write Cycle



Fast-Page-Mode Read-Write, Read-Modify-Write Cycle