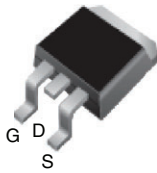


Power MOSFET

D²PAK (TO-263)


N-Channel MOSFET

FEATURES

- Advanced process technology
- Surface-mount
- 175 °C operating temperature
- Fast switching
- Fully avalanche rated
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available
HALOGEN FREE
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

PRODUCT SUMMARY	
V _{DS} (V)	60
R _{DS(on)} (Ω)	V _{GS} = 5 V 0.05
Q _g max. (nC)	35
Q _{gs} (nC)	7.1
Q _{gd} (nC)	25
Configuration	Single

DESCRIPTION

Third generation power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that power MOSFETs are known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²PAK (TO-263) is a surface-mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface-mount application.

ORDERING INFORMATION	
Package	D ² PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHLZ34S-GE3
Lead (Pb)-free	IRLZ34SPbF

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-source voltage	V _{DS}		60	V
Gate-source voltage	V _{GS}		± 10	
Continuous drain current	V _{GS} at 5 V	T _C = 25 °C	30	A
		T _C = 100 °C	21	
Pulsed drain current ^a	I _{DM}		110	
Linear derating factor			0.59	W/°C
Single pulse avalanche energy ^b	E _{AS}		128	mJ
Maximum power dissipation	T _C = 25 °C		88	W
Maximum power dissipation (PCB mount) ^e	T _A = 25 °C		3.7	
Peak diode recovery dv/dt ^c	dv/dt		4.5	V/ns
Operating junction and storage temperature range	T _J , T _{stg}		-55 to +175	°C
Soldering recommendations (peak temperature) ^d	For 10 s		300	

Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- V_{DD} = 25 V, starting T_J = 25 °C, L = 285 μH, R_g = 25 Ω, I_{AS} = 30 A (see fig. 12)
- I_{SD} ≤ 30 A, di/dt ≤ 200 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material)



THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum junction-to-ambient (PCB mount) ^a	R _{thJA}	-	-	40	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	-	1.7	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		60	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.07	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.0	-	2.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 10 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 48 V, V _{GS} = 0 V, T _J = 150 °C		-	-	250	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 5 V	I _D = 18 A ^b	-	-	0.05	Ω
		V _{GS} = 4 V	I _D = 15 A ^b	-	-	0.07	
Forward transconductance	g _{fs}	V _{DS} = 25 V, I _D = 18 A		12	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1600	-	pF
Output capacitance	C _{oss}			-	660	-	
Reverse transfer capacitance	C _{rss}			-	170	-	
Total gate charge	Q _g	V _{GS} = 5 V	I _D = 30 A, V _{DS} = 48 V, see fig. 6 and 13 ^b	-	-	35	nC
Gate-source charge	Q _{gs}			-	-	7.1	
Gate-drain charge	Q _{gd}			-	-	25	
Turn-on delay time	t _{d(on)}	V _{DD} = 30 V, I _D = 30 A, R _g = 6 Ω, R _D = 1 Ω, see fig. 10 ^b		-	14	-	ns
Rise time	t _r			-	170	-	
Turn-off delay time	t _{d(off)}			-	30	-	
Fall time	t _f			-	56	-	
Internal source inductance	L _S	Between lead, and center of die contact		-	7.5	-	nH
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	30	A
Pulsed diode forward current ^a	I _{SM}			-	-	110	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 30 A, V _{GS} = 0 V ^b		-	-	1.6	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 30 A, di/dt = 100 A/μs ^b		-	120	180	ns
Body diode reverse recovery charge	Q _{rr}			-	700	1300	nC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

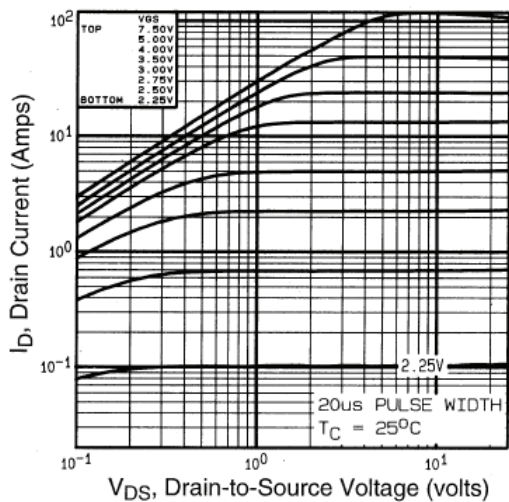


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

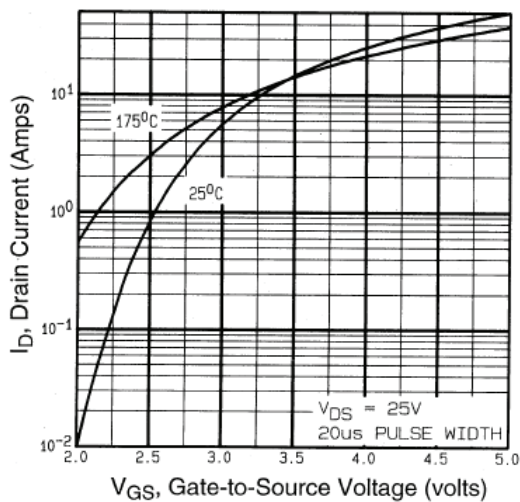


Fig. 3 - Typical Transfer Characteristics

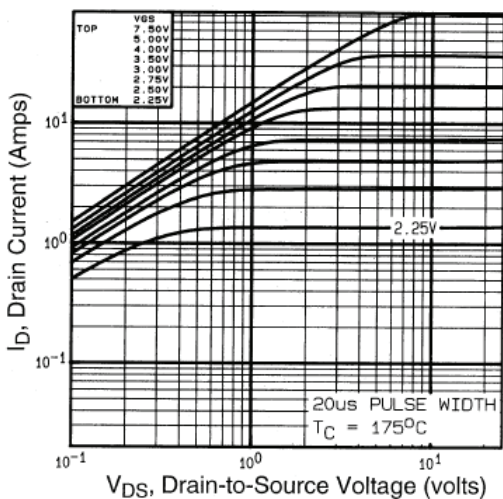


Fig. 2 - Typical Output Characteristics, $T_C = 175\text{ }^\circ\text{C}$

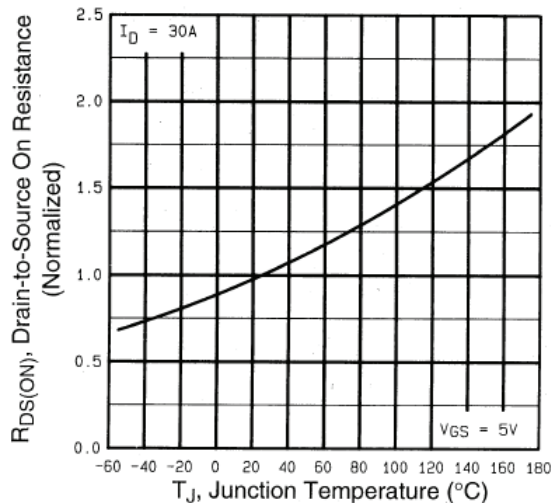


Fig. 4 - Normalized On-Resistance vs. Temperature

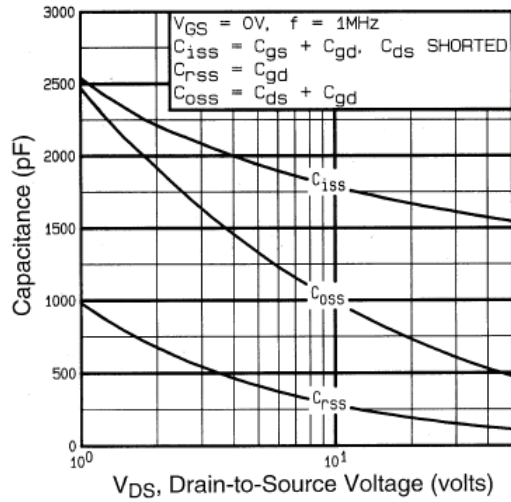


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

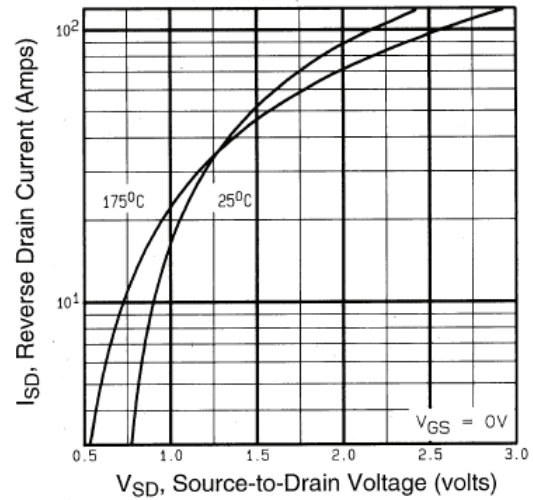


Fig. 7 - Typical Source-Drain Diode Forward Voltage

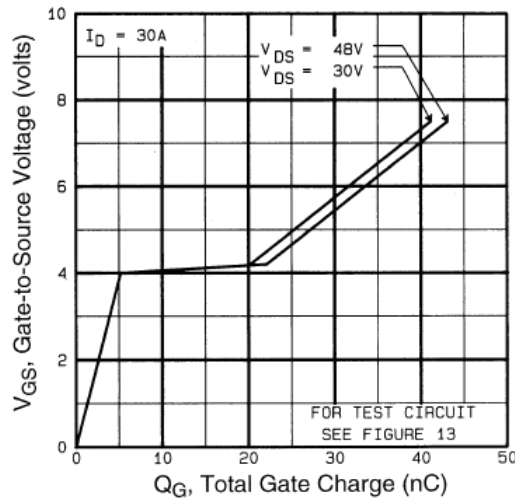


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

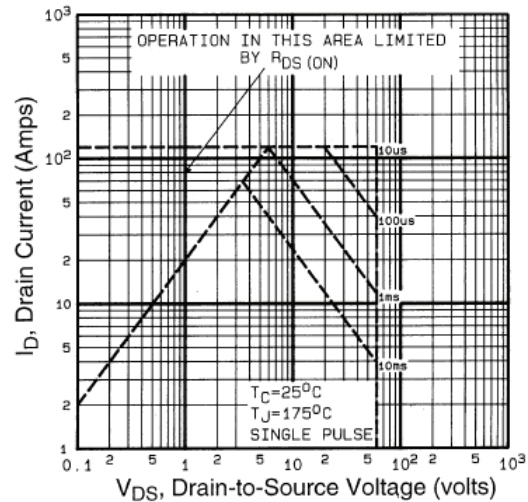


Fig. 8 - Maximum Safe Operating Area

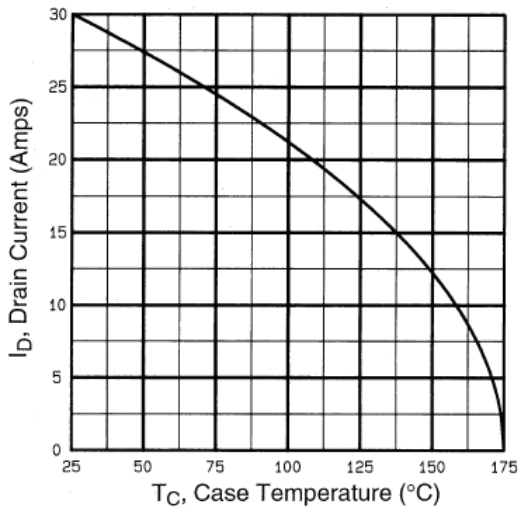


Fig. 9 - Maximum Drain Current vs. Case Temperature

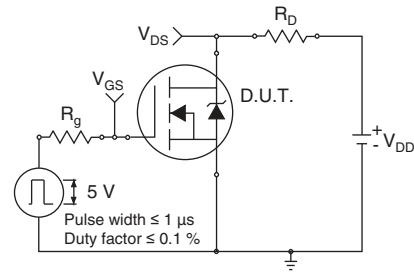


Fig. 10a - Switching Time Test Circuit

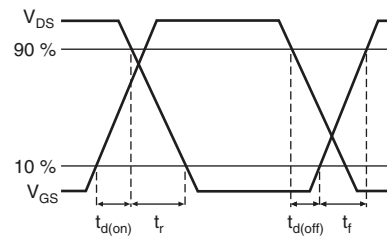


Fig. 10b - Switching Time Waveforms

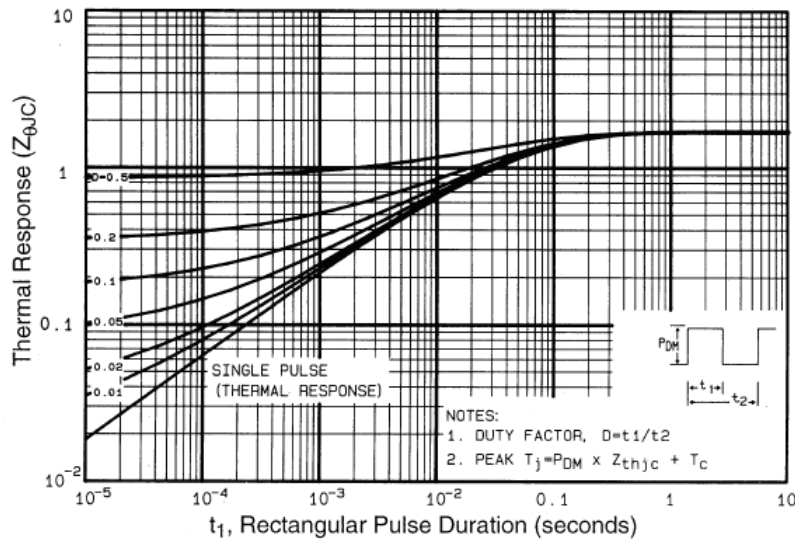


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

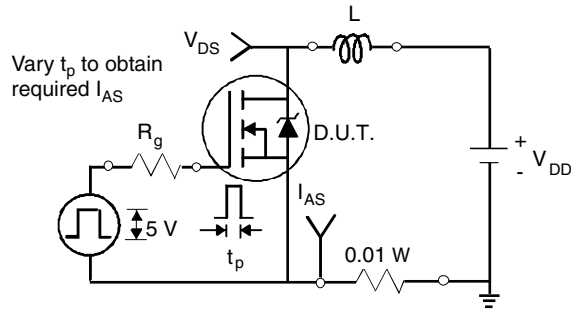


Fig. 12a - Unclamped Inductive Test Circuit

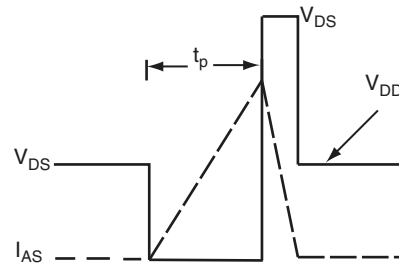


Fig. 12b - Unclamped Inductive Waveforms

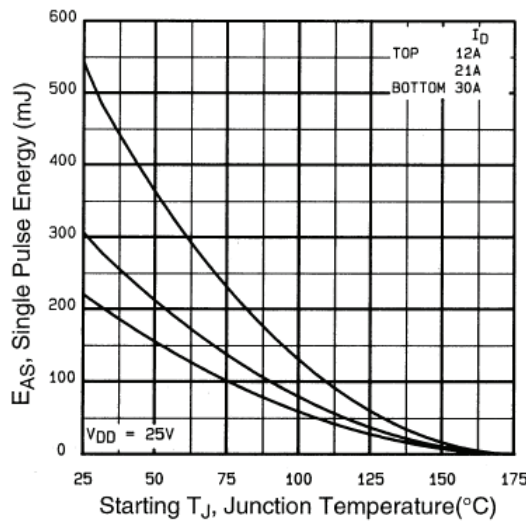


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

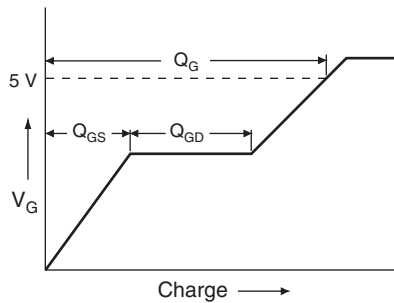


Fig. 13a - Basic Gate Charge Waveform

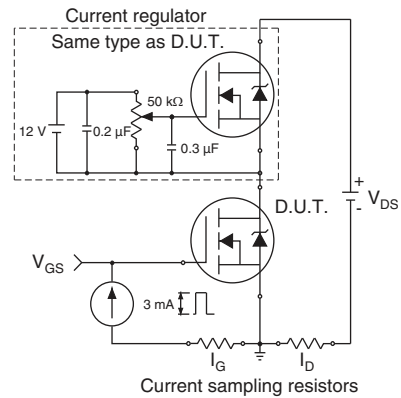
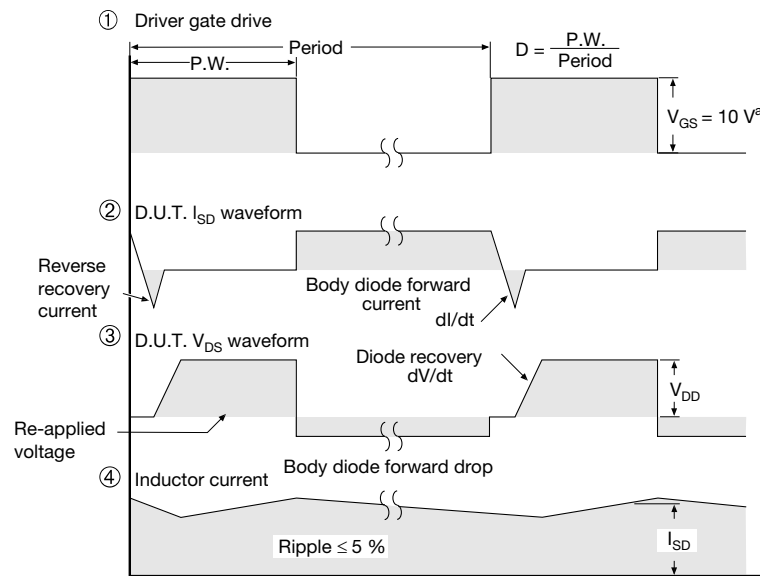
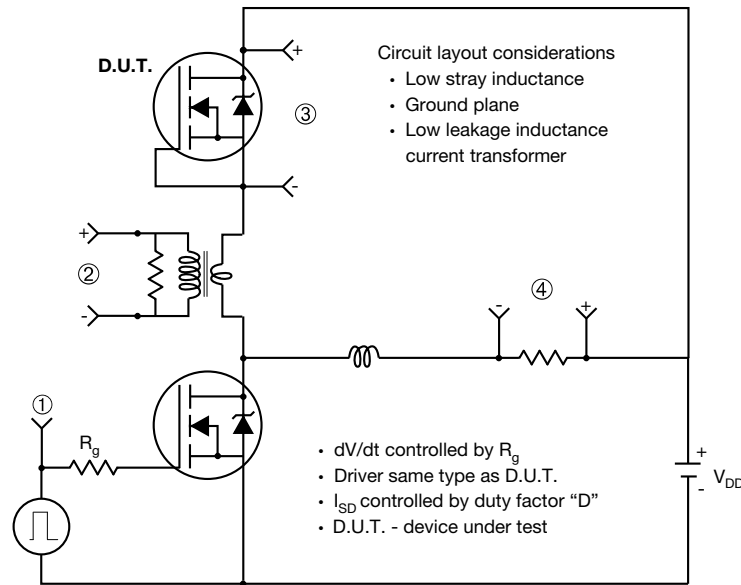


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

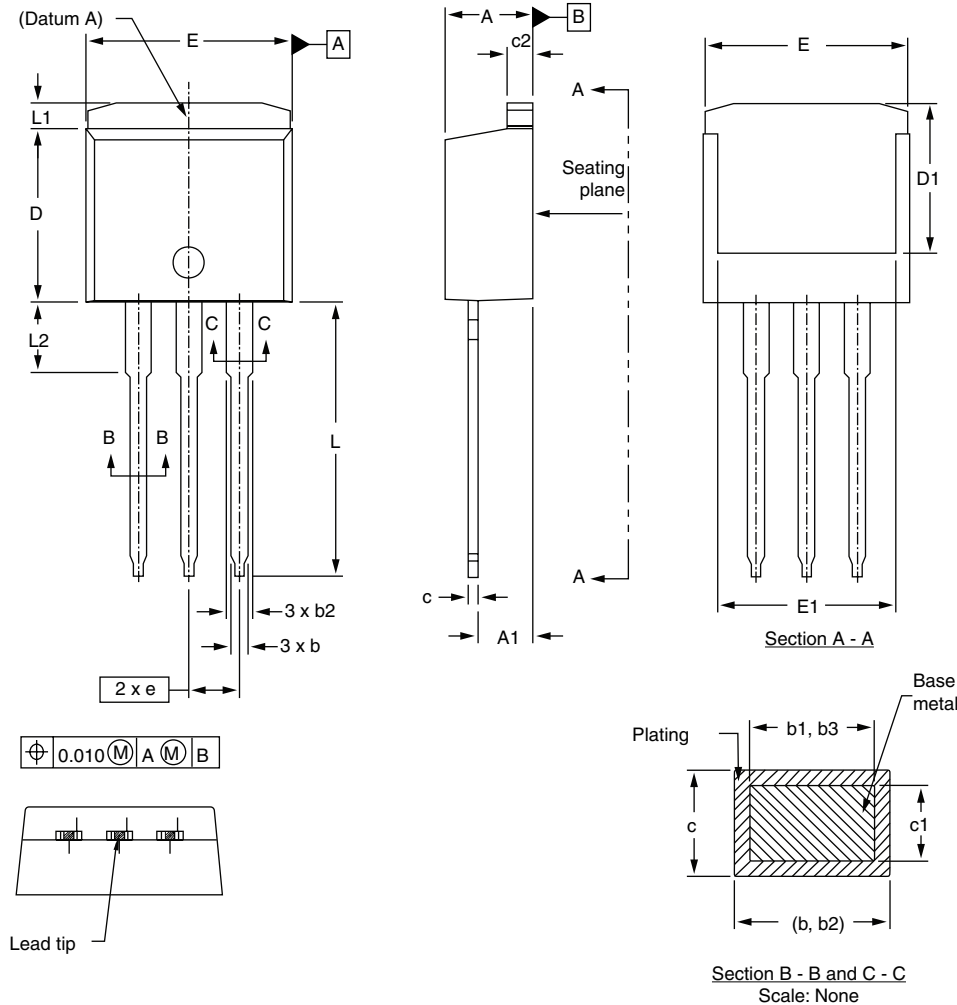


Note
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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I²PAK (TO-262) (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

ECN: S-82442-Rev. A, 27-Oct-08
DWG: 5977

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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