Signetics

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Status	Product Specification
FAST Products	

FAST 74F164
Shift Register

8-Bit Serial-In Parallel-Out Shift Register

FEATURES

- **Gated serial data inputs**
- **Typical shift frequency of 100MHz**
- **Asynchronous Master Reset**
- **Fully buffered clock and data inputs**
- **Fully synchronous data transfers**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F164	100MHz	33mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F164N
14-Pin Plastic SO	N74F164D

DESCRIPTION

The 74F164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered through one of two inputs (D_{sa}, D_{sb}); either input can be used as an active High enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied High.

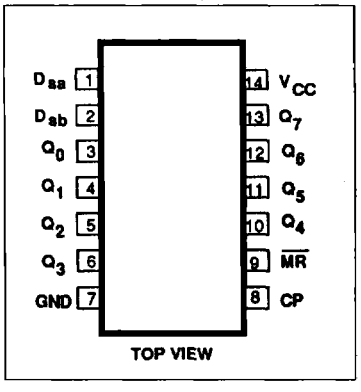
Data shifts one place to the right on each Low-to-High transition of the Clock (CP) input, and enters into Q_0 the logical AND of the the two data inputs (D_{sa}, D_{sb}) that existed one setup time before the rising clock edge. A Low level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{sa}, D_{sb}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

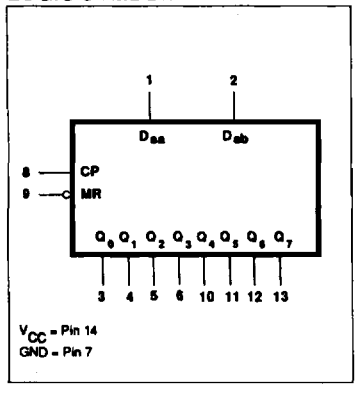
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

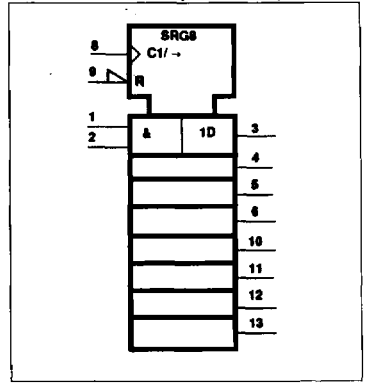


TOP VIEW

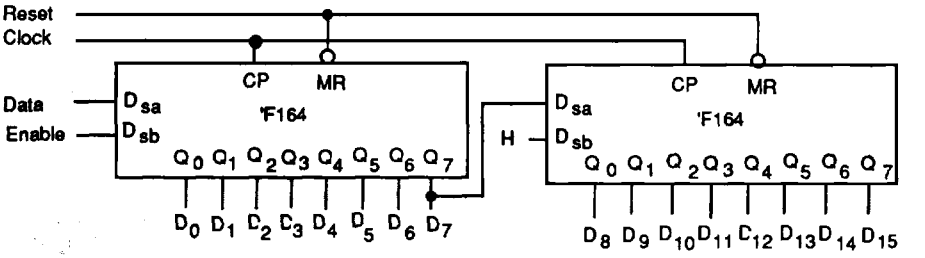
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



APPLICATION



NOTE: The 'F164 can be cascaded to form synchronous shift registers of longer length. Here, two 'F164 are combined to form a 16 bit shift register.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.0 5.0	5.0 7.0	8.0 10.0	2.5 5.0	9.0 11.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	5.5	7.5	10.5	5.5	11.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 3	7.0 7.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 3	1.0 1.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width High or Low	Waveform 1	4.0 7.0			4.0 7.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 2	7.0			7.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	7.0			7.0		ns